51C87
8192 x 8 BIT CHMOS INTEGRATED RAM

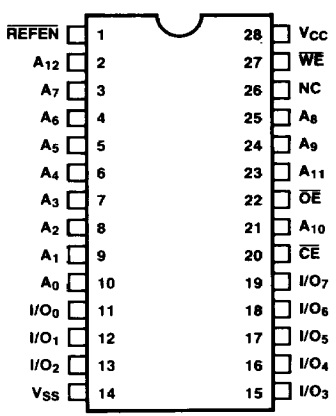
	51C87-12	51C87-15	51C87-20
Maximum Access Time (ns)	120	150	200
Maximum Cycle Time (ns)	175	220	330
Maximum Current (mA)	40	40	40

- **Low Voltage Data Retention**
- **Fast Access Time**
- **Low Standby Current - 200 μA**
- **Low Operating Current - 40 mA**
- **CHMOS III-D technology**
- **Latched Address Inputs**
- **Simple user controlled refresh**
- **Low Input/Output Capacitance**
- **Fully TTL and HCT Compatible**
- **High Reliability Plastic — 28 Pin DIP**

The Intel 51C87 is a high speed 8192 word x8-bit integrated random access memory (iRAM) fabricated on Intel's CHMOS III-D technology, offering high speed and low power. Simple user controlled refresh and integrated refresh control provides static RAM characteristics at a considerable price reduction. The inputs and outputs are fully TTL and HCT compatible and have significantly lower capacitances to allow increased system performance.

These features make the 51C87 ideally suited for microcontroller applications and incorporates many requisite system features including low power dissipation, automatic initialization, extended cycle operation and two-line control to eliminate bus contention.

PIN CONFIGURATION



PIN NAMES

$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
A_0-A_{12}	ADDRESS INPUTS
I/O_0-I/O_7	INPUT/OUTPUT PINS
$\overline{REFEN}$	REFRESH ENABLE
V_{CC}	POWER (+5V)
V_{SS}	GROUND

A1618

MARCH, 1985
ORDER NUMBER: 280088-002

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..Plastic −55 °C to +125°C
Voltage on Any Pin except V_{CC} and D_{OUT} Relative to V_{SS} ..... −2.0 to 7.0V
Voltage on V_{CC} Relative to V_{SS} ..... −1.0V to 7.0V
Voltage on D_{OUT} Relative to V_{SS} ..... −2.0V to V_{CC} + 1V
Data Out Current ..... 50 mA
Power Dissipation 1.0W

†COMMENT
Stresses above those listed under "Absolute Maximum Rating" may cause damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS[1]

$T_A = 0°C$ to 70°C, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	51C87			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
I_{CC}	Operating Current			40	mA	Minimum Cycle Time	3
I_{SB1}	Standby Current TTL			2	mA	$\overline{CE} = V_{IH}$	
I_{SB2}	Standby Current Extended Refresh			200	μA	$\overline{CE} \geq V_{CC} - 0.5V$ $\overline{REFEN} = V_{SS} + 0.2V$	
I_{SB3}	Standby Current CMOS			50	μA	$\overline{CE} \geq V_{CC} - 0.5V$ $\overline{REFEN} = V_{CC} - 0.5V$	7
V_{DR}	V_{CC} Voltage for Data Retention	3.0			V	$\overline{CE} \geq V_{DR} - 0.2V$ $V_{IN} = V_{SS}$ to V_{DR} $\overline{REFEN} = V_{SS} + 0.2V$	6
I_{DR}	Data Retention Current		50	200	μA	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$ $V_{IN} = V_{SS}$ to V_{DR} $\overline{REFEN} = V_{SS} + 0.2$ V	
$\lvert I_{LI} \rvert$	Input Load Current			10	μA	$V_{IH} = V_{SS}$ to V_{CC}	
$\lvert I_{LO} \rvert$	Output Leakage Current			10	μA	$\overline{OE} = V_{IH}$	
V_{IL}	Input Low Voltage	−0.3		0.8	V		1,4
V_{IH}	Input High Voltage	2.4		$V_{CC} + 1$	V		1
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 2.1$ mA	1,5
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -1$ mA	1,5

NOTES FOR D.C. CHARACTERISTICS:
1. All voltages referenced to V_{SS}.
2. Typical values are at $T_A = 25°C$ and $V_{CC} = +5V$.
3. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max) is measured with the outputs open.
4. Specified V_{IL} min is steady state operation. All A.C. parameters are measured with $V_{IL(min)} \geq V_{SS}$ and $V_{IH(max)} \leq V_{CC}$. During transitions the input may overshoot to −1.0V for periods not to exceed 20 nsec.
5. Test conditions apply only for D.C. Characteristics. All A.C. parameters are measured with a load equivalent to two TTL loads and 100 pF.
6. V_{CC} to V_{DR} voltage slew rate must be greater than or equal to 10 ms/V.
7. Valid only after initialization.

CAPACITANCE†

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Address, D_{IN}		6	pF
C_{IN2}	$\overline{CE}$, $\overline{OE}$, $\overline{WE}$, $\overline{REFEN}$		6	pF
C_{OUT}	D_{OUT}		6	pF

†NOTE:
Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS

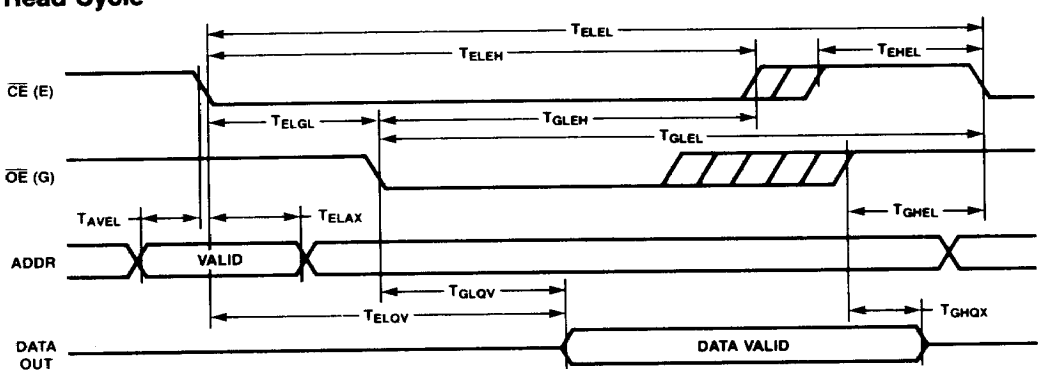
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read Cycle ($\overline{WE} = V_{IH}$)

JEDEC Symbol	Parameter	51C87-12		51C87-15		51C87-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{ELEL}	Cycle Time	175		220		330		ns	
T_{ELQV}	Access Time from $\overline{CE}$		120		150		200	ns	
T_{GLQV}	Access Time from $\overline{OE}$		60		70		90	ns	
T_{ELEH}	$\overline{CE}$ Pulse Width	25		25		25		ns	
T_{EHEL}	$\overline{CE}$ High Time	15		15		15		ns	
T_{AVEL}	Address Set-Up Time	0		0		0		ns	
T_{ELAX}	Address Hold Time	20		25		30		ns	
T_{GLEL}	$\overline{OE}$ low to next $\overline{CE}$ low	100		120		150		ns	
T_{GHEL}	$\overline{OE}$ high to next $\overline{CE}$ low	15		15		15		ns	
T_{GHQX}	$\overline{OE}$ high to Data Float		40		45		55	ns	1
T_{ELGL}	$\overline{CE}$ low to $\overline{OE}$ low		10000		10000		10000	ns	2
T_{GLEH}	$\overline{OE}$ low to $\overline{CE}$ high	20		20		20		ns	

WAVEFORMS

Read Cycle



A.C. CHARACTERISTICS

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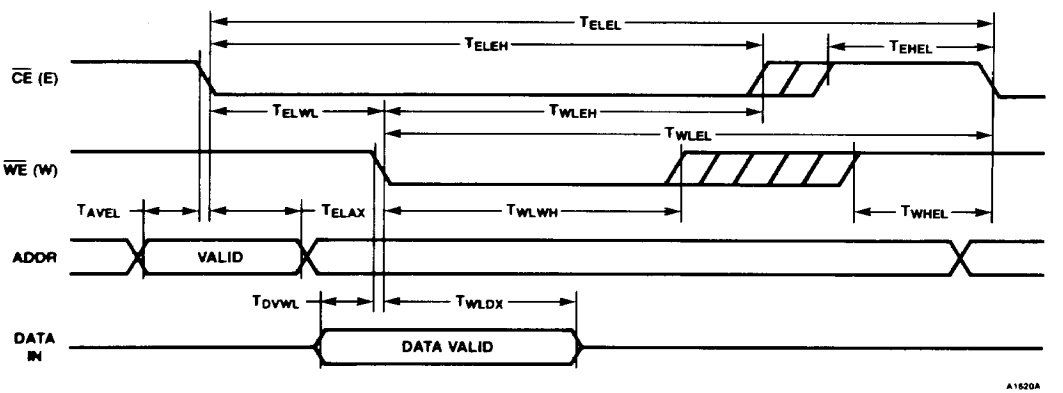
Write Cycle ($\overline{OE} = V_{IH}$)

JEDEC Symbol	Parameter	51C87-12		51C87-15		51C87-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{ELEL}	Cycle Time	175		220		330		ns	
T_{ELEH}	$\overline{CE}$ Pulse Width	25		25		25		ns	
T_{EHEL}	$\overline{CE}$ High Time	15		15		15		ns	
T_{AVEL}	Address Set-Up Time	0		0		0		ns	
T_{ELAX}	Address Hold Time	20		25		35		ns	
T_{WLEL}	$\overline{WE}$ low to next $\overline{CE}$	120		150		200		ns	
T_{WLWH}	$\overline{WE}$ Pulse Width	20		30		40		ns	
T_{WHEL}	$\overline{WE}$ high to next $\overline{CE}$ low	15		15		15		ns	
T_{DVWL}	Date Set-Up to $\overline{WE}$ low	0		0		0		ns	3
T_{WLDX}	Data Hold from $\overline{WE}$ low	20		25		35		ns	3
T_{ELWL}	$\overline{CE}$ low to $\overline{WE}$ low		10000		10000		10000	ns	3
T_{WLEH}	$\overline{WE}$ low to $\overline{CE}$ high	20		20		20		ns	

WAVEFORMS

Write Cycle



A.C. CHARACTERISTICS

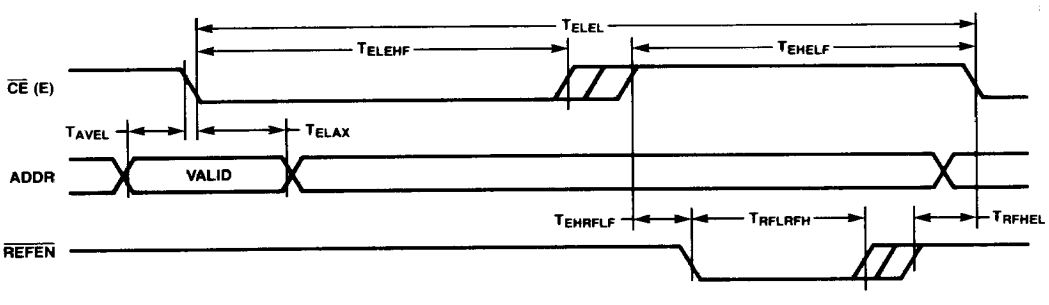
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

False Memory Cycle ($\overline{OE}$ and $\overline{WE} = V_{IH}$)

JEDEC Symbol	Parameter	51C87-12		51C87-15		51C87-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{ELEL}	Cycle Time	175		220		330		ns	
T_{ELEHF}	$\overline{CE}$ Pulse Width	25	10000	25	10000	25	10000	ns	8
T_{EHELF}	$\overline{CE}$ High Time for F.M.C.	90		125		175		ns	9
T_{AVEL}	Address Set-Up Time	0		0		0		ns	
T_{ELAX}	Address Hold Time	20		25		35		ns	
T_{EHRFLF}	$\overline{CE}$ high to $\overline{REFEN}$ low after F.M.C.	100		135		150		ns	
T_{RFHEL}	$\overline{REFEN}$ high to $\overline{CE}$ low	15		15		15		ns	

WAVEFORMS

False Memory Cycle



A.C. CHARACTERISTICS

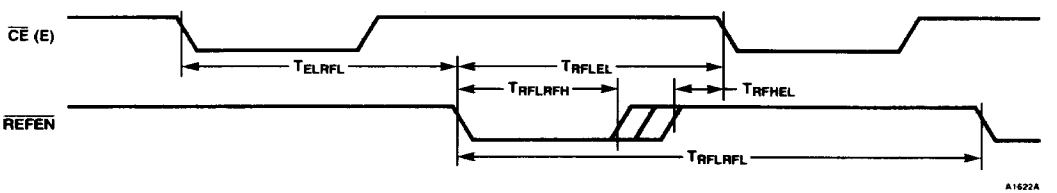
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Refresh Cycle

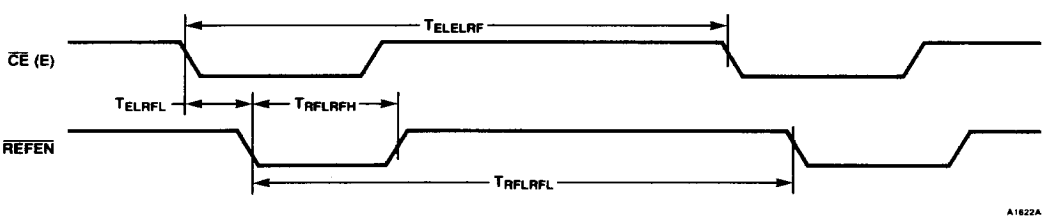
JEDEC Symbol	Parameter	51C87-12		51C87-15		51C87-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{ELRFL}	$\overline{CE}$ low to $\overline{REFEN}$ low	0		0		0		ns	
T_{RFLEL}	$\overline{REFEN}$ low to $\overline{CE}$ low	175		220		330		ns	5
T_{RFHEL}	$\overline{REFEN}$ high to $\overline{CE}$ low	15		15		15		ns	
T_{RFLRFH}	$\overline{REFEN}$ pulse width	20	5000	25	5000	30	5000	ns	4
T_{ELELRF}	Cycle time with a refresh cycle	350		440		660		ns	
T_{RFLRFL}	$\overline{REFEN}$ cycle time to guarantee refresh		31000		31000		31000	ns	
T_{RFHELE}	$\overline{REFEN}$ high to $\overline{CE}$ low - extended cycle	170		220		330		ns	4,7
$T_{RFLRFHE}$	$\overline{REFEN}$ pulse width - extended cycle	5000		5000		5000		ns	4
$T_{RFHRFLE}$	$\overline{REFEN}$ high time - extended cycle	175		220		330		ns	4
T_{VCCRFL}	V_{CC} Min to $\overline{REFEN}$ low - data retention		100		100		100	ns	
T_{VCCRFH}	V_{CC} Min to $\overline{REFEN}$ high - data retention	0		0		0		ns	

WAVEFORMS

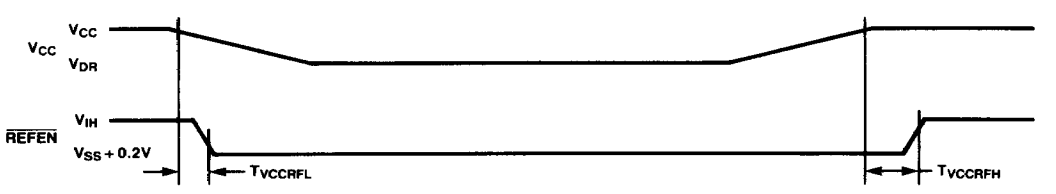
Standard Refresh Cycle[6]



Hidden Refresh Cycle[6]



Low Voltage Data Retention

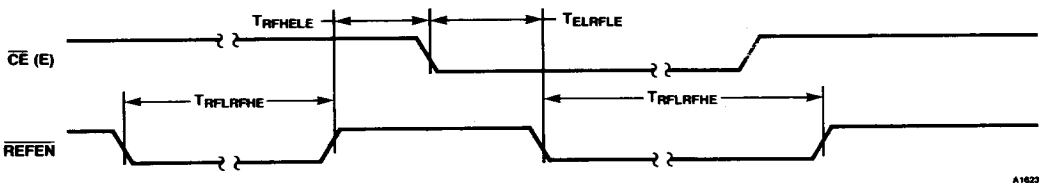


A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

WAVEFORMS

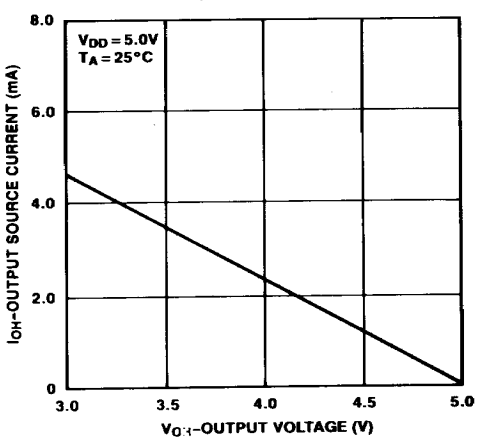
Extended Cycle[4] Refresh



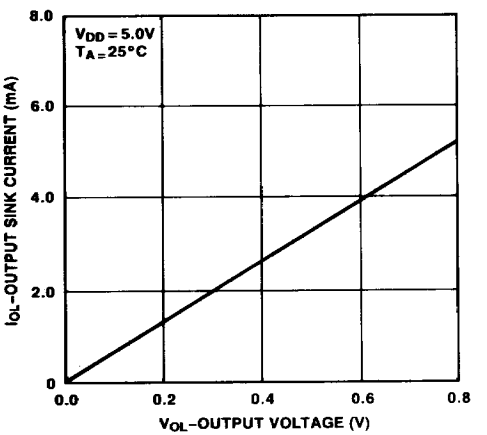
NOTES FOR A.C. CHARACTERISTICS:

1. Transition is measured ±500 mV from steady state logic level.
2. If $\overline{OE}$ low occurs before $\overline{CE}$ then T_{GLQV}, T_{GLEL}, and T_{GLEH}, are referenced from $\overline{CE}$ low.
3. If $\overline{WE}$ low occurs before $\overline{CE}$ then T_{WLEL}, T_{WLWH}, T_{DVWL}, T_{WLDX} and T_{WLEH} are referenced from $\overline{CE}$ low.
4. Extended cycles occur when the $\overline{REFEN}$ pulse width is $> 5\ \mu sec$.
5. Only to guarantee T_{ELQV} min on next cycle. Otherwise T_{RFLEL} min is zero.
6. $\overline{OE}$, $\overline{WE}$ = don't care.
7. $T_{RFHELE} > T_{RFHEL}$
8. Maximum applies for F.M.C. only.
9. Note $T_{EHELF} > T_{EHEL}$

TYPICAL OUTPUT SOURCE CURRENT
I_{OH} VS. V_{OH}



TYPICAL OUTPUT SINK CURRENT
I_{OL} VS. V_{OL}



FUNCTIONAL DESCRIPTION

The 51C87 has four control pins: $\overline{CE}$ (Chip Enable), $\overline{OE}$ (Output Enable), $\overline{WE}$ (Write Enable), and $\overline{REFEN}$ (Refresh Enable). These control lines select and control the operation of the iRAM.

$\overline{CE}$ is the general purpose chip enable line. It is an edge triggered signal that controls several internal operations. An access cycle begins with the leading (falling) edge of $\overline{CE}$. At this time, the external address is latched into the 51C87 and is held throughout the current cycle. $\overline{CE}$ may be pulsed or it may remain low throughout the cycle.

$\overline{OE}$ selects a read cycle and controls the output data bus. When $\overline{OE}$ goes active (low) during a read cycle, the output drivers of the 51C87 are enabled. Data remains valid on the output lines as long as $\overline{OE}$ is active - independent of the state of $\overline{CE}$.

$\overline{WE}$ is the edge triggered input that defines a write cycle. During write cycles, data is latched from the external bus into the 51C87 by the leading (falling) edge of $\overline{WE}$. $\overline{WE}$ and $\overline{OE}$ may not be active during the same cycle.

$\overline{REFEN}$ initiates the internal refresh cycles of the 51C87. A refresh cycle is queued when $\overline{REFEN}$ goes active (low) and will start either immediately or after the present access cycle is completed. An internal refresh address counter provides the refresh address.

ACCESS CYCLES

Read Cycle

A read cycle is initiated by $\overline{CE}$ and $\overline{OE}$ both going active low during the same cycle. $\overline{CE}$ may be either pulsed to initiate a cycle or held active low throughout the cycle. $\overline{OE}$ is a logic level; $\overline{OE}$ controls the 51C87 data output bus. Access times are specified from both $\overline{OE}$ and $\overline{CE}$. Data remains on the data bus until $\overline{OE}$ returns inactive (high) independent of $\overline{CE}$. $\overline{WE}$ may not go active low during a Read cycle.

Write Cycle

A write cycle is initiated by $\overline{CE}$ and $\overline{WE}$ going active low during the same cycle. $\overline{CE}$ may be a pulse or a logic level. $\overline{WE}$ leading edge latches data from the bus into the 51C87. $\overline{OE}$ may not go active low during a Write cycle.

False Memory Cycle

A false memory cycle (FMC) occurs when $\overline{CE}$ goes active (low), and $\overline{OE}$ and $\overline{WE}$ remain inactive (high). No memory cycle is performed, but address set-up and hold times must be met to guarantee the integrity of internal data. During an FMC, the 51C87 performs a refresh cycle on the externally addressed row.

Note that some of the $\overline{CE}$ timing specifications for an FMC differ from those of a read of write cycle.

OTHER OPERATING MODES

Refresh Operation

The 51C87 supports three refresh modes. Two are controlled externally. The third mode can be enabled when the 51C87 is not accessed for extended periods of time (during system stand-by or extended cycle operation). An internal refresh timer guarantees refresh to maintain data integrity.

A refresh cycle is initiated by the leading (falling) edge of $\overline{REFEN}$. Once a refresh cycle begins, cycle operation is internal and automatic. $\overline{REFEN}$ may go inactive (high) after the minimum active low pulse time has been met. Addresses are supplied by the internal refresh address counter. To guarantee internal data integrity, $\overline{REFEN}$ must be strobed at least 256 times in every 4 millisecond period. $\overline{REFEN}$ pulses may be distributed or grouped (burst mode). Both $\overline{REFEN}$ and $\overline{CE}$ may be active low concurrently as long as enough time is allowed for both an access and a refresh cycle before the next $\overline{CE}$ low (i.e. T_{ELELRF}).

The 51C87 may also be refreshed by performing Read, Write, or False Memory cycles on all 256 rows (A0-A6,A12) within a four millisecond period.

Extended Cycles Operation

Extended cycle operation is defined as holding $\overline{OE}$ or $\overline{WE}$ valid (low) for indefinite periods. ($\overline{CE}$ is allowed to return high). Data will remain valid on the bus as long as $\overline{OE}$ is valid. $\overline{WE}$ latches data on the leading (falling) edge. Throughout the remainder of the extended cycle, data may change on the external lines without affecting the contents of the iRAM.

To guarantee refresh of the iRAM array during extended cycles, at reduced data retention voltages or during system standby, $\overline{REFEN}$ must go active low. While $\overline{REFEN}$ is low, an internal timer guarantees that the iRAM array is adequately refreshed, thus insuring data integrity. Refresh cycles will occur automatically, even if $\overline{OE}$ or $\overline{WE}$ remains low. Note that if $\overline{REFEN}$ is not enabled (low), proper refresh of the 51C87 cannot be guaranteed during extended cycles or system standby.

Once $\overline{REFEN}$ returns inactive (high), there are two timing specifications that must be met before the iRAM is accessed again. These are T_{RFLEL} and T_{RFHELE}.

Initialization

The 51C87 is initialized by holding $\overline{REFEN}$ active (low) and all other inputs inactive (high) during power-up and for 100 microseconds after V_{CC} is within specification. Normal operation may begin immediately after initialization.

Additionally, initialization can be done by performing 256 cycles (READ, WRITE or FMC) after V_{CC} is within specification.

Interfacing Considerations

The 51C87 is an edge enabled RAM. A stable $\overline{CE}$ clock is necessary to avoid accidently selecting the RAM. Generally, stable select signals are desirable in all types of microsystem applications. Most common decoding circuits allow addresses to flow directly through the decoder (i.e. decoder permanently enabled). This technique may allow false decoder outputs to occur when addresses are in transition. This may result in false $\overline{CE}$ signals and potentially, invalid memory requests. A simple gating circuit will inhibit enabling the decoder until addresses are valid at the decoder inputs.

Another interfacing consideration is the relationship between $\overline{WE}$ and valid data. The 51C87 performs a write operation on the leading edge of $\overline{WE}$. In a minimum mode 8088 or 8086 system, $\overline{WE}$ occurs before data is valid. A cross-coupled NAND gate configuration on the $\overline{WR}$ signal will prevent this from occurring. This implementation also guarantees valid data on the rising (trailing) edge of $\overline{WE}$ to maintain compatibility with fully static RAMs. (For maximum mode 8088 or 8086 operation, the control signal $\overline{MWTC}$ directly from the 8288 bus controller serves the same function.)