National Semiconductor

April 1997

54AC/74AC574 • 54ACT/74ACT574
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT574 is functionally identical to the 'AC/'ACT374 except for the pinouts.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'AC/'ACT374
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT574 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'ACT574: 5962-89601

Ordering Code: See Section 0

Commercial	Military	Package Number	Package Description
74AC574PC		N20A	20-Lead Molded Dual-In-Line (0.300" Wide)
74AC574SC (Note 1)		M20B	20-Lead Molded Small Outline (0.300" Wide), JEDEC
74AC574SJ (Note 1)		M20D	20-Lead Molded Small Outline, EIAJ Type II
74ACT574PC		N20A	20-Lead Molded Dual-In-Line (0.300" Wide)
74ACT574SC (Note 1)		M20B	20-Lead Molded Small Outline (0.300" Wide), JEDEC
74ACT574SJ (Note 1)		M20D	20-Lead Molded Small Outline, EIAJ Type II
74ACT574MTC (Note 1)		MTC20	20-Lead Molded Thin Shrink Small Outline Package, JEDEC
	54AC574DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
	54AC574FM (Note 2)	W20A	20-Lead Cerpak
	54AC574LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
	54ACT574DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
	54ACT574FM (Note 2)	W20A	20-Lead Cerpak
	54ACT574LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" Tape and Reel. Use suffix SCX, SJX, and MTCX.

Note 2: Military grade device with environmental and burn-in processing, use suffix DMQB, FMQB and LMQB.

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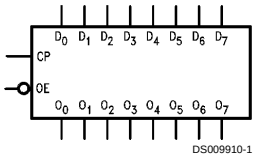
54AC/74AC574 • 54ACT/74ACT574 Octal D-Type Flip-Flop with TRI-STATE Outputs

DSXXX

Logic Symbols



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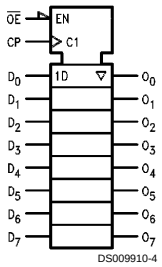
IEEE/IEC



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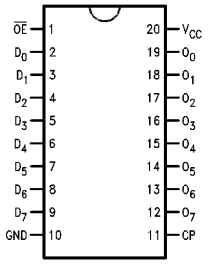
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Connection Diagrams

Pin Assignment for DIP, Flatpak, SOIC and TSSOP



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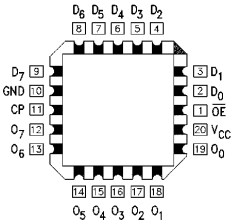
Pin Assignment for LCC



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Functional Description

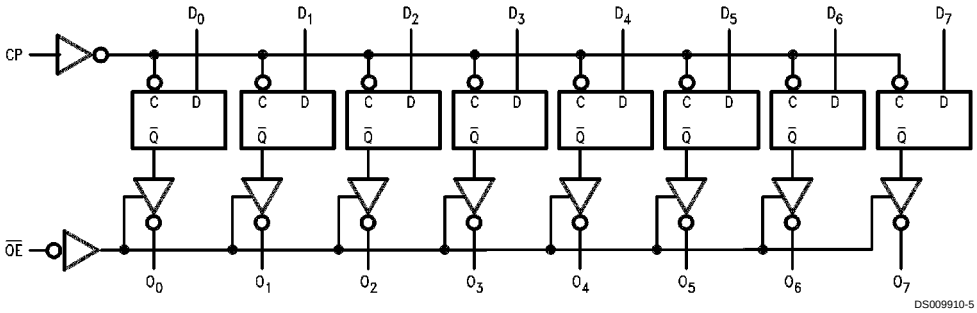
The 'AC/'ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	L	Z	Load
H	⌐	H	H	Z	Load
L	⌐	L	L	L	Data Available
L	⌐	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C
PDIP	140˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
(Unless Otherwise Specified) (AC)	2.0V to 6.0V
(ACT)	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40˚C to +85˚C
54AC/ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 3: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25˚C		54AC T_A = −55˚C to +125˚C	74AC T_A = −40˚C to +85˚C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High	3.0	1.5	2.1	2.1	2.1		V_{OUT} = 0.1V
	Level Input	4.5	2.25	3.15	3.15	3.15	V	or V_{CC} − 0.1V
	Voltage	5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low	3.0	1.5	0.9	0.9	0.9		V_{OUT} = 0.1V
	Level Input	4.5	2.25	1.35	1.35	1.35	V	or V_{CC} − 0.1V
	Voltage	5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High	3.0	2.99	2.9	2.9	2.9		I_{OUT} = −50 μA
	Level Output	4.5	4.49	4.4	4.4	4.4	V	
	Voltage	5.5	5.49	5.4	5.4	5.4		
								(Note 4) V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low	3.0	0.002	0.1	0.1	0.1		I_{OUT} = 50 μA
	Level Output	4.5	0.001	0.1	0.1	0.1	V	
	Voltage	5.5	0.001	0.1	0.1	0.1		
								(Note 4) V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.25	±5.0	±2.5	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	(Note 5) Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	µA	V_{IN} = V_{CC} or GND

Note 4: All outputs loaded; thresholds on input associated with output under test.

Note 5: Maximum test duration 2.0 ms, one output loaded at a time.

Note 6: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V
		5.5	1.5	2.0	2.0	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V
		5.5	1.5	0.8	0.8	0.8		or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 µA
		5.5	5.49	5.4	5.4	5.4		
								(Note 7) V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.70	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.70	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 µA
		5.5	0.001	0.1	0.1	0.1		
								(Note 7) V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.25	±5.0	±2.5	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	(Note 8) Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	µA	V_{IN} = V_{CC} or GND

DC Characteristics for 'ACT Family Devices (Continued)

Note 7: All outputs loaded; thresholds on input associated with output under test.

Note 8: Maximum test duration 2.0 ms, one output loaded at a time.

Note 9: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

See Section 0 for Waveforms

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Symbol	Parameter	V_{CC} (Note 10) (V)	74AC T_A = +25°C C_L = 50 pF			54AC T_A = −55°C to +125°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock	3.3	75	112		55		60		MHz	
	Frequency	5.0	95	153		85		85			
t_{PLH}	Propagation Delay	3.3	3.5	8.5	13.5	1.0	16.5	3.5	15.0	ns	♦♦-♦♦
	CP to O_n	5.0	2.0	6.0	9.5	1.5	11.5	2.0	11.0		
t_{PHL}	Propagation Delay	3.3	3.5	7.5	12.0	1.0	15.0	3.5	13.5	ns	♦♦-♦♦
	CP to O_n	5.0	2.0	5.5	8.5	1.5	10.5	2.0	9.5		
t_{PZH}	Output Enable Time	3.3	2.5	7.0	11.0	1.0	13.0	2.5	12.0	ns	♦♦-♦♦
		5.0	2.0	5.0	8.5	1.5	9.5	2.0	9.0		
t_{PZL}	Output Enable Time	3.3	3.0	6.5	10.5	1.0	12.5	3.0	11.5	ns	♦♦-♦♦
		5.0	2.0	5.0	8.0	1.5	9.5	1.5	9.0		
t_{PHZ}	Output Disable Time	3.3	3.5	7.5	12.0	1.0	14.0	2.5	13.0	ns	♦♦-♦♦
		5.0	2.0	6.0	9.5	1.5	11.5	1.5	10.5		
t_{PLZ}	Output Disable Time	3.3	2.0	5.5	9.0	1.0	10.5	1.5	10.0	ns	♦♦-♦♦
		5.0	1.0	4.5	7.5	1.5	9.0	1.0	8.5		

Note 10: Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

See Section 0 for Waveforms

DSXXX

Symbol	Parameter	V_{CC} (Note 11) (V)	74AC T_A = +25°C C_L = 50 pF		54AC T_A = −55°C to +125°C C_L = 50 pF	74AC T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-Up Time, HIGH or LOW	3.3	0.5	2.5	4.5	3.0	ns	♦♦-♦♦
	D_n to CP	5.0	0	1.5	3.5	2.0		
t_h	Hold Time, HIGH or LOW	3.3	−0.5	1.5	2.5	1.5	ns	♦♦-♦♦
	D_n to CP	5.0	0	1.5	2.5	1.5		
t_w	CP Pulse Width	3.3	3.5	6.0	7.5	7.0	ns	♦♦-♦♦
	HIGH or LOW	5.0	2.0	4.0	5.0	5.0		

Note 11: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

See Section 0 for Waveforms

Symbol	Parameter	V_{CC} (Note 12) (V)	74ACT T_A = +25°C C_L = 50 pF			54ACT T_A = −55°C to +125°C C_L = 50 pF		74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	5.0	100	110		70		85		ns	
t_{PLH}	Propagation Delay CP to O_n	5.0	2.5	7.0	11.0	1.5	13.5	2.0	12.0	ns	⧫⧫-⧫⧫
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	6.5	10.0	1.5	12.5	1.5	11.0	ns	⧫⧫-⧫⧫
t_{PZH}	Output Enable Time	5.0	2.0	6.4	9.5	1.5	11.0	1.5	10.0	ns	⧫⧫-⧫⧫
t_{PZL}	Output Enable Time	5.0	2.0	6.0	9.0	1.5	11.0	1.5	10.0	ns	⧫⧫-⧫⧫
t_{PHZ}	Output Disable Time	5.0	2.0	7.0	10.5	1.5	12.0	1.5	11.5	ns	⧫⧫-⧫⧫
t_{PLZ}	Output Disable Time	5.0	2.0	5.5	8.5	1.5	10.0	1.5	9.0	ns	⧫⧫-⧫⧫

Note 12: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

See Section 0 for Waveforms

Symbol	Parameter	V_{CC} (Note 13) (V)	74ACT T_A = +25°C C_L = 50 pF		54ACT T_A = −55°C to +125°C C_L = 50 pF	74ACT T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-Up Time, HIGH or LOW D_n to CP	5.0	1.5	2.5	3.5	2.5	ns	⧫⧫-⧫⧫
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	2.0	1.0	ns	⧫⧫-⧫⧫
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	3.0	5.0	4.0	ns	⧫⧫-⧫⧫

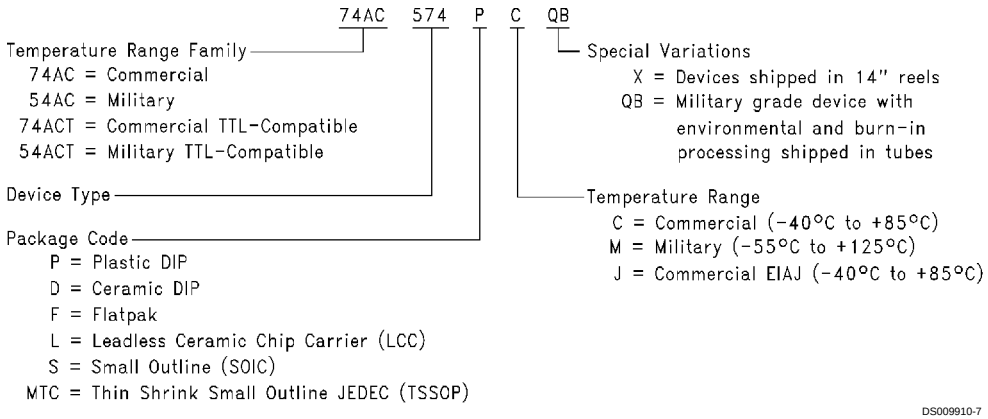
Note 13: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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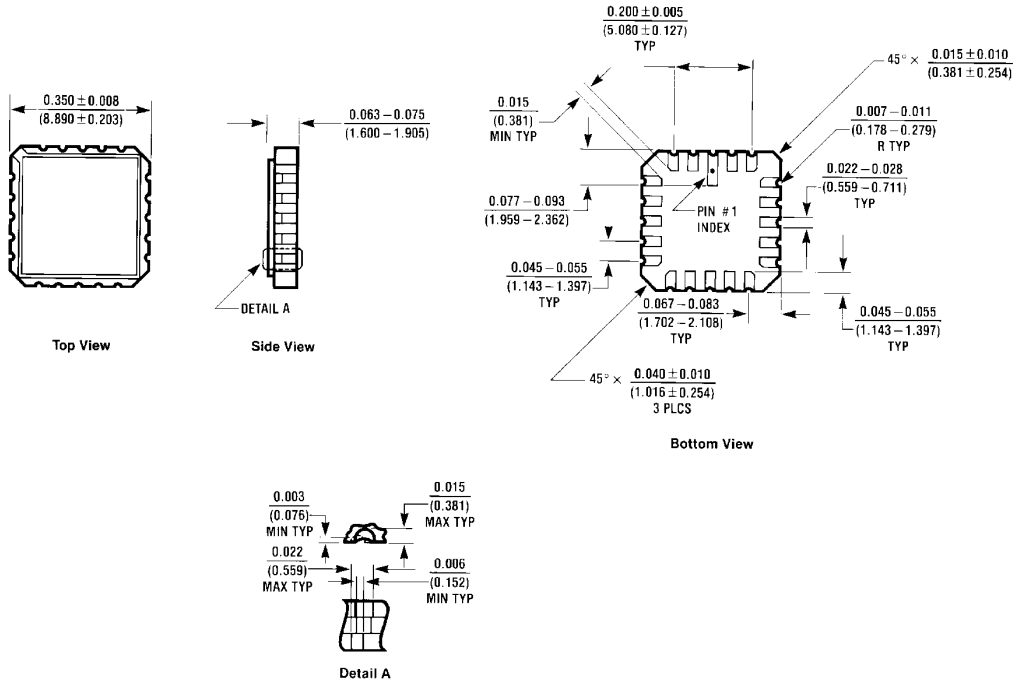
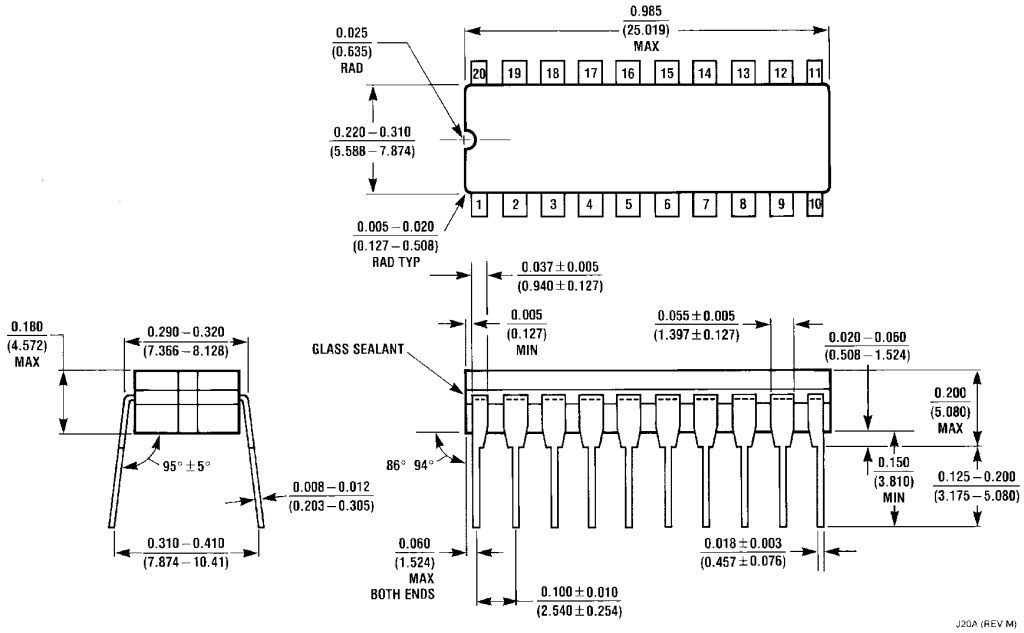
Physical Dimensions inches (millimeters)

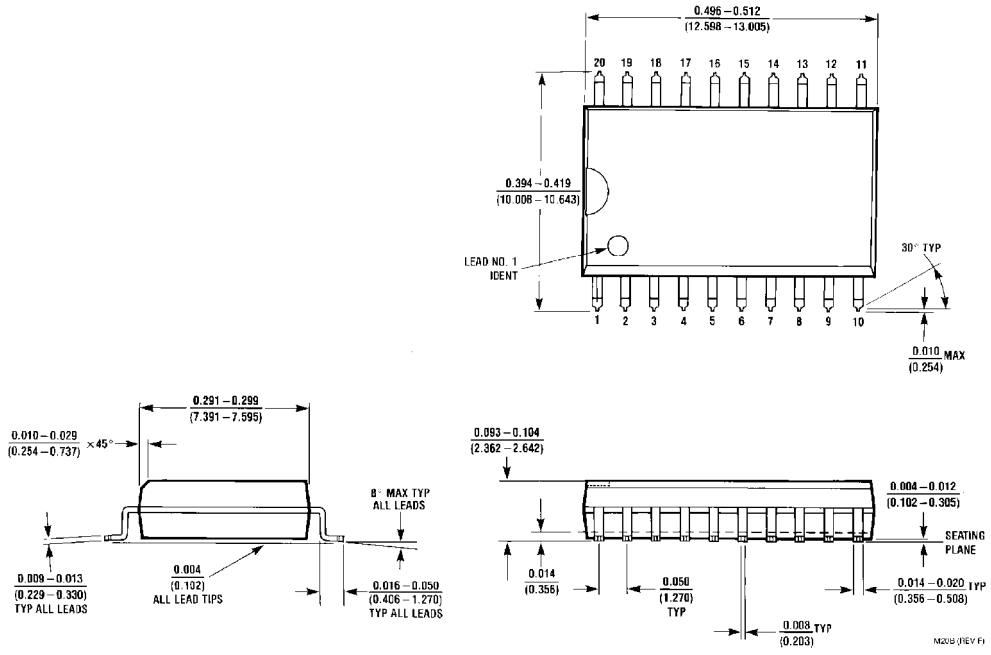


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)

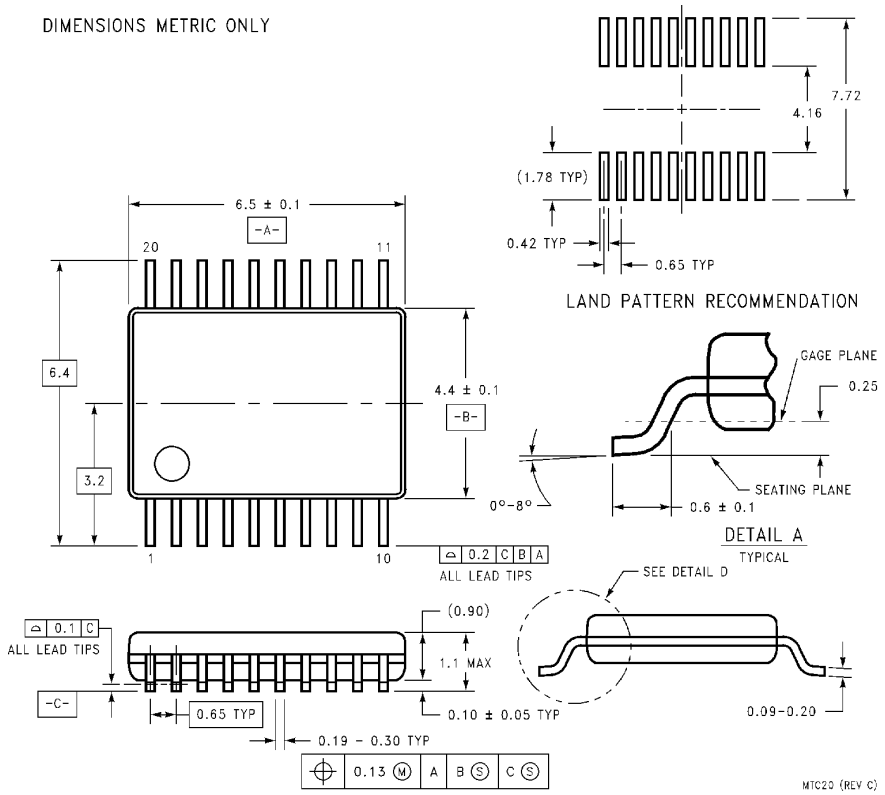


20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

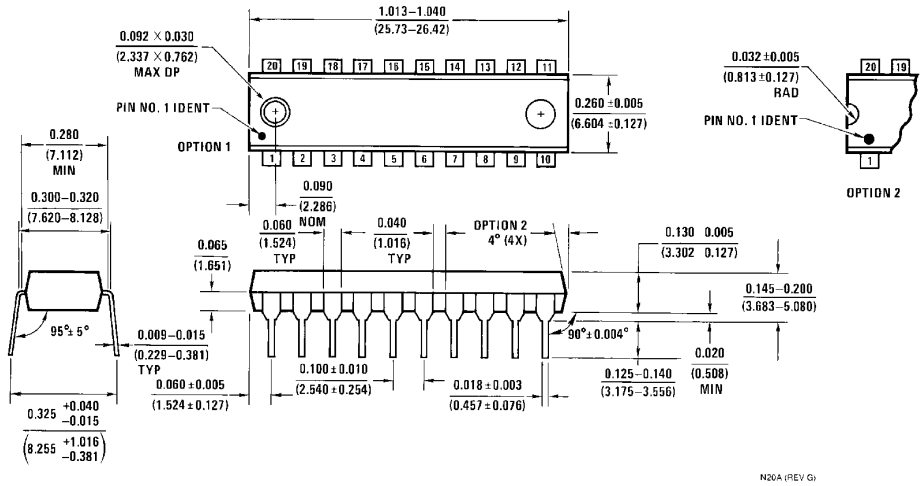


20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

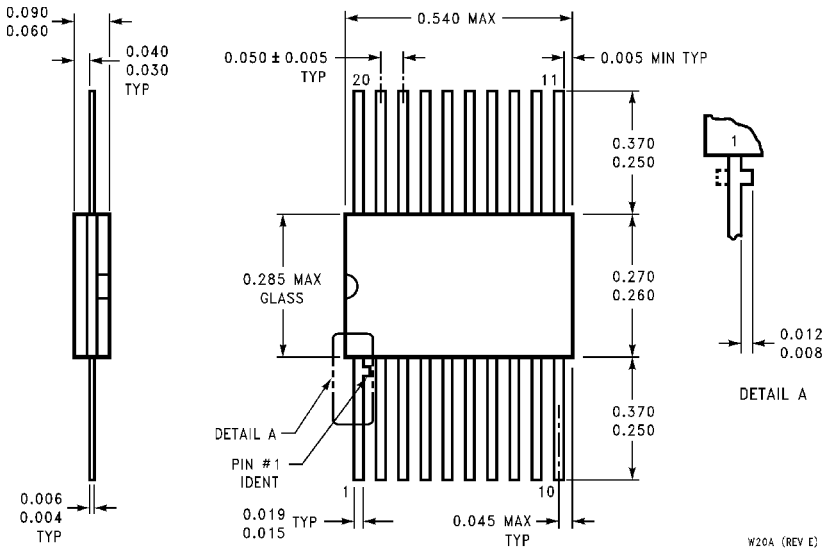


20-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTC20



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



20 Lead Ceramic Flatpak (F)
NS Package Number W20A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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