

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT132

Quad 2-input NAND Schmitt trigger

Product specification
File under Integrated Circuits, IC06

September 1993

Quad 2-input NAND Schmitt trigger

74HC/HCT132

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT132 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT132 contain four 2-input NAND gates which accept standard input signals. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The gate switches at different points for positive and negative-going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H .

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|--|--|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay nA, nB to nY | $C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$ | 11 | 17 | ns |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per gate | notes 1 and 2 | 24 | 20 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$

For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

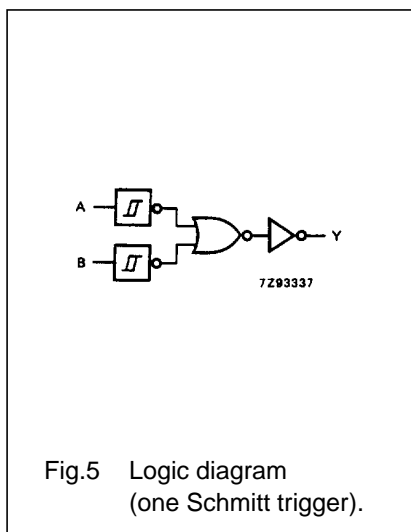
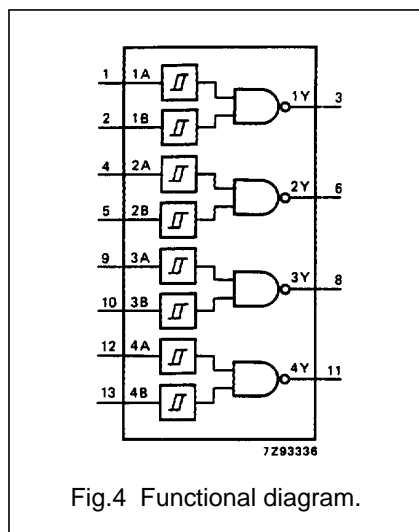
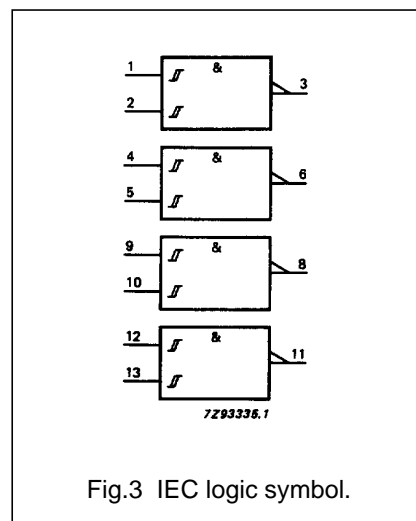
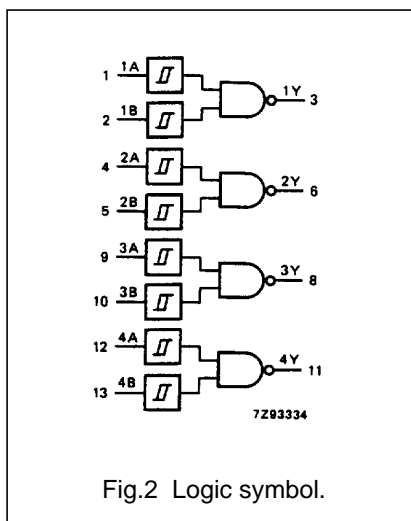
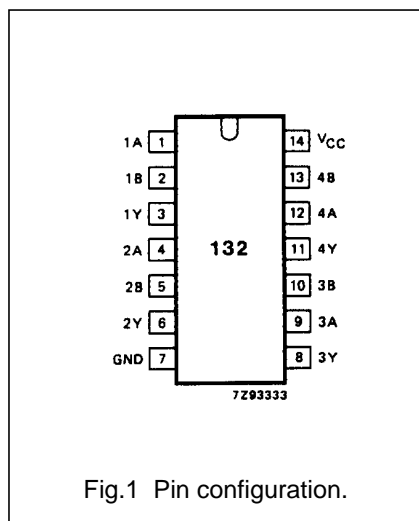
See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Quad 2-input NAND Schmitt trigger

74HC/HCT132

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------|-----------------|-------------------------|
| 1, 4, 9, 12 | 1A to 4A | data inputs |
| 2, 5, 10, 13 | 1B to 4B | data inputs |
| 3, 6, 8, 11 | 1Y to 4Y | data outputs |
| 7 | GND | ground (0 V) |
| 14 | V _{CC} | positive supply voltage |



FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|----|--------|
| nA | nB | nY |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

Notes

- H = HIGH voltage level
L = LOW voltage level

APPLICATIONS

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators

Quad 2-input NAND Schmitt trigger

74HC/HCT132

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*". Transfer characteristics are given below.

Output capability: standard

I_{CC} category: SSI

Transfer characteristics for 74HC

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-----------------|---|-----------------------|------|------|------------|------|-------------|------|---|------|------------------------|-----------|
| | | 74HC | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| V _{T+} | positive-going threshold | 0.7 | 1.18 | 1.5 | 0.7 | 1.5 | 0.7 | 1.5 | V | 2.0 | Figs 6 and 7 | |
| | | 1.7 | 2.38 | 3.15 | 1.7 | 3.15 | 1.7 | 3.15 | | 4.5 | | |
| | | 2.1 | 3.14 | 4.2 | 2.1 | 4.2 | 2.1 | 4.2 | | 6.0 | | |
| V _{T-} | negative-going threshold | 0.3 | 0.63 | 1.0 | 0.3 | 1.0 | 0.3 | 1.0 | V | 2.0 | Figs 6 and 7 | |
| | | 0.9 | 1.67 | 2.2 | 0.9 | 2.2 | 0.9 | 2.2 | | 4.5 | | |
| | | 1.2 | 2.26 | 3.0 | 1.2 | 3.0 | 1.2 | 3.0 | | 6.0 | | |
| V _H | hysteresis (V _{T+} - V _{T-}) | 0.2 | 0.55 | 1.0 | 0.2 | 1.0 | 0.2 | 1.0 | V | 2.0 | Figs 6 and 7 | |
| | | 0.4 | 0.71 | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | | 4.5 | | |
| | | 0.6 | 0.88 | 1.6 | 0.6 | 1.6 | 0.6 | 1.6 | | 6.0 | | |

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|-----------------------------------|-----------------------|------|------|------------|------|-------------|------|----|------|------------------------|-----------|
| | | 74HC | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 TO +85 | | -40 TO +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay nA, nB to nY | | 36 | 125 | | 155 | | 190 | ns | 2.0 | Fig.13 | |
| | | | 13 | 25 | | 31 | | 38 | | 4.5 | | |
| | | | 10 | 21 | | 26 | | 32 | | 6.0 | | |
| t _{THL} / t _{TLH} | output transition time | | 19 | 75 | | 95 | | 110 | ns | 2.0 | Fig.13 | |
| | | | 7 | 15 | | 19 | | 22 | | 4.5 | | |
| | | | 6 | 13 | | 16 | | 19 | | 6.0 | | |

Quad 2-input NAND Schmitt trigger

74HC/HCT132

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*". Transfer characteristics are given below.

Output capability: standard

I_{CC} category: SSI

Notes to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|--------|-----------------------|
| nA, nB | 0.3 |

Transfer characteristics for 74HCT

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|----------|----------------------------------|----------------|------|------|------------|------|-------------|------|---|------|-----------------|-----------|
| | | 74HCT | | | | | | | | | V_{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| V_{T+} | positive-going threshold | 1.2 | 1.41 | 1.9 | 1.2 | 1.9 | 1.2 | 1.9 | V | 4.5 | Figs 6 and 7 | |
| | | 1.4 | 1.59 | 2.1 | 1.4 | 2.1 | 1.4 | 2.1 | | | | |
| V_{T-} | negative-going threshold | 0.5 | 0.85 | 1.2 | 0.5 | 1.2 | 0.5 | 1.2 | V | 4.5 | Figs 6 and 7 | |
| | | 0.6 | 0.99 | 1.4 | 0.6 | 1.4 | 0.6 | 1.4 | | | | |
| V_H | hysteresis ($V_{T+} - V_{T-}$) | 0.4 | 0.56 | – | 0.4 | – | 0.4 | – | V | 4.5 | Figs 6 and 7 | |
| | | 0.4 | 0.60 | – | 0.4 | – | 0.4 | – | | | | |

AC CHARACTERISTICS FOR 74HCT

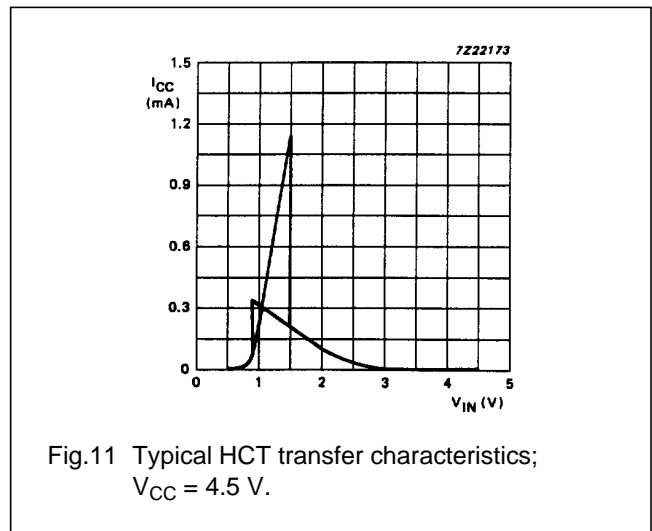
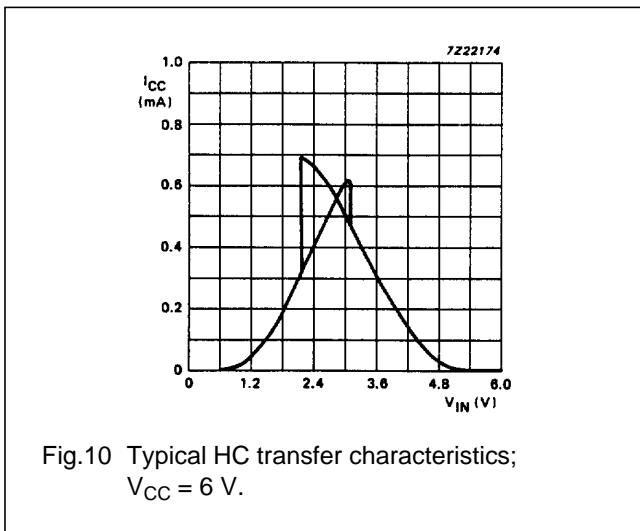
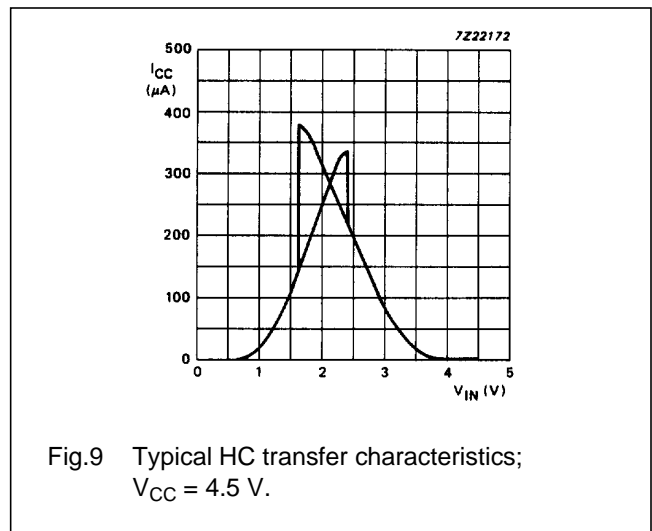
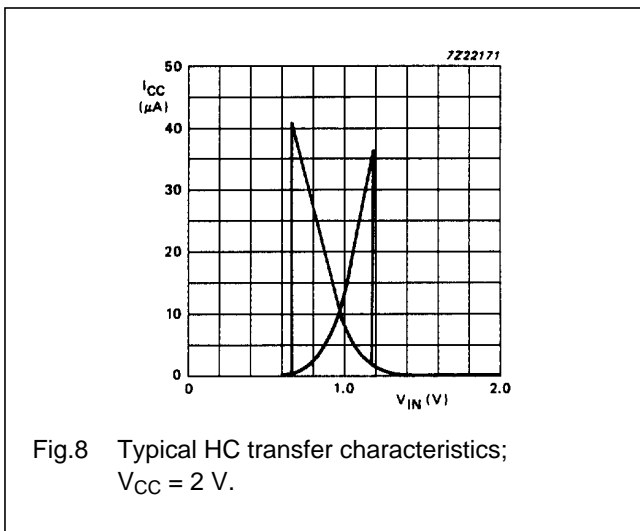
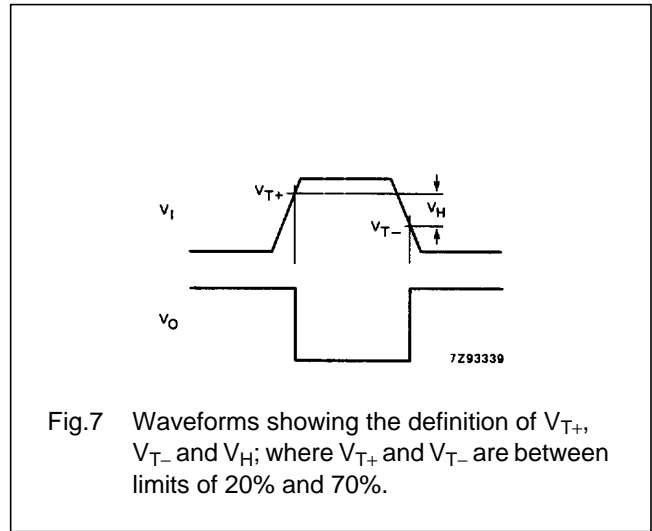
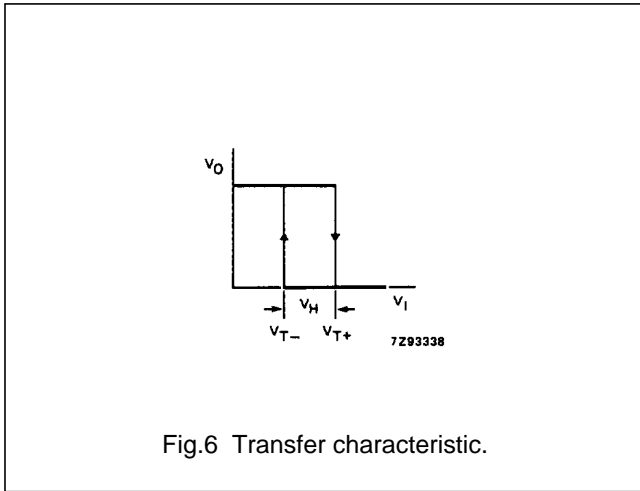
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|---------------------|-----------------------------------|----------------|------|------|------------|------|-------------|------|----|------|-----------------|-----------|
| | | 74HCT | | | | | | | | | V_{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t_{PHL} / t_{PLH} | propagation delay nA, nB to nY | | 20 | 33 | | 41 | | 50 | ns | 4.5 | Fig.13 | |
| t_{THL} / t_{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.13 | |

Quad 2-input NAND Schmitt trigger

74HC/HCT132

TRANSFER CHARACTERISTIC WAVEFORMS



Quad 2-input NAND Schmitt trigger

74HC/HCT132

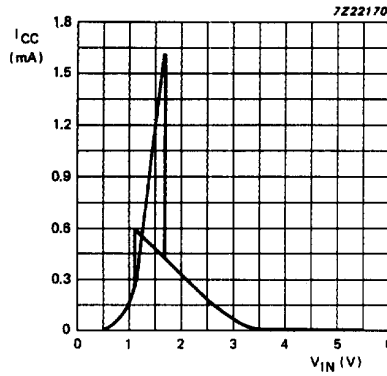
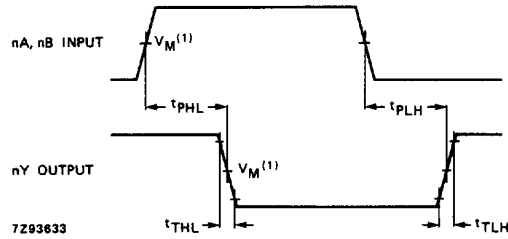


Fig.12 Typical HCT transfer characteristics; $V_{CC} = 5.5 V$.

AC WAVEFORMS



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
 HCT: $V_M = 1.3 V$; $V_I = \text{GND to } 3 V$.

Fig.13 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Quad 2-input NAND Schmitt trigger

74HC/HCT132

Application information

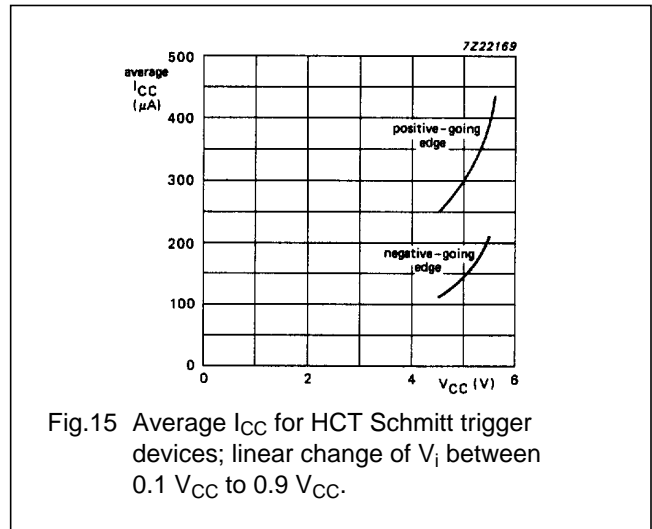
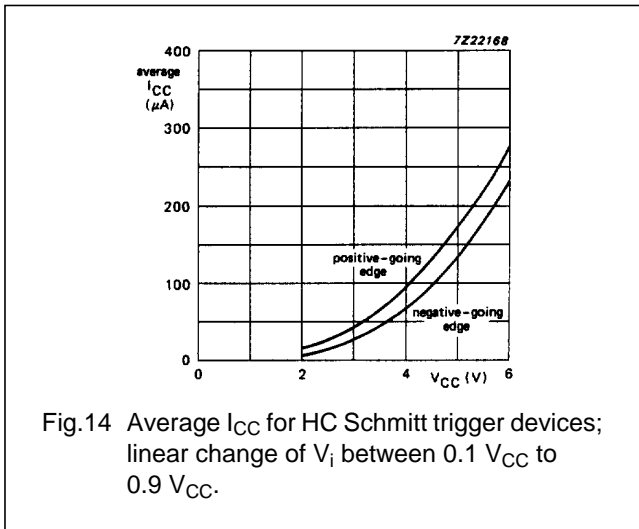
The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$$P_{ad} = f_i \times (t_r \times I_{CCa} + t_f \times I_{CCa}) \times V_{CC}$$

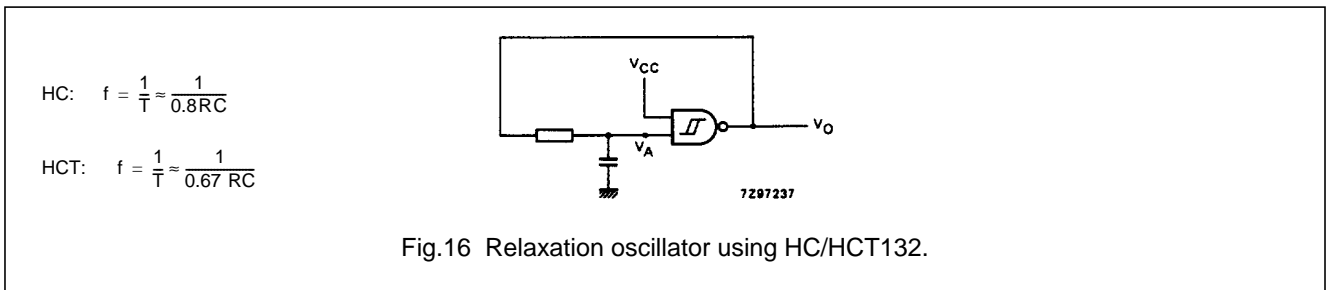
Where:

- P_{ad} = additional power dissipation (μW)
- f_i = input frequency (MHz)
- t_r = input rise time (ns); 10% – 90%
- t_f = input fall time (ns); 10% – 90%
- I_{CCa} = average additional supply current (μA)

Average I_{CCa} differs with positive or negative input transitions, as shown in Figs 14 and 15.



HC/HCT132 used in a relaxation oscillator circuit, see Fig.16.



Note to Application information

All values given are typical unless otherwise specified.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".