# Low Cost, Dual/Triple Video Amplifiers

# AD8072/AD8073

**FEATURES**
**Very Low Cost**
**Good Video Specifications ($R_L$ = 150 Ω)**
- **Gain Flatness of 0.1 dB to 10 MHz**
- **0.05% Differential Gain Error**
- **0.1° Differential Phase Error**

**Low Power**
- **3.5 mA/Amplifier Supply Current**
- **Operates on Single +5 V to +12 V Supply**

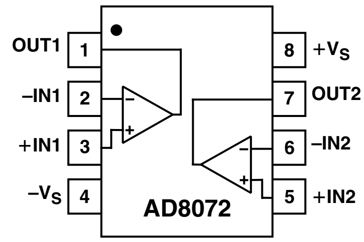
**High Speed**
- **100 MHz, –3 dB Bandwidth (G = +2)**
- **500 V/µs Slew Rate**
- **Fast Settling Time of 25 ns (0.1%)**

**Easy to Use**
- **30 mA Output Current**
- **Output Swing to 1.3 V of Rails on Single +5 V Supply**

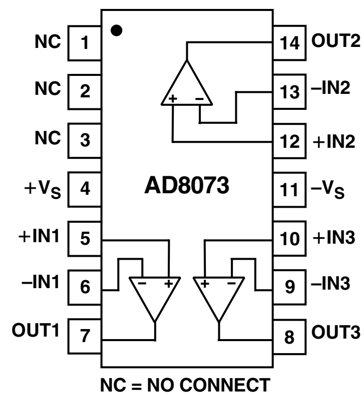
**APPLICATIONS**
**Video Line Driver**
**Computer Video Plug-In Boards**
**RGB or S-Video Amplifier in Component Systems**

**FUNCTIONAL BLOCK DIAGRAMS**

**8-Lead Plastic (N), SOIC (R), and µSOIC (RM) Packages**




**14-Lead Plastic (N), and SOIC (R) Packages**




## PRODUCT DESCRIPTION

The AD8072 (dual) and AD8073 (triple) are low cost, current feedback amplifiers intended for high volume, cost sensitive applications. In addition to being low cost, these amplifiers deliver solid video performance into a 150 Ω load while consuming only 3.5 mA per amplifier of supply current. Furthermore, the AD8073 is three amplifiers in a single 14-lead narrow-body SOIC package. This makes it ideal for applications where small size is essential. Each amplifier's inputs and output are accessible providing added gain setting flexibility.

These devices provide 30 mA of output current per amplifier, and are optimized for driving one back terminated video load (150 Ω) each. These current feedback amplifiers feature gain flatness of 0.1 dB to 10 MHz while offering differential gain and phase error of 0.05% and 0.1°. This makes the AD8072 and AD8073 ideal for business and consumer video electronics.

Both will operate from a single +5 V to +12 V power supply. The outputs of each amplifier swing to within 1.3 volts of either supply rail to accommodate video signals on a single +5 V supply.

The high bandwidth of 100 MHz, 500 V/µs of slew rate, along with settling to 0.1% in 25 ns, make the AD8072 and AD8073 useful in many general purpose, high speed applications where a single +5 V or dual power supplies up to ±6 V are needed. The AD8072 is available in 8-lead plastic DIP, SOIC, and µSOIC packages while the AD8073 is available in 14-lead plastic DIP and SOIC packages. Both operate over the commercial temperature range of 0°C to +70°C. Additionally, the AD8072ARM operates over the industrial temperature range of –40°C to +85°C.

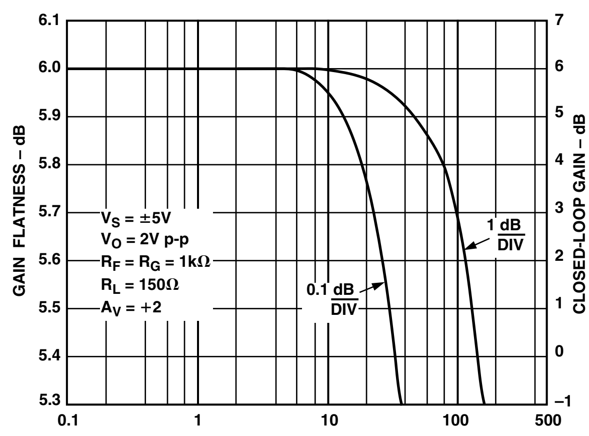



*Figure 1. Large Signal Frequency Response*

REV. A



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# AD8072/AD8073–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $T_A$ = +25°C, $V_S$ = ±5 V, $R_L$ = 150 Ω, unless otherwise noted)

| Parameter | Conditions | AD8072/AD8073 Min | Typ | Max | Units |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | $R_F$ = 1 kΩ | | | | |
| –3 dB Bandwidth, Small Signal | No Peaking, G = +2 | 80 | 100 | | MHz |
| 0.1 dB Bandwidth, Small Signal | No Peaking, G = +2 | 8 | 10 | | MHz |
| Slew Rate | $V_O$ = 4 V Step | | 500 | | V/µs |
| Settling Time to 0.1% | $V_O$ = 2 V Step | | 25 | | ns |
| DISTORTION/NOISE PERFORMANCE | $R_F$ = 1 kΩ | | | | |
| Differential Gain | f = 3.58 MHz, G = +2 | | 0.05 | 0.15 | % |
| Differential Phase | f = 3.58 MHz, G = +2 | | 0.1 | 0.3 | Degrees |
| Crosstalk | f = 5 MHz | | 60 | | dB |
| Input Voltage Noise | f = 10 kHz | | 3 | | nV/$\sqrt{Hz}$ |
| Input Current Noise | f = 10 kHz (±$I_{IN}$) | | 6 | | pA/$\sqrt{Hz}$ |
| DC PERFORMANCE | | | | | |
| Transimpedance | | | 0.3 | | MΩ |
| Input Offset Voltage | | | 2 | 6 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | | 8 | mV |
| Offset Drift | | | 11 | | µV/°C |
| Input Bias Current (±) | | | 4 | 12 | µA |
| Input Bias Current Drift (±) | | | 12 | | nA/°C |
| INPUT CHARACTERISTICS | | | | | |
| –Input Resistance | | | 120 | | Ω |
| +Input Resistance | | | 1 | | MΩ |
| Input Capacitance | | | 1.6 | | pF |
| Common-Mode Rejection Ratio | $V_{CM}$ = –3.8 V to +3.8 V | | 56 | | dB |
| Input Common-Mode Voltage Range | | | ±3.8 | | V |
| OUTPUT CHARACTERISTICS | | | | | |
| +Output Voltage Swing | | 3 | 3.3 | | V |
| –Output Voltage Swing | | 2.25 | 3 | | V |
| Output Current | $R_L$ = 10 Ω | | 30 | | mA |
| Short Circuit Current | | | 80 | | mA |
| POWER SUPPLY | | | | | |
| Operating Range | | | ±2.5 to ±6 | | V |
| Power Supply Rejection Ratio | $V_S$ = ±4 V to ±6 V | | 70 | | dB |
| Quiescent Current per Amplifier | | | 3.5 | 5 | mA |
| OPERATING TEMPERATURE RANGE | | 0 | | +70 | °C |

Specifications subject to change without notice.

# ELECTRICAL CHARACTERISTICS (@ $T_A$ = +25°C, $V_S$ = +5 V, $R_L$ = 150 Ω to 2.5 V, unless otherwise noted)

| Parameter | Conditions | AD8072/AD8073 Min | Typ | Max | Units |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | $R_F$ = 1 kΩ | | | | |
| –3 dB Bandwidth, Small Signal | No Peaking, G = +2 | 78 | 100 | | MHz |
| 0.1 dB Bandwidth, Small Signal | No Peaking, G = +2 | 7.8 | 10 | | MHz |
| Slew Rate | $V_O$ = 2 V Step | | 350 | | V/µs |
| Settling Time to 0.1% | $V_O$ = 2 V Step | | 25 | | ns |
| DISTORTION/NOISE PERFORMANCE | $R_F$ = 1 kΩ | | | | |
| Differential Gain | f = 3.58 MHz, G = +2, $R_L$ to 1.5 V | | 0.1 | | % |
| Differential Phase | f = 3.58 MHz, G = +2, $R_L$ to 1.5 V | | 0.1 | | Degrees |
| Crosstalk | f = 5 MHz | | 60 | | dB |
| Input Voltage Noise | f = 10 kHz | | 3 | | nV/√Hz |
| Input Current Noise | f = 10 kHz (±$I_{IN}$) | | 6 | | pA/√Hz |
| DC PERFORMANCE | | | | | |
| Transimpedance | | | 0.25 | | MΩ |
| Input Offset Voltage | | | 1.5 | 4 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | | 6 | mV |
| Offset Drift | | | 9 | | µV/°C |
| Input Bias Current (±) | | | 3 | 10 | µA |
| Input Bias Current Drift (±) | | | 10 | | nA/°C |
| INPUT CHARACTERISTICS | | | | | |
| –Input Resistance | | | 120 | | Ω |
| +Input Resistance | | | 1 | | MΩ |
| Input Capacitance | | | 1.6 | | pF |
| Common-Mode Rejection Ratio | $V_{CM}$ = +1.2 V to +3.8 V | | 54 | | dB |
| Input Common-Mode Voltage Range | | | +1.2 to +3.8 | | V |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | | +1.5 to +3.5 | +1.3 to +3.7 | | V |
| Output Current | $R_L$ = 10 Ω | | 20 | | mA |
| Short Circuit Current | | | 60 | | mA |
| POWER SUPPLY | | | | | |
| Operating Range | | | ±2.5 to ±6 | | V |
| Power Supply Rejection Ratio | $V_S$ = +4 V to +6 V | | 64 | | dB |
| Quiescent Current per Amplifier | | | 3 | 4.5 | mA |
| OPERATING TEMPERATURE RANGE | | 0 | | +70 | °C |

## ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .13.2 V
Internal Power Dissipation[2]
  AD8072 8-Lead Plastic (N) . . . . . . . . . . . . . . . . . 1.3 Watts
  AD8072 8-Lead Small Outline (SO-8) . . . . . . . . . 0.9 Watts
  AD8072 8-Lead µSOIC (RM) . . . . . . . . . . . . . . . 0.6 Watts
  AD8073 14-Lead Plastic (N) . . . . . . . . . . . . . . . . 1.6 Watts
  AD8073 14-Lead Small Outline (R) . . . . . . . . . . . 1.0 Watts
Input Voltage (Common Mode) . . . . . . . . . . . . . . . . . . . .$\pm V_S$
Differential Input Voltage . . . . . . . . . . . . . . . . . . . . . ±1.25 V
Output Short Circuit Duration . . . . . . . . . . . . . . . . . . . . . . .
  Observe Power Derating Curves
Storage Temperature Range
  N, R, RM Packages . . . . . . . . . . . . . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . . . .+300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead Plastic Package: $\theta_{JA}$ = 90°C/W
8-Lead SOIC Package: $\theta_{JA}$ = 140°C/W
8-Lead µSOIC Package: $\theta_{JA}$ = 214°C/W
14-Lead Plastic Package: $\theta_{JA}$ = 75°C/W
14-Lead SOIC Package: $\theta_{JA}$ = 120°C/W

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD8072ARM | –40°C to +85°C | 8-Lead µSOIC | RM-8 |
| AD8072ARM-REEL | –40°C to +85°C | 13" Reel 8-Lead µSOIC | RM-8 |
| AD8072ARM-REEL7 | –40°C to +85°C | 7" Reel 8-Lead µSOIC | RM-8 |
| AD8072JN | 0°C to +70°C | 8-Lead Plastic DIP | N-8 |
| AD8072JR | 0°C to +70°C | 8-Lead SOIC | SO-8 |
| AD8072JR-REEL | 0°C to +70°C | 13" Reel 8-Lead SOIC | SO-8 |
| AD8072JR-REEL7 | 0°C to +70°C | 7" Reel 8-Lead SOIC | SO-8 |
| AD8073JN | 0°C to +70°C | 14-Lead Plastic DIP | N-14 |
| AD8073JR | 0°C to +70°C | 14-Lead Narrow SOIC | R-14 |
| AD8073JR-REEL | 0°C to +70°C | 13" Reel 14-Lead SOIC | R-14 |
| AD8073JR-REEL7 | 0°C to +70°C | 7" Reel 14-Lead SOIC | R-14 |

## MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8072 and AD8073 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8072 and AD8073 are internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figures 2 and 3.

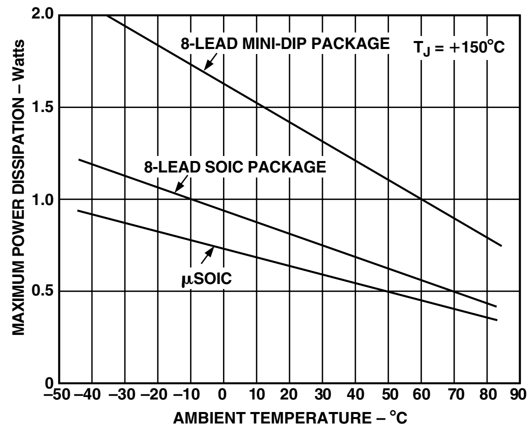



*Figure 2. AD8072 Maximum Power Dissipation vs. Temperature*

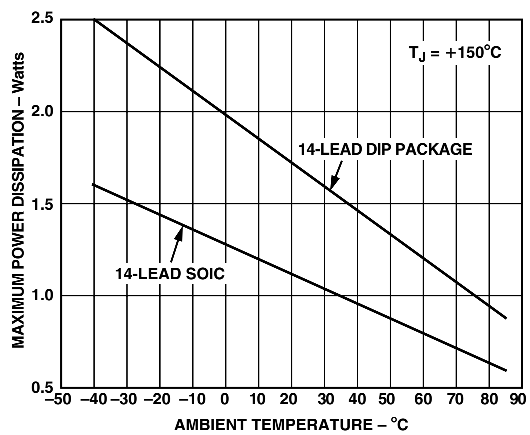



*Figure 3. AD8073 Maximum Power Dissipation vs. Temperature*

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8072 and AD8073 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

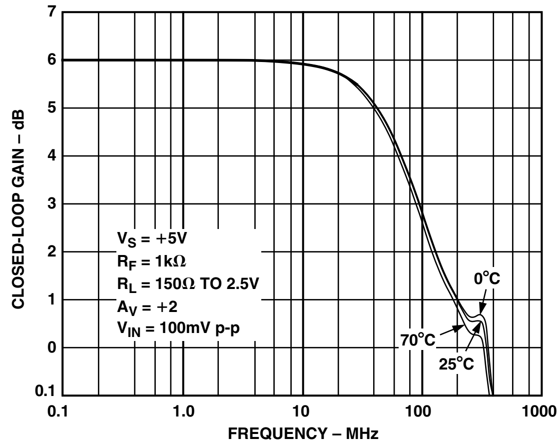



*Figure 4. Frequency Response Over Temperature; $V_S = +5$ V*

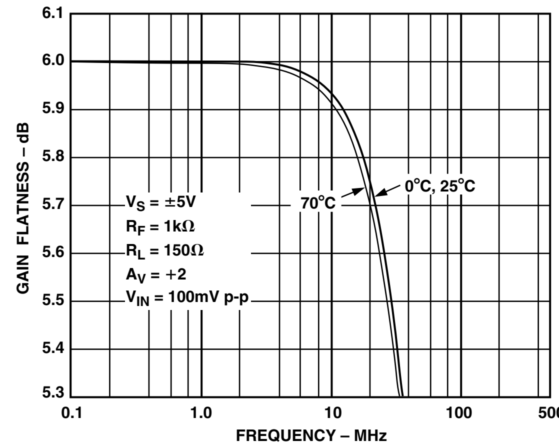



*Figure 7. 0.1 dB Flatness vs. Frequency Over Temperature; $V_S = \pm5$ V*

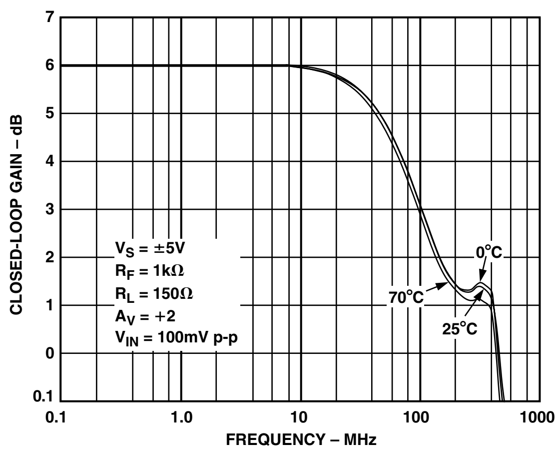



*Figure 5. Frequency Response Over Temperature; $V_S = \pm5$ V*

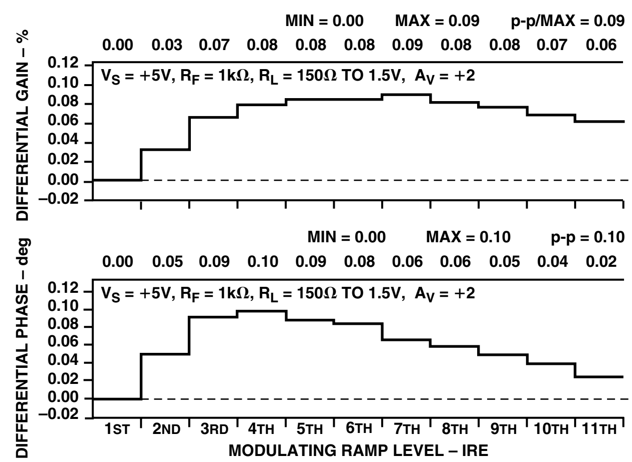



*Figure 8. Differential Gain and Phase, $V_S = +5$ V*

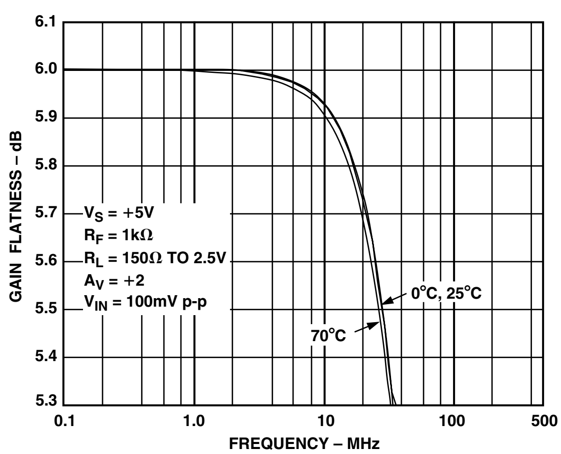



*Figure 6. 0.1 dB Flatness vs. Frequency Over Temperature; $V_S = +5$ V*

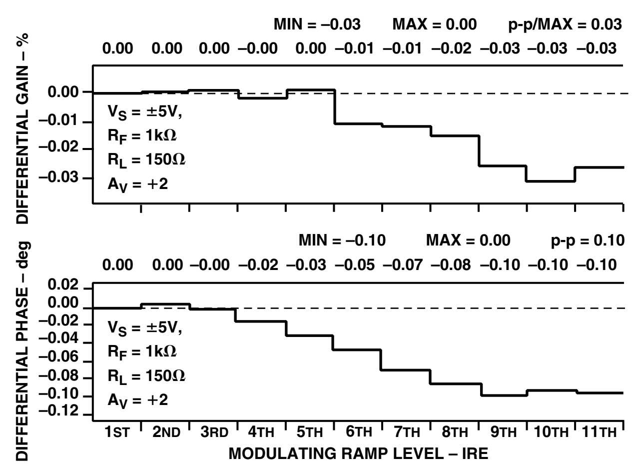



*Figure 9. Differential Gain and Phase, $V_S = \pm5$ V*

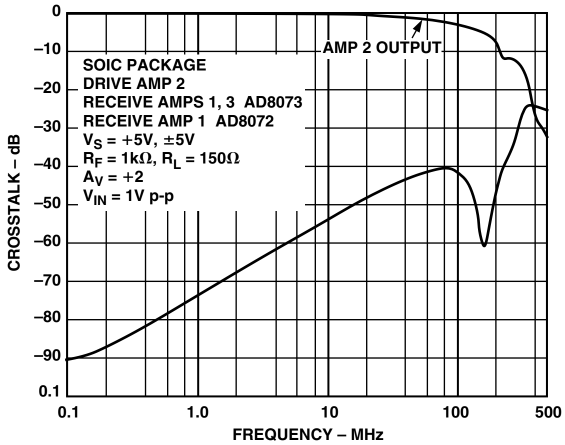



*Figure 10. Crosstalk vs. Frequency*

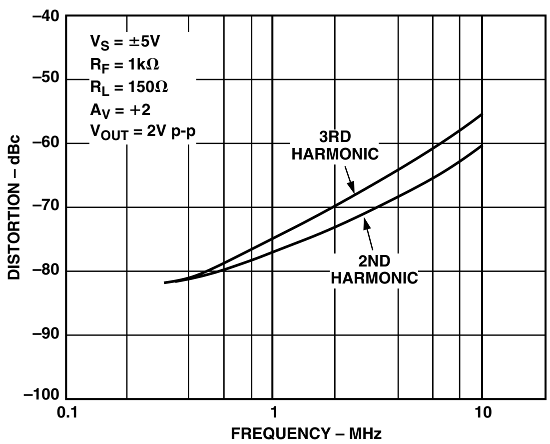



*Figure 11. Distortion vs. Frequency; $V_S = \pm 5$ V*

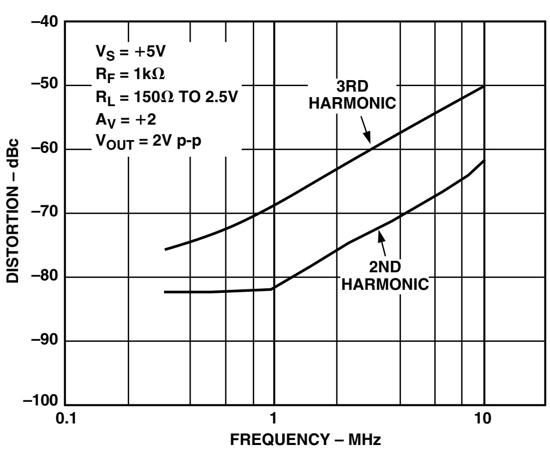



*Figure 12. Distortion vs. Frequency; $V_S = +5$ V*

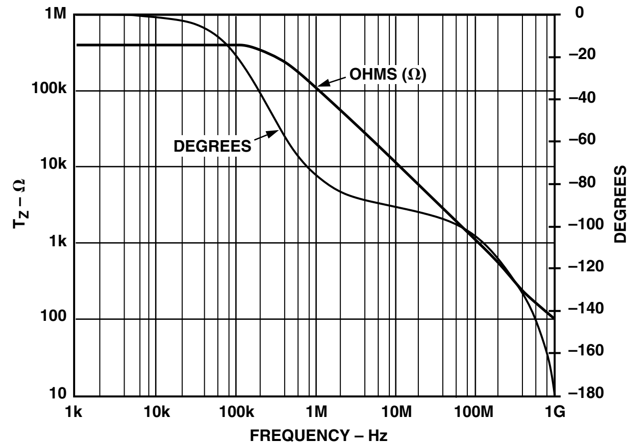



*Figure 13. Open-Loop Transimpedance vs. Frequency*

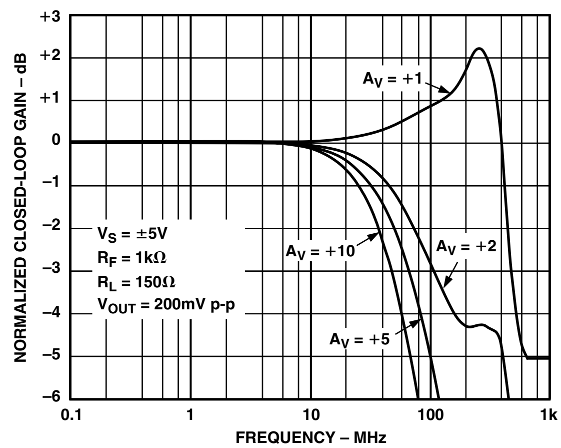



*Figure 14. Normalized Frequency Response; $V_S = \pm 5$ V*

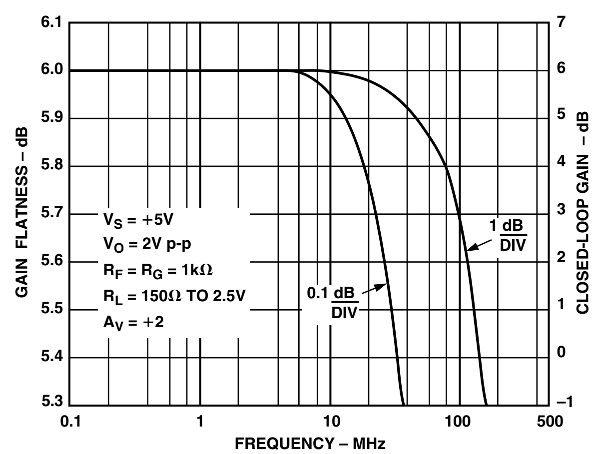



*Figure 15. Large Signal Frequency Response*

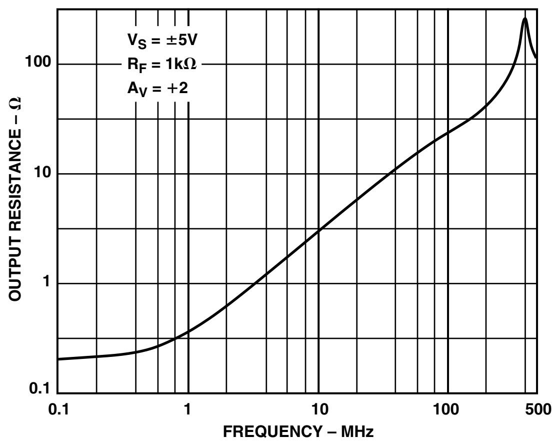



Figure 16. Output Resistance vs. Frequency; $V_S = \pm 5$ V

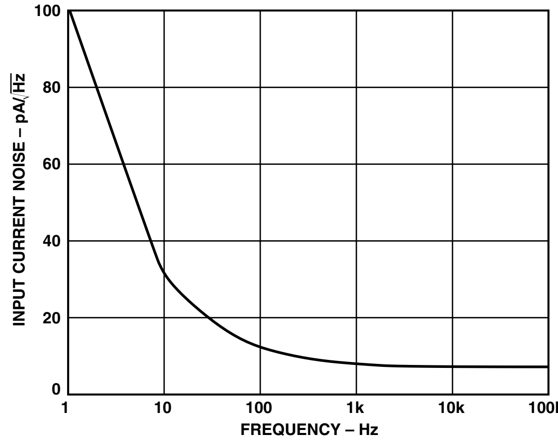



Figure 18. Noise vs. Frequency; $V_S = \pm 5$ V

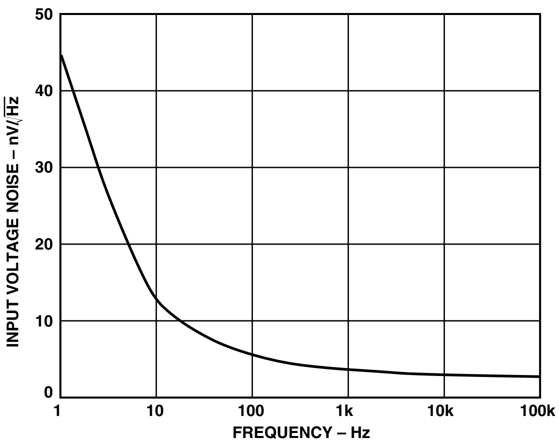



Figure 17. Noise vs. Frequency; $V_S = \pm 5$ V

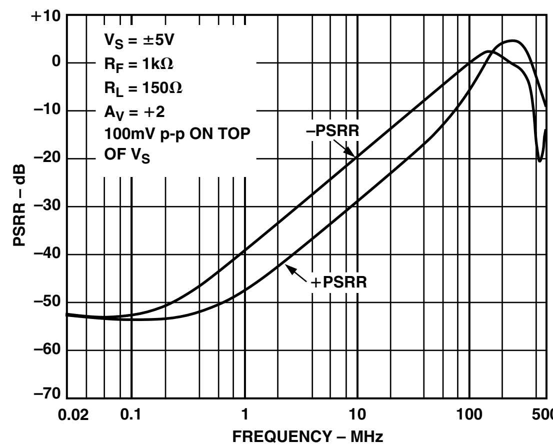



Figure 19. PSRR vs. Frequency

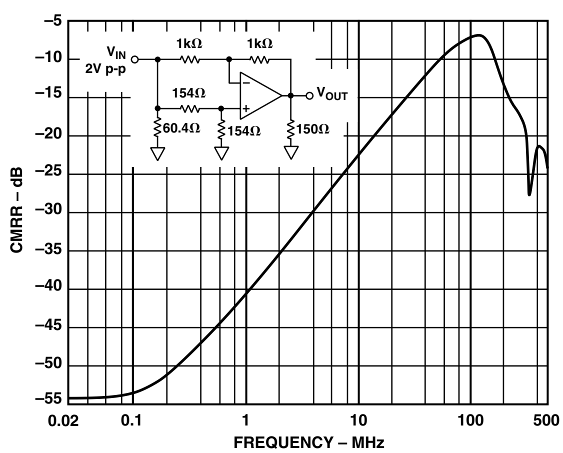



Figure 20. CMRR vs. Frequency; $V_S = \pm 5$ V

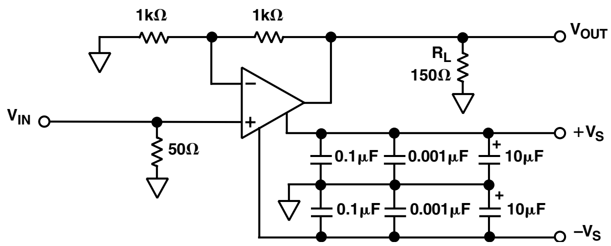


*Figure 21. Test Circuit; Gain = +2*

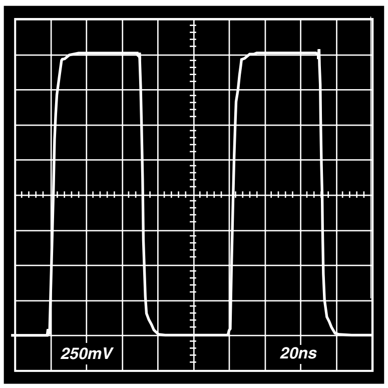


*Figure 22. 2 V Step Response; G = +2, $V_S$ = ±5 V*

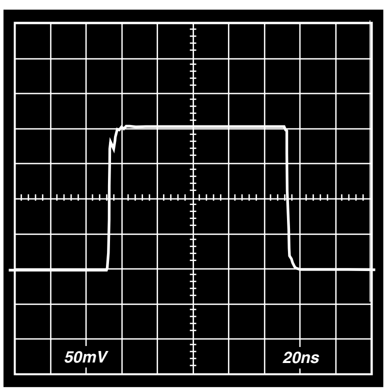


*Figure 23. 200 mV Step Response; G = +2, $V_S$ = ±5 V*

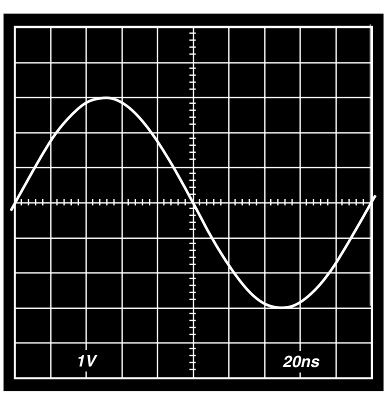


*Figure 24. Sine Response; G = +2, $V_S$ = ±5 V*

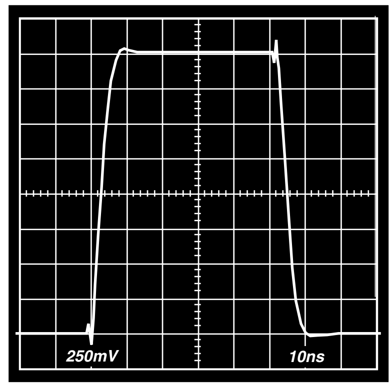


*Figure 25. 2 V Step Response; G = +2, $V_S$ = ±2.5 V*

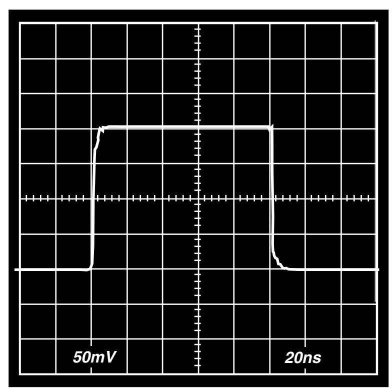


*Figure 26. 200 mV Step Response; G = +2, $V_S$ = ±2.5 V*

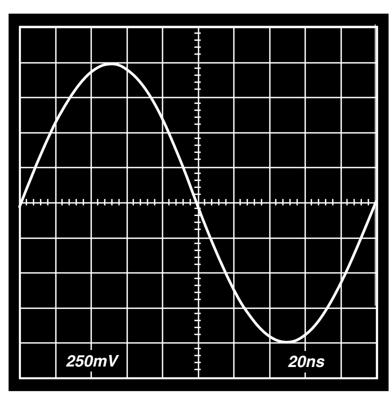


*Figure 27. Sine Response; G = +2, $V_S$ = ±2.5 V*

Note: $V_S$ = ±2.5 V operation is identical to $V_S$ = +5 V single supply operation.

## APPLICATIONS

### Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input range are exceeded. The amplifier must recover from this overdrive condition and resume normal operation. As shown in Figure 28, the AD8072 and AD8073 recover within 75 ns from positive overdrive and 30 ns from negative overdrive.

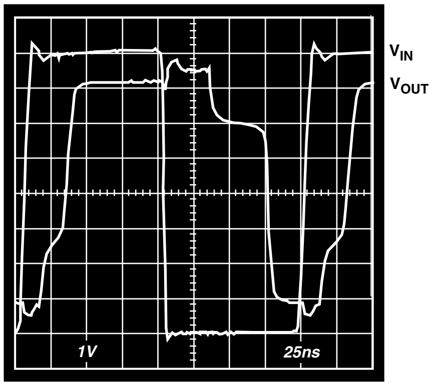



*Figure 28. Overload Recovery; $V_S$ = ±5 V, $V_{IN}$ = 8 V p-p, $R_F$ = 1 kΩ, $R_L$ = 150 Ω, G = +2*

### Bandwidth vs. Feedback Resistor Value

The closed-loop frequency response of a current feedback amplifier is a function of the feedback resistor. A smaller feedback resistor will produce a wider bandwidth response. However, if the feedback resistance becomes too small, the gain flatness can be affected. As a practical consideration, the minimum value of feedback resistance for the AD8072/AD8073 was found to be 649 Ω. For resistances below this value, the gain flatness will be affected and more significant lot to lot variations in device performance will be noticed. Figure 29 shows a plot of the frequency response of an AD8072/AD8073 at a gain of two with both feedback and gain resistors equal to 649 Ω.

On the other hand, the bandwidth of a current feedback amplifier can be decreased by increasing the feedback resistance. This can sometimes be useful where it is desired to reduce the noise bandwidth of a system. As a practical matter, the maximum value of feedback resistor was found to be 2 kΩ. Figure 29 shows the frequency response of an AD8072/AD8073 at a gain of two with both feedback and gain resistors equal to 2 kΩ.

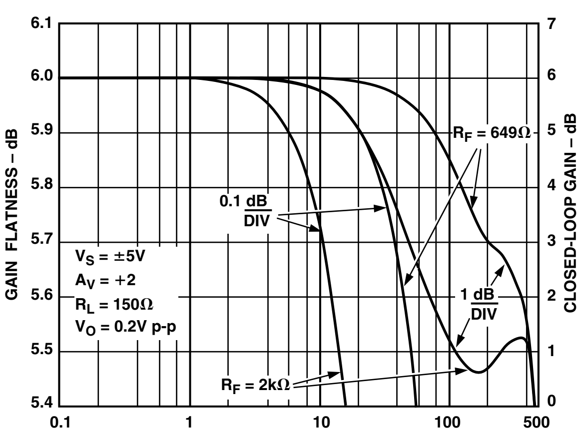



*Figure 29. Frequency Response vs. $R_F$*

### Capacitive Load Drive

When an op amp output drives a capacitive load, extra phase shift due to the pole formed by the op amp's output impedance and the capacitor can cause peaking or even oscillation. The top trace of Figure 30, $R_S$ = 0 Ω, shows the output of one of the amplifiers of the AD8072/AD8073 when driving a 50 pF capacitor as shown in the schematic of Figure 31.

The amount of peaking can be significantly reduced by adding a resistor in series with the capacitor. The lower trace of Figure 30 shows the same capacitor being driven with a 25 Ω resistor in series with it. In general, the resistor value will have to be experimentally determined, but from 10 Ω to 50 Ω is a practical range of values to experiment with for capacitive loads of up to a few hundred pF.

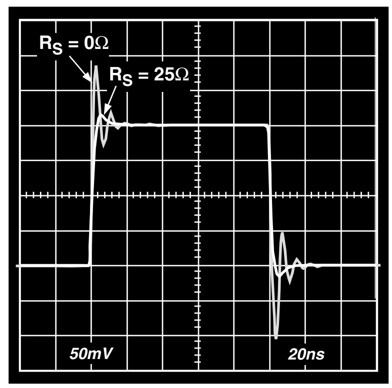



*Figure 30. Capacitive Low Drive*

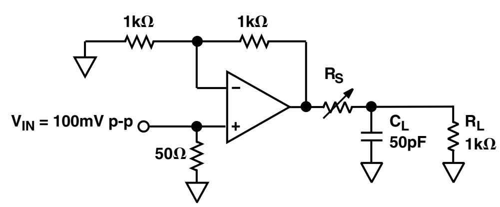



*Figure 31. Capacitive Load Drive Circuit*

### Crosstalk

Crosstalk between internal amplifiers may vary depending on which amplifier is being driven and how many amplifiers are being driven. This variation typically stems from pin location on the package and the internal layout of the IC itself. Table I illustrates the typical crosstalk results for a combination of conditions.

**Table I. AD8073JR Crosstalk Table (dB)**

| | AD8073JR | Receive Amplifier 1 | 2 | 3 |
|---|---|---|---|---|
| Drive Amplifier | 1 | X | –60 | –56 |
| | 2 | –60 | X | –60 |
| | 3 | –54 | –60 | X |
| | All Hostile | –53 | –55 | –54 |

**CONDITIONS**

$V_S = \pm 5$ V
$R_F = 1$ kΩ, $R_L = 150$ Ω
$A_V = +2$
$V_{OUT} = 2$ V p-p on Drive Amplifier

### Layout Considerations

The specified high speed performance of the AD8072 and AD8073 require careful attention to board layout and component selection. Proper RF design techniques and low parasitic component selection are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing. One end of the capacitor should be connected to the ground plane and the other within 1/8 inches of each power pin. An additional large (4.7 µF–10 µF) tantalum electrolytic capacitor should be connected in parallel, but not necessarily as close to the supply pins, to provide current for fast large-signal changes at the device's output.

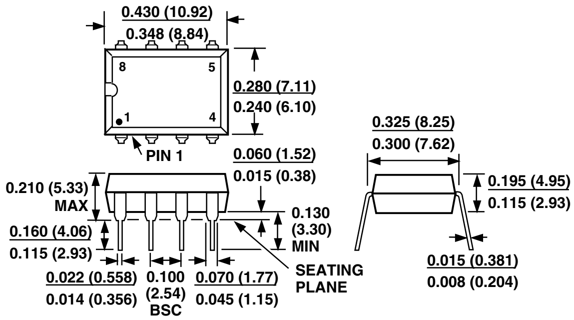
The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1 pF at the inverting input will affect high speed performance.

Stripline design techniques should be used for long signal traces (greater than about 1 inch). These should be designed with a characteristic impedance of 50 Ω or 75 Ω and be properly terminated at each end.

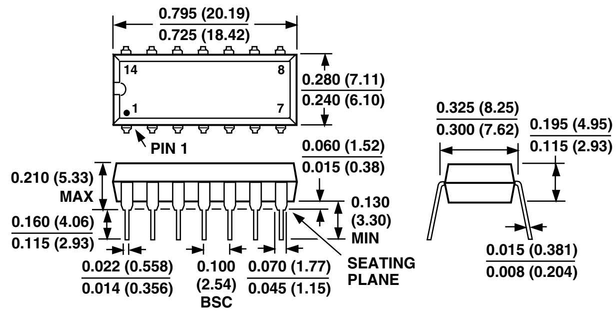
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

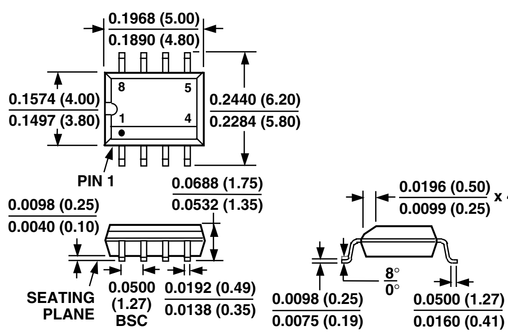
### 8-Lead Plastic DIP (N-8)



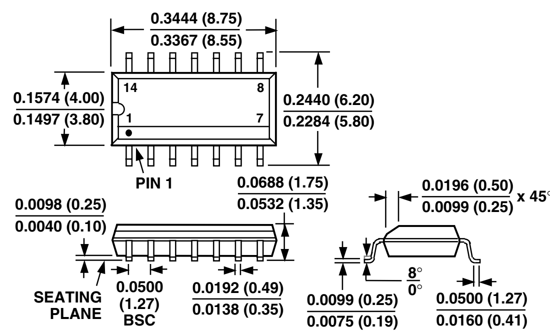

### 14-Lead Plastic DIP (N-14)



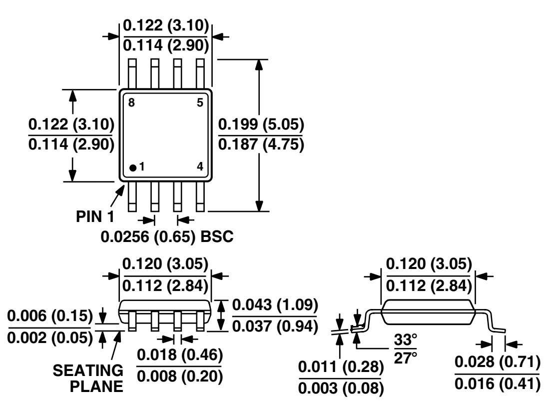

### 8-Lead Plastic SOIC (SO-8)




### 14-Lead SOIC (R-14)




### 8-Lead μSOIC (RM-8)

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