

Am9102/Am91L02 FAMILY

1024x1 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Low-Power Dissipation
100 mW typical; 260 mW maximum
- Standby operating mode reduces power 84%
18 mW typical; 42 mW maximum
- Input and output voltage levels identical to TTL
- High-Output Drive — Two full TTL loads guaranteed
- High Noise Immunity — 400 mV guaranteed
- Uniform Access Times
Switching characteristics are insensitive to data patterns, addressing patterns, and power supply variations
- Single 5-Volt Power Supply
10% tolerance for full temperature range devices
5% tolerance for commercial range devices
- High-Performance Plug-In Replacement for: Intel 2102, Signetics 2602, Intersil IM7552, Mostek 4102, T14033/4/5
- Available for operation over both commercial and military ranges
- 100% reliability assurance testing in accordance with MIL-STD-883
- Zero data hold and address hold times simplify timing requirements

FUNCTIONAL DESCRIPTION

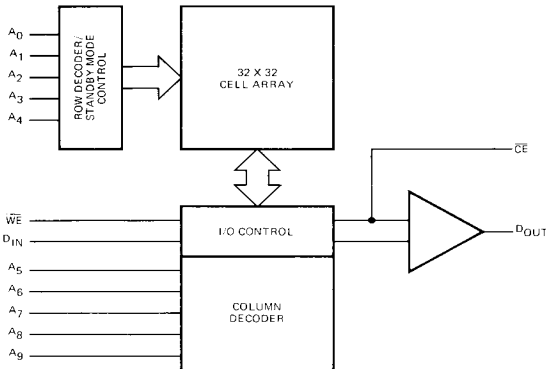
The Am9102 Family of 1024-bit static N-channel RAMs contains members with cycle times ranging from 650ns to 200ns. All the devices are organized as 1024 x 1, and all have a power-saving standby operating mode.

Each device has a chip enable input (CE) that controls a three-state output to make construction of large memory systems simple. Reading and writing are performed by enabling the chip and applying a LOW to write or a HIGH to read on the write enable input (WE). All inputs are directly TTL compatible with no external components required, and the output will drive two full TTL loads in both the HIGH and LOW states.

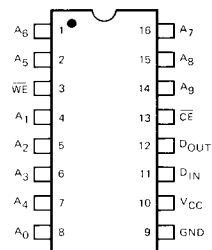
The devices operate from a single +5 volt power supply. The power dissipation of the devices can be reduced to about 16% of the normal operating power by lowering the voltage on the power supply pin. Data is guaranteed to be retained in the power-down condition.

All unit members in the family are available in plastic or hermetic DIPs for operation over the commercial temperature range and, except for the Am9102D/E, may also be purchased for operation over the military temperature range. All AC and DC parameters are guaranteed over the operating range.

BLOCK DIAGRAM



CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

AMBIENT TEMPERATURE	PACKAGE TYPE	POWER TYPE	ACCESS TIMES					
			650ns	500ns	400ns	300ns	250ns	200ns
0°C < T _A < +70°C	Molded DIP	Standard	AM9102PC	AM9102APC	AM9102BPC	AM9102CPC	AM9102DPC	Am9102EPC
		Low	AM91L02PC	AM91L02APC	AM91L02BPC	AM91L02CPC		
	Hermetic DIP	Standard	AM9102DC	AM9102ADC	AM9102BDC	AM9102CDC	AM9102DDC	Am9102EDC
		Low	AM91L02DC	AM91L02ADC	AM91L02BDC	AM91L02CDC	AM91L01CDC	
-55°C to +125°C	Hermetic DIP	Standard	AM9102DM	AM9102ADM	AM9102BDM	AM9102CDM	AM9101CDM	
		Low	AM91L02DM	AM91L02ADM	AM91L02BDM	AM91L02CDM	AM91L01CDM	
	Hermetic Flat Pack	Standard	AM9102FM	AM9102AFM	AM9102BFM			
		Low	AM91L02FM	AM91L02AFM	AM91L02BFM			

Am9102/Am91L02

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	-65°C to +150°C
Ambient Temperature Under Bias	-55°C to +125°C
V _{CC} With Respect to V _{SS} , Continuous	-0.5V to +7V
DC Voltage Applied to Outputs	-0.5V to +7V
DC Input Voltage	-0.5V to +7V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS over operating range

Am91L02PC, Am91L02DC T_A = 0°C to +70°C V_{CC} = +5.0V ±5%

Parameters	Description	Test Conditions	Am9102/A/B Am91L02/A/B		Am9102C Am9102D Am9102E		Units	
			Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = MIN., I _{OH} = -200μA	2.4		2.4		Volts	
V _{OL}	Output LOW Voltage	V _{CC} = MIN., I _{OL} = 3.2mA		0.4		0.4	Volts	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0	V _{CC}	2.0	V _{CC}	Volts	
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	-0.5	0.8	-0.5	0.8	Volts	
I _{LI}	Input Load Current	V _{CC} = MAX., V _{IN} = 0V to 5.25V		10		10	μA	
I _{CC1}	Power Supply Current	All inputs = V _{CC} Data out open V _{CC} = MAX.	T _A = 25°C	Am91L02	28		31	mA
				Am9102		45		
T _A = 0°C			Am91L02		30		33	
			Am9102		50		55	
I _{LO}	Output Leakage Current	V _{CS} = V _{IH}	V _{OUT} = V _{CC}			5.0	5.0	μA
			V _{OUT} = 0.4V			-10	-10	

Am91L02DM, FM T_A = -55°C to +125°C V_{CC} = +5.0V ±10%

Parameters	Description	Test Conditions	Am9102/A/B Am91L02/A/B		Am9102C Am91L02C		Units	
			Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	I _{OH} = -200μA	V _{CC} = 4.75V		2.4		2.4	Volts
			V _{CC} = 4.50V		2.2		2.2	
V _{OL}	Output LOW Voltage	V _{CC} = MIN., I _{OL} = 3.2mA		0.4		0.4	Volts	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0	V _{CC}	2.0	V _{CC}	Volts	
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	-0.5	0.8	-0.5	0.8	Volts	
I _{LI}	Input Load Current	V _{CC} = MAX., V _{IN} = 0V to 5.5V		10		10	μA	
I _{CC1}	Power Supply Current	All inputs = V _{CC} Data out open V _{CC} = MAX.	T _A = 25°C	Am91L02	28		31	mA
				Am9102		45		
T _A = -55°C			Am91L02		35		37	
			Am9102		55		60	
I _{LO}	Output Leakage Current	V _{CS} = V _{IH}	V _{OUT} = V _{CC}			10	10	μA
			V _{OUT} = 0.4V			-10	-10	

CAPACITANCE (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
C _{IN}	Input Capacitance, Any Input	V _{IN} = 0V, f = 1MHz		3.0	5.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V, f = 1MHz		4.0	6.0	pF

Am9102 FAMILY SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS

over operating temperature and voltage range

Load = 1 TTL gate and 100pF, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, $t_r = t_f = 10ns$. Output reference level 0.8V, 2.0V

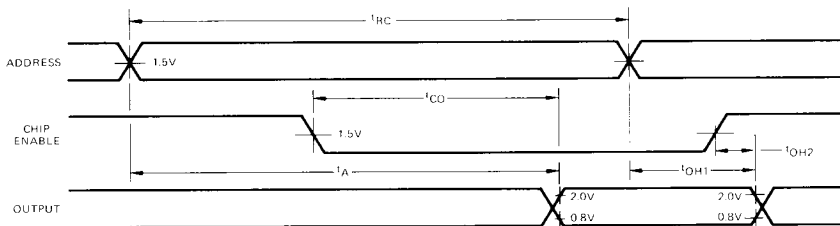
Read Cycle Characteristics		Am9102 Am91L02		Am9102A Am91L02A		Am9102B Am91L02B		Am9102C Am91L02C		Am9102D		Am9102E		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	650		500		400		300		250		200		ns
t_A	Access Time		650		500		400		300		250		200	ns
t_{CO}	\overline{CE} LOW to Output HIGH or LOW		200		175		150		125		100		80	ns
t_{OH1}	Previous Read Data Valid with Respect to Chip Select	50		50		50		50		40		30		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Select	0		0		0		0		0		0		ns

Write Cycle Requirements

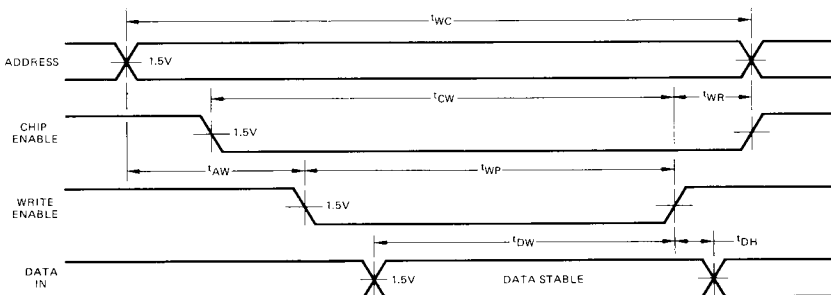
t_{WC}	Write Cycle Time	650		500		400		300		250		200		ns
t_{AW}	Address Set-Up Time	20		20		20		20		20		20		ns
t_{WP}	Write Pulse Width	200		175		150		125		100		80		ns
t_{WR}	Write Recovery Time (Address Hold Time)	0		0		0		0		0		0		ns
t_{DW}	Data Set-Up Time	175		150		125		100		75		60		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{CW}	Chip Enable Set-Up Time	200		175		150		125		100		85		ns

SWITCHING WAVEFORMS

READ CYCLE



WRITE CYCLE



POWER DOWN STANDBY OPERATION

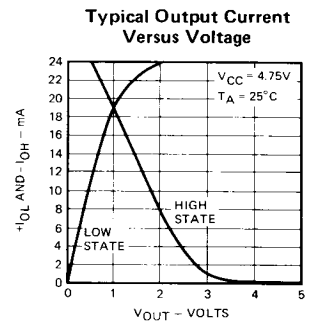
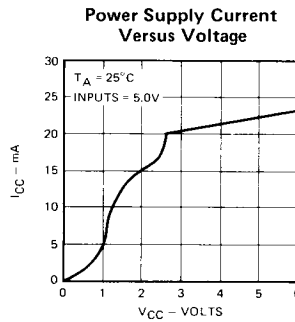
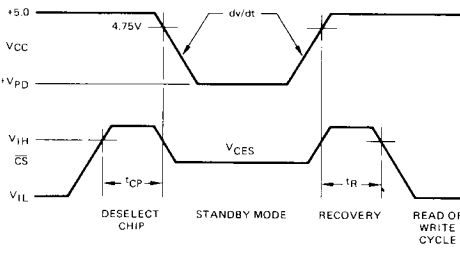
The Am9102 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated back-up power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power.

A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

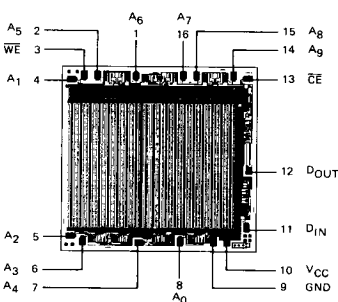
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be raised for the chip disable time (t_{CP}) prior to entering the standby mode, and should be held at V_{PD} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units	
V_{PD}	V_{CC} in Standby Mode		1.5				
I_{PD}	I_{CC} in Standby Mode	$T_A = 0^\circ C$ All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L02	10	23	mA
				Am9102	12	28	
			$V_{PD} = 2.0V$	Am91L02	12	28	
		Am9102	15	38			
		$T_A = -55^\circ C$ All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L02	10	26	
				Am9102	12	31	
$V_{PD} = 2.0V$	Am91L02		12	31			
Am9102	15	42					
dv/dt	Rate of Change of V_{CC}				1.0	V/ μs	
t_R	Standby Recovery Time		T_{RC}			ns	
T_{CP}	Chip Deselect Time		0			ns	
V_{CES}	\overline{CE} Bias in Standby		V_{PD}			Volts	

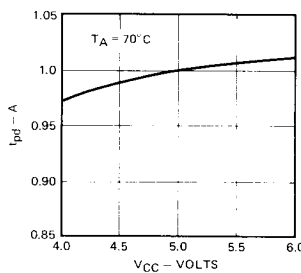


Metallization and Pad Layout

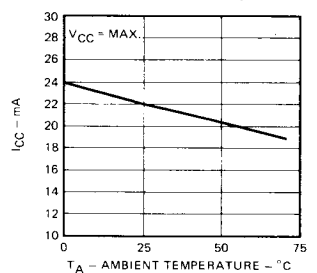


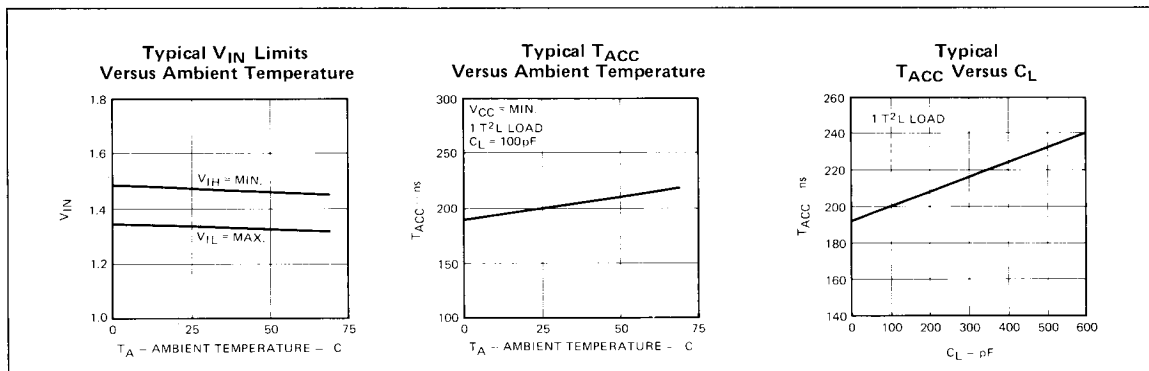
DIE SIZE 0.128'' X 0.128''

Access Time Versus V_{CC} Normalized to $V_{CC} = +5.0$ Volts



Typical Power Supply Current Versus Ambient Temperature





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DEFINITION OF TERMS

FUNCTIONAL TERMS

\overline{CE} Active LOW chip enable. Data can be read from or written into the memory only if \overline{CE} is LOW.

\overline{WE} Active LOW write enable. Data is written into the memory if \overline{WE} is LOW and read from the memory if \overline{WE} is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drains are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during

which the chip enable must be LOW prior to reading data on the output.

t_{OH1} Minimum Access Time. Minimum time which will elapse between change of address and any change on the data output.

t_{OH2} Minimum time which will elapse between a change on the chip enable and any change on the data output.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-Up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-Up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

