

# AN5766K

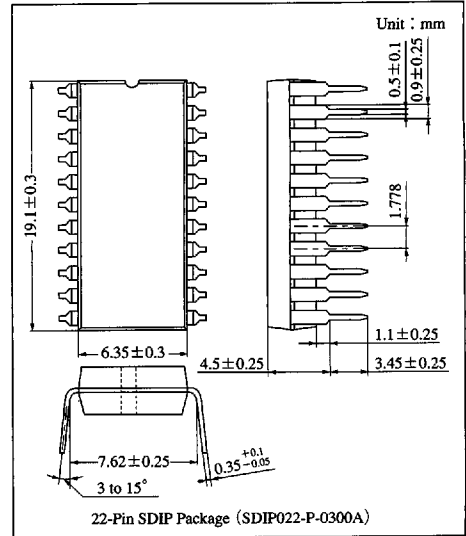
## Pin-Cushion Distortion-Correction IC for CRT Monitor

### Overview

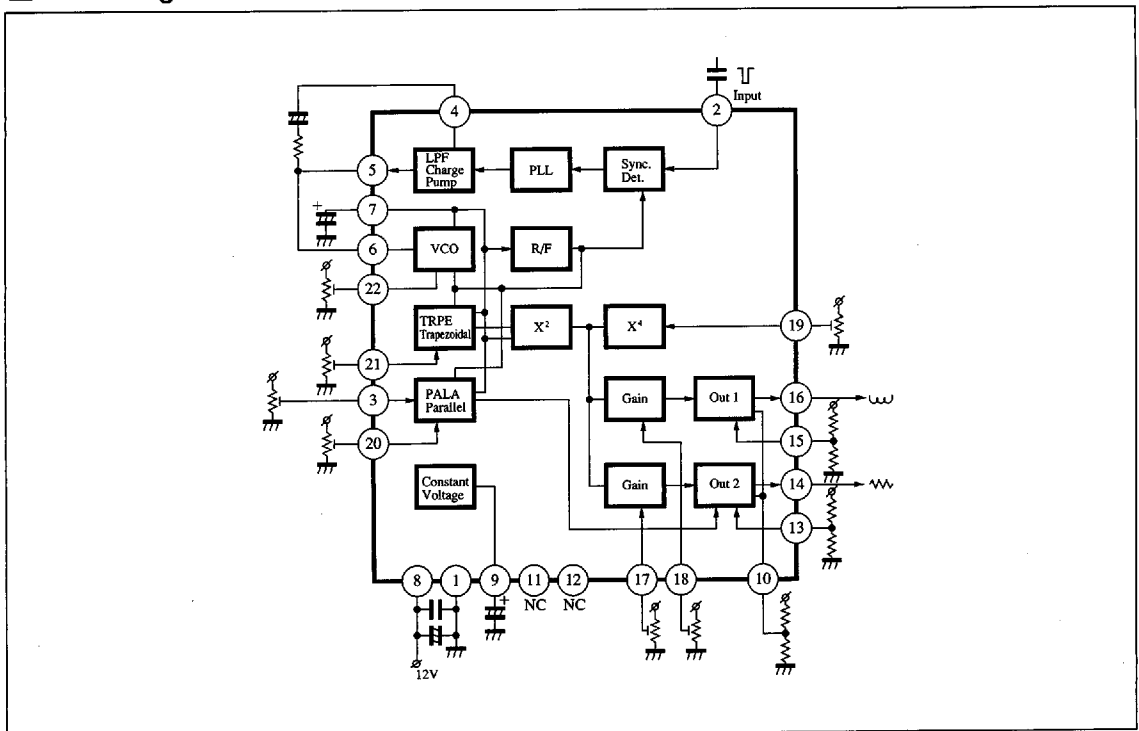
The AN5766K is a pin-cushion distortion-correction IC for CRT monitor. It can respond to 50 to 200Hz of vertical synchronous signal input. And also, it outputs E-W correction parabola-wave and saw-tooth wave.

### Features

- Vertical synchronous signal input range :  $f_v = 50$  to 200Hz (for either polarity)
- Correction circuits for EW Pin-cushion, EW corner, and trapezoidal correction circuits.
- Correction circuits for parallelograms and EW balance



### Block Diagram



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### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	13.4	V
Supply current	$I_{CC}$	20	mA
Power dissipation <sup>Note 2)</sup>	$P_D$	268	mW
Operating ambient temperature <sup>Note 1)</sup>	$T_{opr}$	-20 to +70	°C
Storage temperature <sup>Note 1)</sup>	$T_{stg}$	-55 to +150	°C

Note 1)  $T_a = 25^\circ\text{C}$  except operating ambient temperature and storage temperature.

Note 2) Allowable power dissipation of the package at  $T_a = 70^\circ\text{C}$ .

### Recommended Operating Range ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Range
Operating supply voltage range	$V_{CC}$	9.6V to 13.2V

### Electrical Characteristics ( $T_a = 25 \pm 2^\circ\text{C}$ )

Parameter	Symbol	Condition	min	typ	max	Unit
Circuit current	$I_{CC}$		8	11	15	mA
Circuit voltage	$V_{9-1}$	$V_{CC} = 12\text{V}$	5.3	6	6.7	V
	$V_{17-1}$		1.9	2.3	2.7	V
	$V_{18-1}$		1.9	2.3	2.7	V
	$V_{19-1}$		1.9	2.3	2.7	V
	$V_{20-1}$		1.9	2.3	2.7	V
	$V_{21-1}$		1.9	2.3	2.7	V
	$V_{22-1}$		1.9	2.3	2.7	V
Maximum parabola output amplitude	$e_{MAX}$	$V_{CC} = 12\text{V}$ At $V_{18} = 5\text{V}$	2.9	4.0	5.1	$V_{P-P}$
Center position adjustment quantity	$\Delta e_S$	$V_{CC} = 12\text{V}$ At $V_{22} = 5\text{V} \rightarrow 0\text{V}$ change	0.4	0.8	1.2	V
Trapezoidal correction quantity	$\Delta e_T$	$V_{22} = \text{open}$ , at $V_{21} = 5\text{V} \rightarrow 0\text{V}$ change	-2.7	-2.1	-1.5	V
Corner correction amount	$\Delta e_C$	$V_{21} = \text{open}$ , at $V_{19} = 5\text{V} \rightarrow 0\text{V}$ change	1.9	2.5	3.1	V
Side Pin-cushion amplitude (min.)	$e_{MIN}$	$V_{18} = 0\text{V}$ , $V_{15} = 8\text{V}$ at negative polarity parabola output	2.9	4.0	5.1	$V_{P-P}$
Side Pin-cushion amplitude (typ.)	$e_{TYP}$	At $V_{18} = 0\text{V}$ , $V_{15} = 8\text{V}$ $V_{18} = 2.5\text{V}$	—	0.3	0.5	$V_{P-P}$
Standard RAMP output	$e_{R-TYP}$	$V_{CC} = 12\text{V}$ At $V_{17}$ , $V_{20}$ , $V_{21} = \text{open}$	—	0.3	0.5	$V_{P-P}$
Parallelogram correction (max.)	$e_{P1}$	$V_{CC} = 12\text{V}$ At $V_{20} = 5\text{V}$	2.9	4.0	5.1	V
Parallelogram correction (min.)	$e_{P2}$	$V_{CC} = 12\text{V}$ At $V_{20} = 0\text{V}$	-3.8	-3.0	-2.2	V
Parallelogram amplitude (max.)	$e_{G1}$	$V_{CC} = 12\text{V}$ , $V_{20} = \text{open}$ $V_{17} = 5\text{V}$ , At $V_{13} = 4\text{V}$	3.1	4.2	5.3	V
Parallelogram amplitude (min.)	$e_{G2}$	$V_{CC} = 12\text{V}$ $V_{17} = 0\text{V}$ , At $V_{13} = 8\text{V}$	-5.3	-4.2	-3.1	V
Ramp output trapezoidal correction	$\Delta e_{RT}$	$V_{CC} = 12\text{V}$ , $V_{13} = 8\text{V}$ At $V_{21} = 5\text{V} \rightarrow 0\text{V}$ change	-3.8	-3.0	-2.2	V
PLL synchronous input (min.)	$f_{V1}$	VCO frequency in $V_{sync}$ 50Hz input	—	50	—	Hz
PLL synchronous input (max.)	$f_{V2}$	VCO frequency in $V_{sync}$ 200Hz input	—	200	—	Hz
Input bias voltage	$V_{2-1}$	Open voltage at $V_{CC} = 12\text{V}$	—	4.9	—	V

ICs for  
TV

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Panasonic

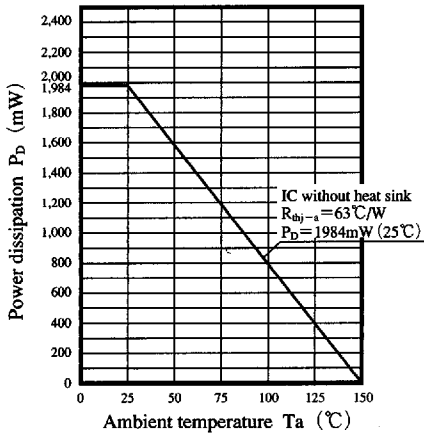
**Pin Descriptions**

Pin No.	Pin name	Pin No.	Pin name
1	GND	12	NC
2	Ver. sync. signal input	13	DC bias input for RAMP output
3	Cross-over distortion Adj. for RAMP output	14	RAMP output
4	LPF	15	DC Bias input for parabola output
5	Charge pump output	16	Parabola output
6	VCO control input	17	Parallelogram amplitude control
7	VCO capacitor	18	Side Pin-cushion amplitude control
8	V <sub>CC</sub> (+12V)	19	Corner correction control
9	Bias output (6V)	20	Parallelogram correction control
10	DC offset	21	Trapezoid correction control
11	NC	22	Center position correction control

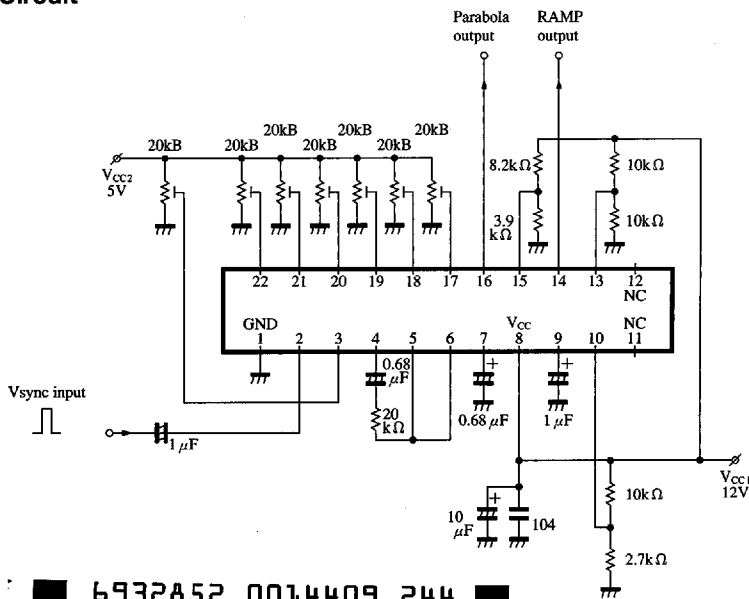
**Reference**

Power dissipation of package

$P_D - T_a$



**Application Circuit**



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