

## Fast-Charge IC

### Features

- ▶ Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- ▶ Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- ▶ Easily integrated into systems or used as a stand-alone charger
- ▶ Pre-charge qualification of temperature and voltage
- ▶ Configurable, direct LED outputs display battery and charge status
- ▶ Fast-charge termination by  $\Delta$  temperature/ $\Delta$  time, peak voltage detection,  $-\Delta V$ , maximum voltage, maximum temperature, and maximum time
- ▶ Optional top-off charge and pulsed current maintenance charging
- ▶ Logic-level controlled low-power mode ( $< 5\mu A$  standby current)

### General Description

The bq2004 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Integration of closed-loop current control circuitry allows the bq2004 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2004-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2004 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2004 may alternatively be used to gate an externally regulated charging current.

Fast charge may begin on application of the charging supply, replace-

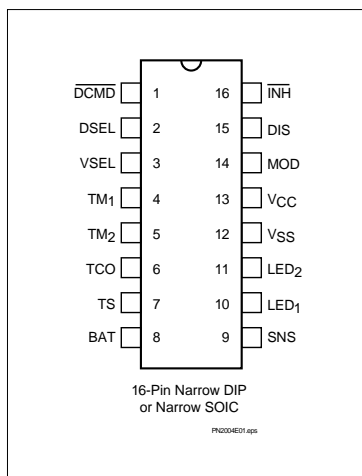
ment of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature time ( $\Delta T/\Delta t$ )
- Peak voltage detection (PVD)
- Negative delta voltage ( $-\Delta V$ )
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, optional top-off and pulsed current maintenance phases are available.

### Pin Connections



### Pin Names

|                 |                            |                         |                          |
|-----------------|----------------------------|-------------------------|--------------------------|
| DCMD            | Discharge command          | SNS                     | Sense resistor input     |
| DSEL            | Display select             | LED <sub>1</sub>        | Charge status output 1   |
| VSEL            | Voltage termination select | LED <sub>2</sub>        | Charge status output 2   |
| TM <sub>1</sub> | Timer mode select 1        | V <sub>SS</sub>         | System ground            |
| TM <sub>2</sub> | Timer mode select 2        | V <sub>CC</sub>         | 5.0V $\pm$ 10% power     |
| TCO             | Temperature cutoff         | MOD                     | Charge current control   |
| TS              | Temperature sense          | DIS                     | Discharge control output |
| BAT             | Battery voltage            | $\overline{\text{INH}}$ | Charge inhibit input     |

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## Pin Descriptions

### **$\overline{\text{DCMD}}$ Discharge-before-charge control input**

The  $\overline{\text{DCMD}}$  input controls the conditions that enable discharge-before-charge.  $\overline{\text{DCMD}}$  is pulled up internally. A negative-going pulse on  $\overline{\text{DCMD}}$  initiates a discharge to end-of-discharge voltage (EDV) on the BAT pin, followed by a new charge cycle start. Tying  $\overline{\text{DCMD}}$  to ground enables automatic discharge-before-charge on every new charge cycle start.

### **DSEL Display select input**

This three-state input configures the charge status display mode of the LED<sub>1</sub> and LED<sub>2</sub> outputs. See Table 2.

### **VSEL Voltage termination select input**

This three-state input controls the voltage-termination technique used by the bq2004. When high, PVD is active. When floating,  $-\Delta V$  is used. When pulled low, both PVD and  $-\Delta V$  are disabled.

### **TM<sub>1</sub>-TM<sub>2</sub> Timer mode inputs**

TM<sub>1</sub> and TM<sub>2</sub> are three-state inputs that configure the fast charge safety timer, voltage termination hold-off time, "top-off", and trickle charge control. See Table 1.

### **TCO Temperature cut-off threshold input**

Input to set maximum allowable battery temperature. If the potential between TS and SNS is less than the voltage at the TCO input, then fast charge or top-off charge is terminated.

### **TS Temperature sense input**

Input, referenced to SNS, for an external thermister monitoring battery temperature.

### **BAT Battery voltage input**

BAT is the battery voltage sense input, referenced to SNS. This is created by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

### **SNS Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor in the current path of the battery. SNS is the reference potential for both the TS and BAT pins. If SNS is connected to V<sub>SS</sub>, then MOD switches high at the beginning of charge and low at the end of charge.

### **LED<sub>1</sub>-LED<sub>2</sub> Charge status outputs**

Push-pull outputs indicating charging status. See Table 2.

### **V<sub>SS</sub> Ground**

### **V<sub>CC</sub> V<sub>CC</sub> supply input**

5.0V,  $\pm 10\%$  power input.

### **MOD Charge current control output**

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow.

### **DIS Discharge control output**

Push-pull output used to control an external transistor to discharge the battery before charging.

### **$\overline{\text{INH}}$ Charge inhibit input**

When low, the bq2004 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a new charge cycle is started.

## Functional Description

Figure 3 shows a block diagram and Figure 4 shows a state diagram of the bq2004.

### Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a two-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

**Note:** This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between VCC and VSS. See Figure 1. Both the BAT and TS inputs are referenced to SNS, so the signals used inside the IC are:

$$V_{BAT} - V_{SNS} = V_{CELL}$$

and

$$V_{TS} - V_{SNS} = V_{TEMP}$$

### Discharge-Before-Charge

The  $\overline{DCMD}$  input is used to command discharge-before-charge via the DIS output. Once activated, DIS becomes active (high) until  $V_{CELL}$  falls below  $V_{EDV}$ , at which time DIS goes low and a new fast charge cycle begins.

The  $\overline{DCMD}$  input is internally pulled up to  $V_{CC}$  (its inactive state). Leaving the input unconnected, therefore, results in disabling discharge-before-charge. A negative going pulse on  $\overline{DCMD}$  initiates discharge-before-charge at any time regardless of the current state of the bq2004. If  $\overline{DCMD}$  is tied to  $V_{SS}$ , discharge-before-charge will be the first step in all newly started charge cycles.

### Starting a Charge Cycle

A new charge cycle (see Figure 2) is started by:

1.  $V_{CC}$  rising above 4.5V
2.  $V_{CELL}$  falling through the maximum cell voltage,  $V_{MCV}$  where:

$$V_{MCV} = 0.8 * V_{CC} \pm 30mV$$

3. A transition on the  $\overline{INH}$  input from low to high.

If  $\overline{DCMD}$  is tied low, a discharge-before-charge is executed as the first step of the new charge cycle. Otherwise, pre-charge qualification testing is the first step.

The battery must be within the configured temperature and voltage limits before fast charging begins.

The valid battery voltage range is  $V_{EDV} < V_{BAT} < V_{MCV}$  where:

$$V_{EDV} = 0.4 * V_{CC} \pm 30mV$$

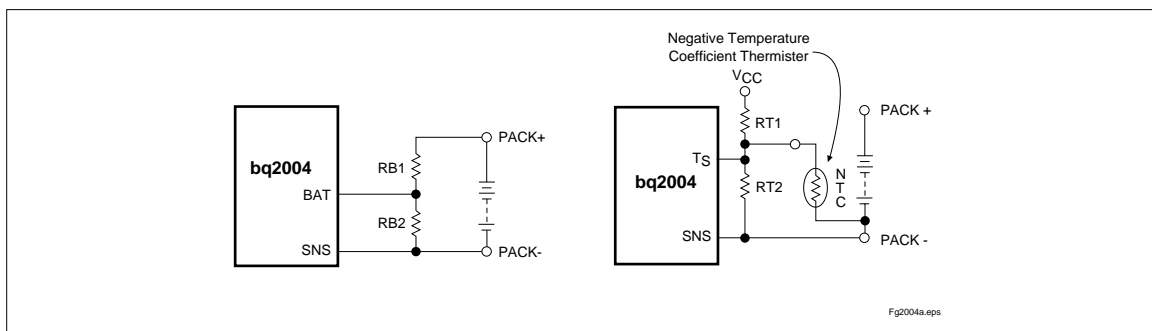
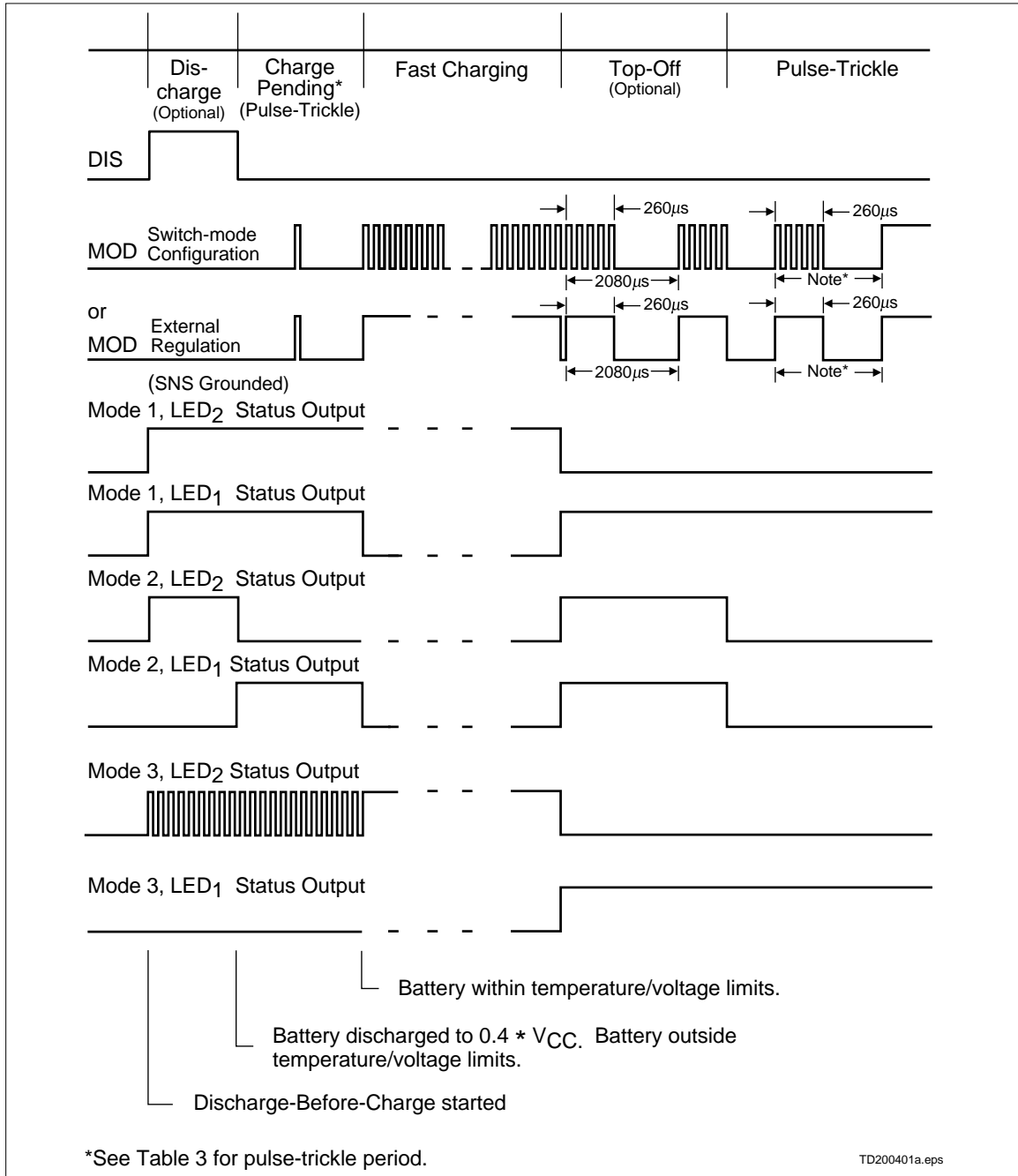


Figure 1. Voltage and Temperature Monitoring



**Figure 2. Charge Cycle Phases**

The valid temperature range is  $V_{HTF} < V_{TEMP} < V_{LTF}$ , where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/4 * V_{LTF}) + (3/4 * V_{TCO})] \pm 30mV$$

**Note:** The low temperature fault (LTF) threshold is not enforced if the IC is configured for PVD termination (VSEL = high).

$V_{TCO}$  is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between  $V_{CC}$  and ground. The allowed range is  $0.2$  to  $0.4 * V_{CC}$ .

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. The MOD output is modulated to provide the configured trickle charge rate in the charge pending state. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditions are outside of the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the six possible termination conditions:

- Delta temperature/delta time ( $\Delta T/\Delta t$ )
- Peak voltage detection (PVD)
- Negative delta voltage ( $-\Delta V$ )
- Maximum voltage
- Maximum temperature
- Maximum time

### PVD and -V Termination

The bq2004 samples the voltage at the BAT pin once every 34s. When  $-\Delta V$  termination is selected, if  $V_{CELL}$  is lower than any previously measured value by  $12mV \pm 4mV$  ( $6mV/cell$ ), fast charge is terminated. When PVD termination is selected, if  $V_{CELL}$  is lower than any previ-

| VSEL Input | Voltage Termination |
|------------|---------------------|
| Low        | Disabled            |
| Float      | $-\Delta V$         |
| High       | PVD                 |

ously measured value by  $6mV \pm 2mV$  ( $3mV/cell$ ), fast charge is terminated. The PVD and  $-\Delta V$  tests are valid in the range  $0.4 * V_{CC} < V_{CELL} < 0.8 * V_{CC}$ .

### Voltage Sampling

Each sample is an average of voltage measurements taken  $57\mu s$  apart. The IC takes 32 measurements in PVD mode and 16 measurements in  $-\Delta V$  mode. The resulting sample periods ( $9.17ms$  and  $18.18ms$ , respectively) filter out harmonics centered around  $55Hz$  and  $109Hz$ . This technique minimizes the effect of any AC line ripple that may feed through the power supply from either  $50Hz$  or  $60Hz$  AC sources. Tolerance on all timing is  $\pm 16\%$ .

### Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period,  $-\Delta V$  termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied.  $\Delta T/\Delta t$ , maximum voltage and maximum temperature terminations are not affected by the hold-off period.

### T/ t Termination

The bq2004 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If  $V_{TEMP}$  has fallen  $16mV \pm 4mV$  or more, fast charge is terminated. If VSEL = high, the  $\Delta T/\Delta t$  termination test is valid only when  $V_{TCO} < V_{TEMP} < V_{TCO} + 0.2 * V_{CC}$ . Otherwise the  $\Delta T/\Delta t$  termination test is valid only when  $V_{TCO} < V_{TEMP} < V_{LTF}$ .

### Temperature Sampling

Each sample is an average of 16 voltage measurements taken  $57\mu s$  apart. The resulting sample period ( $18.18ms$ ) filters out harmonics around  $55Hz$ . This technique minimizes the effect of any AC line ripple that may feed through the power supply from either  $50Hz$  or  $60Hz$  AC sources. Tolerance on all timing is  $\pm 16\%$ .

### Maximum Voltage, Temperature, and Time

Anytime  $V_{CELL}$  rises above  $V_{MCV}$ , the LEDs go off and charging ceases immediately. If  $V_{CELL}$  then falls back below  $V_{MCV}$  before  $t_{MCV} = 1.5s \pm 0.5s$ , the chip transitions to the Charge Complete state (maximum voltage termination). If  $V_{CELL}$  remains above  $V_{MCV}$  at the expiration of  $t_{MCV}$ , the bq2004 transitions to the Battery Absent state (battery removal). See Figure 4.

Maximum temperature termination occurs anytime  $V_{TEMP}$  falls below the temperature cutoff threshold  $V_{TCO}$ . Unless PVD termination is enabled (VSEL = high), charge will also be terminated if  $V_{TEMP}$  rises above the low temperature fault threshold,  $V_{LTF}$ , after fast charge begins. The  $V_{LTF}$  threshold is not enforced when the IC is configured for PVD termination.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of  $C/4$ ,  $C/2$ ,  $1C$ , and  $2C$ . Maximum time-out termination is enforced on the fast-charge phase, then reset,

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and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

### Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time equal to the fast-charge safety time (See Table 1.) During top-off, the MOD pin is enabled at a duty cycle of 260 $\mu$ s active for every 1820 $\mu$ s inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

### Pulse-Trickle Charge

Pulse-trickle charging follows the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger. The configured pulse-trickle rate is also applied in the charge pending state to raise the voltage of an over-discharged battery up to the minimum required before fast charge can begin.

In the pulse-trickle mode, MOD is active for 260 $\mu$ s of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/64 when

top-off is enabled and C/32 when top-off is disabled. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V<sub>SS</sub>.

### Charge Status Indication

Charge status is indicated by the LED<sub>1</sub> and LED<sub>2</sub> outputs. The state of these outputs in the various charge cycle phases is given in Table 2 and illustrated in Figure 2.

In all cases, if V<sub>CELL</sub> exceeds the voltage at the MCV pin, both LED<sub>1</sub> and LED<sub>2</sub> outputs are held low regardless of other conditions. Both can be used to directly drive an LED.

### Charge Current Control

The bq2004 controls charge current through the MOD output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch mode configuration, the nominal regulated current is:

$$I_{REG} = 0.225V/R_{SNS}$$

Charge current is monitored at the SNS input by the voltage drop across a sense resistor, R<sub>SNS</sub>, between the low side of the battery pack and ground. R<sub>SNS</sub> is sized to provide the desired fast charge current.

**Table 1. Fast-Charge Safety Time/Hold-Off/Top-Off Table**

| Corresponding Fast-Charge Rate | TM1   | TM2   | Typical Fast-Charge Safety Time (minutes) | Typical PVD, $\pm\Delta V$ Hold-Off Time (seconds) | Top-Off Rate | Pulse-Trickle Rate | Pulse-Trickle Period (Hz) |
|--------------------------------|-------|-------|---|--|--------------|--------------------|---------------------------|
| C/4                            | Low   | Low   | 360                                       | 137  | Disabled     | Disabled           | Disabled                  |
| C/2                            | Float | Low   | 180                                       | 820  | Disabled     | C/32               | 240                       |
| 1C                             | High  | Low   | 90  | 410  | Disabled     | C/32               | 120                       |
| 2C                             | Low   | Float | 45  | 200  | Disabled     | C/32               | 60                        |
| 4C                             | Float | Float | 23  | 100  | Disabled     | C/32               | 30                        |
| C/2                            | High  | Float | 180                                       | 820  | C/16         | C/64               | 120                       |
| 1C                             | Low   | High  | 90  | 410  | C/8          | C/64               | 60                        |
| 2C                             | Float | High  | 45  | 200  | C/4          | C/64               | 30                        |
| 4C                             | High  | High  | 23  | 100  | C/2          | C/64               | 15                        |

**Note:** Typical conditions = 25°C, V<sub>CC</sub> = 5.0V.

If the voltage at the SNS pin is less than  $V_{SNSLO}$ , the MOD output is switched high to pass charge current to the battery.

$$V_{SNSLO} = 0.04 * V_{CC} \pm 25mV$$

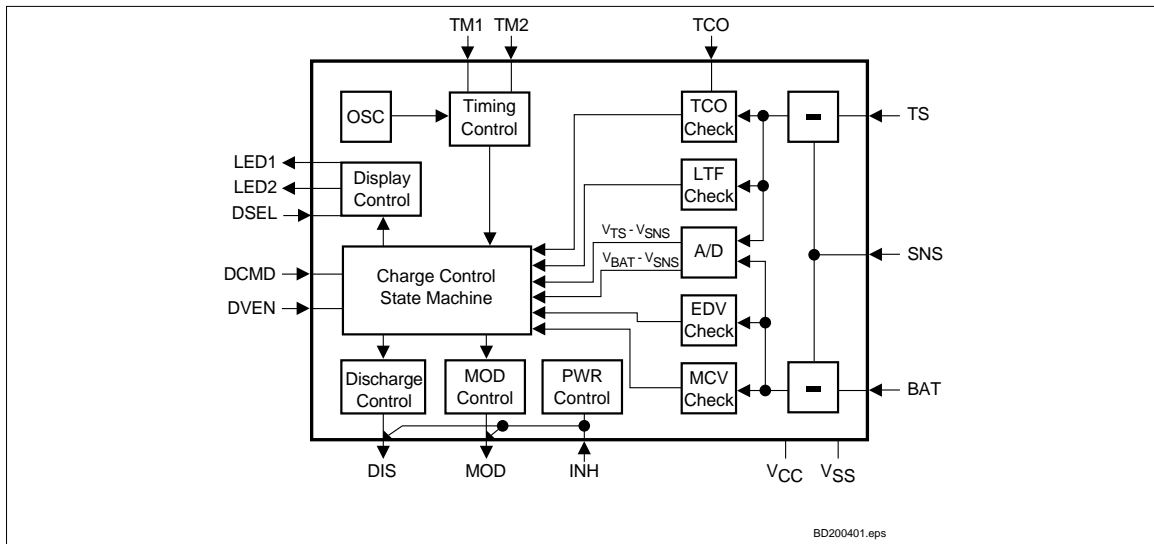
$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When the SNS voltage is greater than  $V_{SNSHI}$ , the MOD output is switched low—shutting off charging current to the battery.

When used to gate an externally regulated current source, the SNS pin is connected to  $V_{SS}$ , and no sense resistor is required.

**Table 2. bq2004 LED Status Display Options**

| Mode 1          | Charge Status  | LED <sub>1</sub> | LED <sub>2</sub>      |
|-----------------|--|------------------|-----------------------|
| DSEL = $V_{SS}$ | Battery absent   | Low              | Low                   |
|                 | Fast charge pending or discharge-before-charge in progress | High             | High                  |
|                 | Fast charge in progress                                    | Low              | High                  |
|                 | Charge complete, top-off, and/or trickle                   | High             | Low                   |
| Mode 2          | Charge Status  | LED <sub>1</sub> | LED <sub>2</sub>      |
| DSEL = Floating | Battery absent, fast charge in progress or complete        | Low              | Low                   |
|                 | Fast charge pending  | High             | Low                   |
|                 | Discharge in progress                                      | Low              | High                  |
|                 | Top-off in progress  | High             | High                  |
| Mode 3          | Charge Status  | LED <sub>1</sub> | LED <sub>2</sub>      |
| DSEL = $V_{CC}$ | Battery absent   | Low              | Low                   |
|                 | Fast charge pending or discharge-before-charge in progress | Low              | 1/8s high<br>1/8s low |
|                 | Fast charge in progress                                    | Low              | High                  |
|                 | Fast charge complete, top-off, and/or trickle              | High             | Low                   |



**Figure 3. Block Diagram**

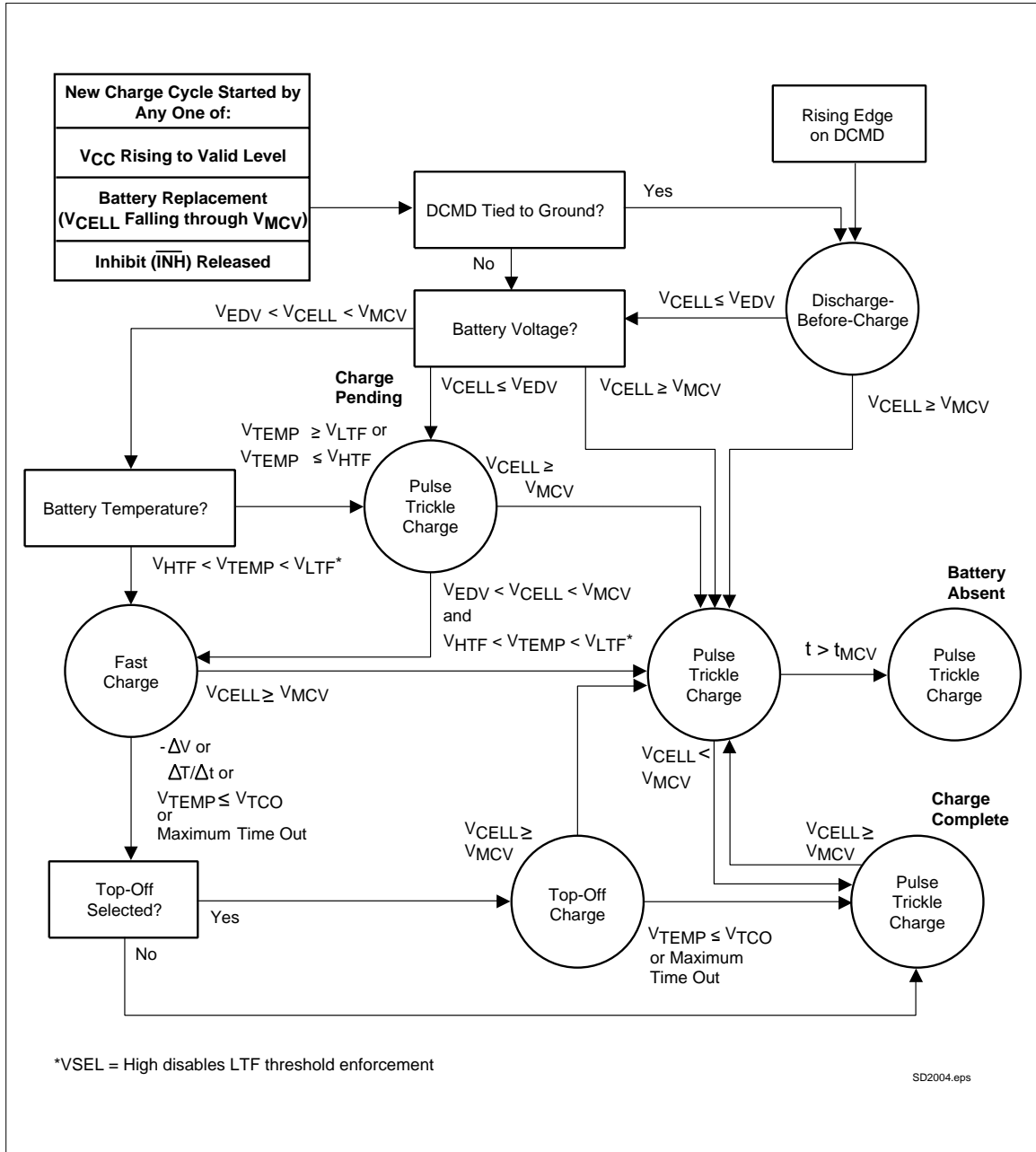


Figure 4. State Diagram



## Absolute Maximum Ratings

| Symbol              | Parameter   | Minimum | Maximum | Unit | Notes       |
|---------------------|---|---------|---------|------|-------------|
| V <sub>CC</sub>     | V <sub>CC</sub> relative to V <sub>SS</sub>   | -0.3    | +7.0    | V    |             |
| V <sub>T</sub>      | DC voltage applied on any pin excluding V <sub>CC</sub> relative to V <sub>SS</sub> | -0.3    | +7.0    | V    |             |
| T <sub>OPR</sub>    | Operating ambient temperature   | -20     | +70     | °C   | Commercial  |
| T <sub>STG</sub>    | Storage temperature   | -55     | +125    | °C   |             |
| T <sub>SOLDER</sub> | Soldering temperature   | -       | +260    | °C   | 10 sec max. |
| T <sub>BIAS</sub>   | Temperature under bias  | -40     | +85     | °C   |             |

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## DC Thresholds (T<sub>A</sub> = T<sub>OPR</sub>; V<sub>CC</sub> ±10%)

| Symbol             | Parameter                                    | Rating  | Tolerance | Unit | Notes  |
|--------------------|--|---|-----------|------|--|
| V <sub>SNSHI</sub> | High threshold at SNS resulting in MOD = Low | 0.05 * V <sub>CC</sub>                                | ±0.025    | V    |  |
| V <sub>SNSLO</sub> | Low threshold at SNS resulting in MOD = High | 0.04 * V <sub>CC</sub>                                | ±0.025    | V    |  |
| V <sub>LTF</sub>   | Low-temperature fault                        | 0.4 * V <sub>CC</sub>                                 | ±0.030    | V    | V <sub>TEMP</sub> ≥ V <sub>LTF</sub> inhibits/terminates charge  |
| V <sub>HTF</sub>   | High-temperature fault                       | (1/4 * V <sub>LTF</sub> ) + (3/4 * V <sub>TCO</sub> ) | ±0.030    | V    | V <sub>TEMP</sub> ≤ V <sub>HTF</sub> inhibits charge             |
| V <sub>EDV</sub>   | End-of-discharge voltage                     | 0.4 * V <sub>CC</sub>                                 | ±0.030    | V    | V <sub>CELL</sub> < V <sub>EDV</sub> inhibits fast charge        |
| V <sub>MVCV</sub>  | Maximum cell voltage                         | 0.8 * V <sub>CC</sub>                                 | ±0.030    | V    | V <sub>CELL</sub> > V <sub>MVCV</sub> inhibits/terminates charge |
| V <sub>THERM</sub> | TS input change for ΔT/Δt detection          | -16   | ±4        | mV   | V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C                      |
| -ΔV                | BAT input change for -ΔV detection           | -12   | ±4        | mV   | V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C                      |
| PVD                | BAT input change for PVD detection           | -6  | ±2        | mV   | V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C                      |

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## Recommended DC Operating Conditions (T<sub>A</sub> = T<sub>OPR</sub>)

| Symbol            | Condition   | Minimum               | Typical | Maximum               | Unit | Notes   |
|-------------------|---|-----------------------|---------|-----------------------|------|---|
| V <sub>CC</sub>   | Supply voltage  | 4.5                   | 5.0     | 5.5                   | V    |   |
| V <sub>BAT</sub>  | Battery input   | 0                     | -       | V <sub>CC</sub>       | V    |   |
| V <sub>CELL</sub> | BAT voltage potential                                 | 0                     | -       | V <sub>CC</sub>       | V    | V <sub>BAT</sub> - V <sub>SNS</sub>   |
| V <sub>TS</sub>   | Thermistor input                                      | 0                     | -       | V <sub>CC</sub>       | V    |   |
| V <sub>TEMP</sub> | TS voltage potential                                  | 0                     | -       | V <sub>CC</sub>       | V    | V <sub>TS</sub> - V <sub>SNS</sub>  |
| V <sub>TCO</sub>  | Temperature cutoff                                    | 0.2 * V <sub>CC</sub> | -       | 0.4 * V <sub>CC</sub> | V    | Valid ΔT/Δt range   |
| V <sub>IH</sub>   | Logic input high                                      | 2.0                   | -       | -                     | V    | DCMD, $\overline{\text{INH}}$   |
|                   | Logic input high                                      | V <sub>CC</sub> - 0.3 | -       | -                     | V    | TM <sub>1</sub> , TM <sub>2</sub> , DSEL, VSEL  |
| V <sub>IL</sub>   | Logic input low                                       | -                     | -       | 0.8                   | V    | DCMD, $\overline{\text{INH}}$   |
|                   | Logic input low                                       | -                     | -       | 0.3                   | V    | TM <sub>1</sub> , TM <sub>2</sub> , DSEL, VSEL  |
| V <sub>OH</sub>   | Logic output high                                     | V <sub>CC</sub> - 0.8 | -       | -                     | V    | DIS, MOD, LED <sub>1</sub> , LED <sub>2</sub> ,<br>I <sub>OH</sub> ≤ -10mA  |
| V <sub>OL</sub>   | Logic output low                                      | -                     | -       | 0.8                   | V    | DIS, MOD, LED <sub>1</sub> , LED <sub>2</sub> ,<br>I <sub>OL</sub> ≤ 10mA   |
| I <sub>CC</sub>   | Supply current  | -                     | 1       | 3                     | mA   | Outputs unloaded  |
| I <sub>SB</sub>   | Standby current                                       | -                     | -       | 1                     | μA   | $\overline{\text{INH}} = V_{\text{IL}}$   |
| I <sub>OH</sub>   | DIS, LED <sub>1</sub> , LED <sub>2</sub> , MOD source | -10                   | -       | -                     | mA   | @V <sub>OH</sub> = V <sub>CC</sub> - 0.8V   |
| I <sub>OL</sub>   | DIS, LED <sub>1</sub> , LED <sub>2</sub> , MOD sink   | 10                    | -       | -                     | mA   | @V <sub>OL</sub> = V <sub>SS</sub> + 0.8V   |
| I <sub>L</sub>    | Input leakage   | -                     | -       | ±1                    | μA   | $\overline{\text{INH}}$ , BAT, V = V <sub>SS</sub> to V <sub>CC</sub>   |
|                   | Input leakage   | 50                    | -       | 400                   | μA   | DCMD, V = V <sub>SS</sub> to V <sub>CC</sub>  |
| I <sub>IL</sub>   | Logic input low source                                | -                     | -       | 70                    | μA   | TM <sub>1</sub> , TM <sub>2</sub> , DSEL, VSEL,<br>V = V <sub>SS</sub> to V <sub>SS</sub> + 0.3V                        |
| I <sub>IH</sub>   | Logic input high source                               | -70                   | -       | -                     | μA   | TM <sub>1</sub> , TM <sub>2</sub> , DSEL, VSEL,<br>V = V <sub>CC</sub> - 0.3V to V <sub>CC</sub>                        |
| I <sub>IZ</sub>   | Tri-state   | -2                    | -       | 2                     | μA   | TM <sub>1</sub> , TM <sub>2</sub> , DSEL, and VSEL<br>should be left disconnected<br>(floating) for Z logic input state |

**Note:** All voltages relative to V<sub>SS</sub> except as noted.

## Impedance

| Symbol           | Parameter               | Minimum | Typical | Maximum | Unit |
|------------------|-------------------------|---------|---------|---------|------|
| R <sub>BAT</sub> | Battery input impedance | 50      | -       | -       | MΩ   |
| R <sub>TS</sub>  | TS input impedance      | 50      | -       | -       | MΩ   |
| R <sub>TCO</sub> | TCO input impedance     | 50      | -       | -       | MΩ   |
| R <sub>SNS</sub> | SNS input impedance     | 50      | -       | -       | MΩ   |

## Timing (T<sub>A</sub> = 0 to +70°C; V<sub>CC</sub> ±10%)

| Symbol           | Parameter  | Minimum | Typical | Maximum | Unit | Notes   |
|------------------|--|---------|---------|---------|------|---|
| t <sub>PW</sub>  | Pulse width for $\overline{\text{DCMD}}$ and $\overline{\text{INH}}$ pulse command | 1       | -       | -       | μs   | Pulse start for charge or discharge before charge               |
| d <sub>FCV</sub> | Time base variation  | -16     | -       | 16      | %    | V <sub>CC</sub> = 4.75V to 5.25V                                |
| f <sub>REG</sub> | MOD output regulation frequency  | -       | -       | 300     | kHz  |   |
| t <sub>MCV</sub> | Maximum voltage termination time limit   | 1       | -       | 2       | s    | Time limit to distinguish battery removed from charge complete. |

**Note:** Typical is at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0V.

# bq2004

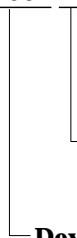
## Data Sheet Revision History

| Change No. | Page No. | Description   | Nature of Change  |
|------------|----------|---|---|
| 1          | 10       | Standby current ISB                                   | Was 5 A max; is 1 A max   |
| 2          | 9        | V <sub>BSNSLO</sub> Rating                            | Was: V <sub>SNSHI</sub> - (0.01 * V <sub>CC</sub> )<br>Is: 0.04 * V <sub>CC</sub>                                       |
| 2          | 7        | Correction in Peak Voltage Detect Termination section | Was VCELL; is VBAT  |
| 2          | 3        | Added block diagram                                   | Diagram insertion   |
| 2          | 7        | Added VSEL/termination table                          | Table insertion   |
| 2          | 8        | Added values to Table 3                               | Top-off rate values   |
| 3          | 7        | VSEL/Termination                                      | Low, High changed   |
| 4          | All      | Revised and expanded format of this data sheet        | Clarification   |
| 5          | 9        | Corrected V <sub>HTF</sub> rating                     | Was: (1/3 * V <sub>LTF</sub> ) + (2/3 * V <sub>TCO</sub> )<br>Is: (1/4 * V <sub>LTF</sub> ) + (3/4 * V <sub>TCO</sub> ) |
| 6          | 9        | T <sub>OPR</sub>                                      | Deleted industrial temperature range  |
| 7          | 9        | Corrected V <sub>HTF</sub> DC threshold               | Was: (1/4 * V <sub>LTF</sub> ) + (2/3 * V <sub>TCO</sub> )<br>Is: (1/4 * V <sub>LTF</sub> ) + (3/4 * V <sub>TCO</sub> ) |
| 8          | 9        | Corrected V <sub>NSLO</sub> tolerance                 | Was: ±0.010<br>Is: ±0.025   |

**Notes:** Change 1 = Apr. 1994 B "Final" changes from Dec. 1993 A "Preliminary."  
Change 2 = Sept. 1996 C changes from Apr. 1994 B.  
Change 3 = April 1997 C changes from Sept. 1996 C.  
Change 4 = Oct. 1997 D changes from April 1997 C.  
Change 5 = Jan. 1998 E changes from Oct. 1997 D.  
Change 6 = June 1999 F changes from Jan. 1998 E.  
Change 7 = Feb. 2001 G changes from June 1999 F.  
Change 8 = Apr. 2005 H changes from Feb. 2001 G.

## Ordering Information

**bq2004**



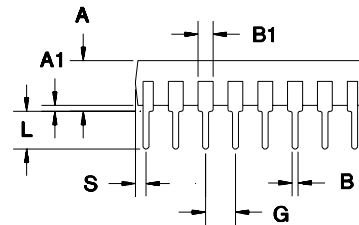
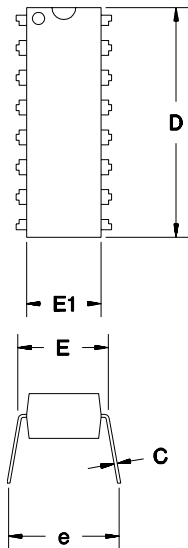
**Package Option:**

PN = 16-pin narrow plastic DIP  
SN = 16-pin narrow SOIC

**Device:**

bq2004 Fast-Charge IC

16-Pin DIP Narrow (PN)

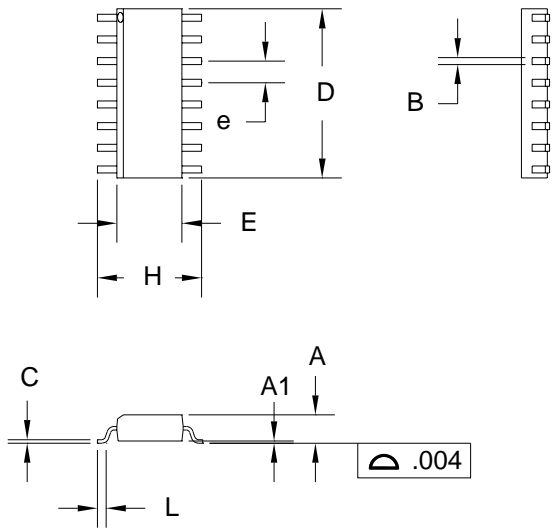


16-Pin PN (0.300" DIP)

| Dimension | Inches |       | Millimeters |       |
|-----------|--------|-------|-------------|-------|
|           | Min.   | Max.  | Min.        | Max.  |
| A         | 0.160  | 0.180 | 4.06        | 4.57  |
| A1        | 0.015  | 0.040 | 0.38        | 1.02  |
| B         | 0.015  | 0.022 | 0.38        | 0.56  |
| B1        | 0.055  | 0.065 | 1.40        | 1.65  |
| C         | 0.008  | 0.013 | 0.20        | 0.33  |
| D         | 0.740  | 0.770 | 18.80       | 19.56 |
| E         | 0.300  | 0.325 | 7.62        | 8.26  |
| E1        | 0.230  | 0.280 | 5.84        | 7.11  |
| e         | 0.300  | 0.370 | 7.62        | 9.40  |
| G         | 0.090  | 0.110 | 2.29        | 2.79  |
| L         | 0.115  | 0.150 | 2.92        | 3.81  |
| S         | 0.020  | 0.040 | 0.51        | 1.02  |

# bq2004

## 16-Pin SOIC Narrow (SN)



## 16-Pin SN (0.150" SOIC)

| Dimension | Inches |       | Millimeters |       |
|-----------|--------|-------|-------------|-------|
|           | Min.   | Max.  | Min.        | Max.  |
| A         | 0.060  | 0.070 | 1.52        | 1.78  |
| A1        | 0.004  | 0.010 | 0.10        | 0.25  |
| B         | 0.013  | 0.020 | 0.33        | 0.51  |
| C         | 0.007  | 0.010 | 0.18        | 0.25  |
| D         | 0.385  | 0.400 | 9.78        | 10.16 |
| E         | 0.150  | 0.160 | 3.81        | 4.06  |
| e         | 0.045  | 0.055 | 1.14        | 1.40  |
| H         | 0.225  | 0.245 | 5.72        | 6.22  |
| L         | 0.015  | 0.035 | 0.38        | 0.89  |

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| BQ2004PN         | ACTIVE                | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| BQ2004PNG4       | ACTIVE                | PDIP         | N               | 16   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | N / A for Pkg Type           |
| BQ2004SN         | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| BQ2004SNG4       | ACTIVE                | SOIC         | D               | 16   | 40          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| BQ2004SNTR       | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |
| BQ2004SNTRG4     | ACTIVE                | SOIC         | D               | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ2004SNTR | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**

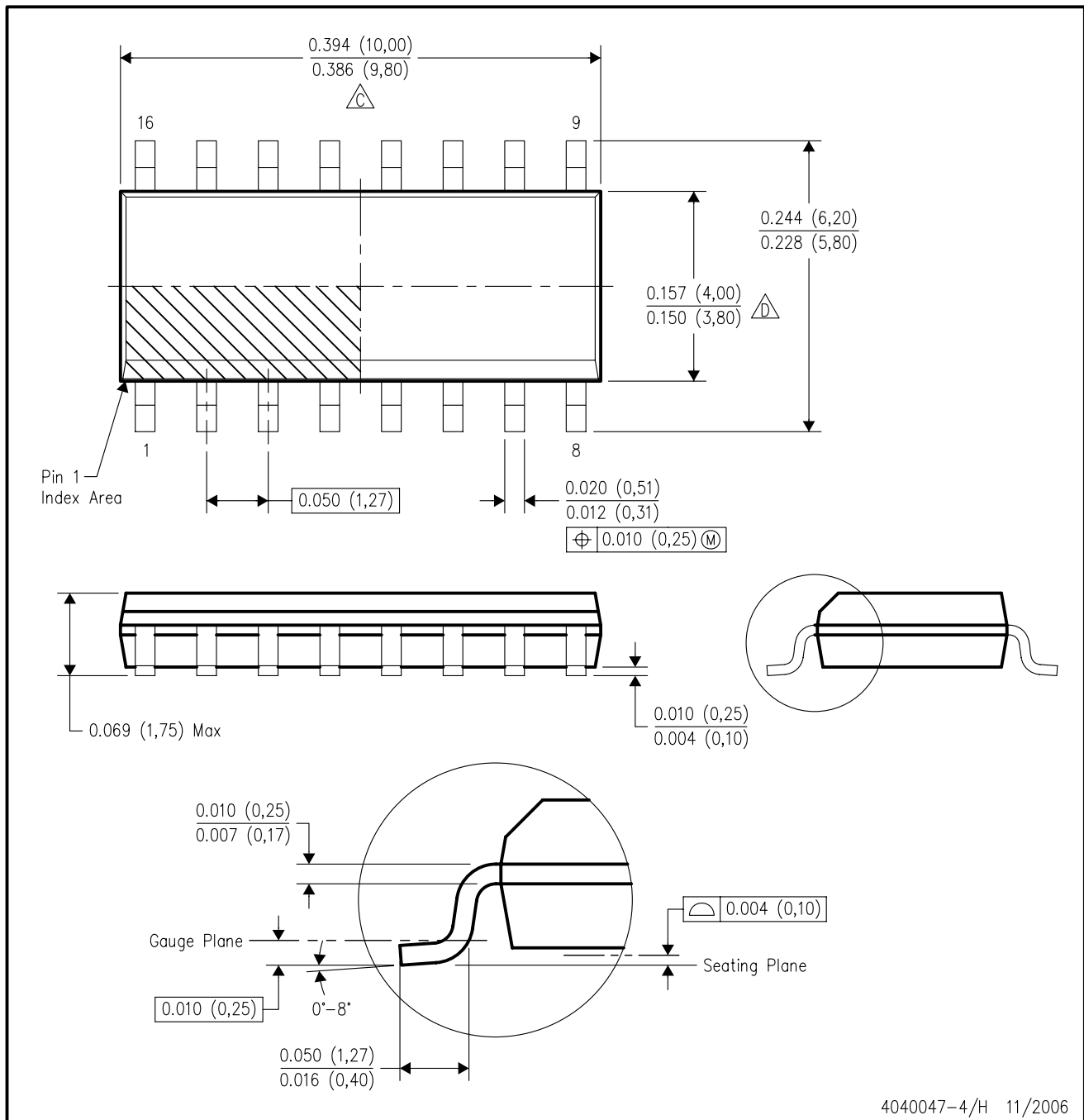


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ2004SNTR | SOIC         | D               | 16   | 2500 | 346.0       | 346.0      | 33.0        |

D (R-PDSO-G16)

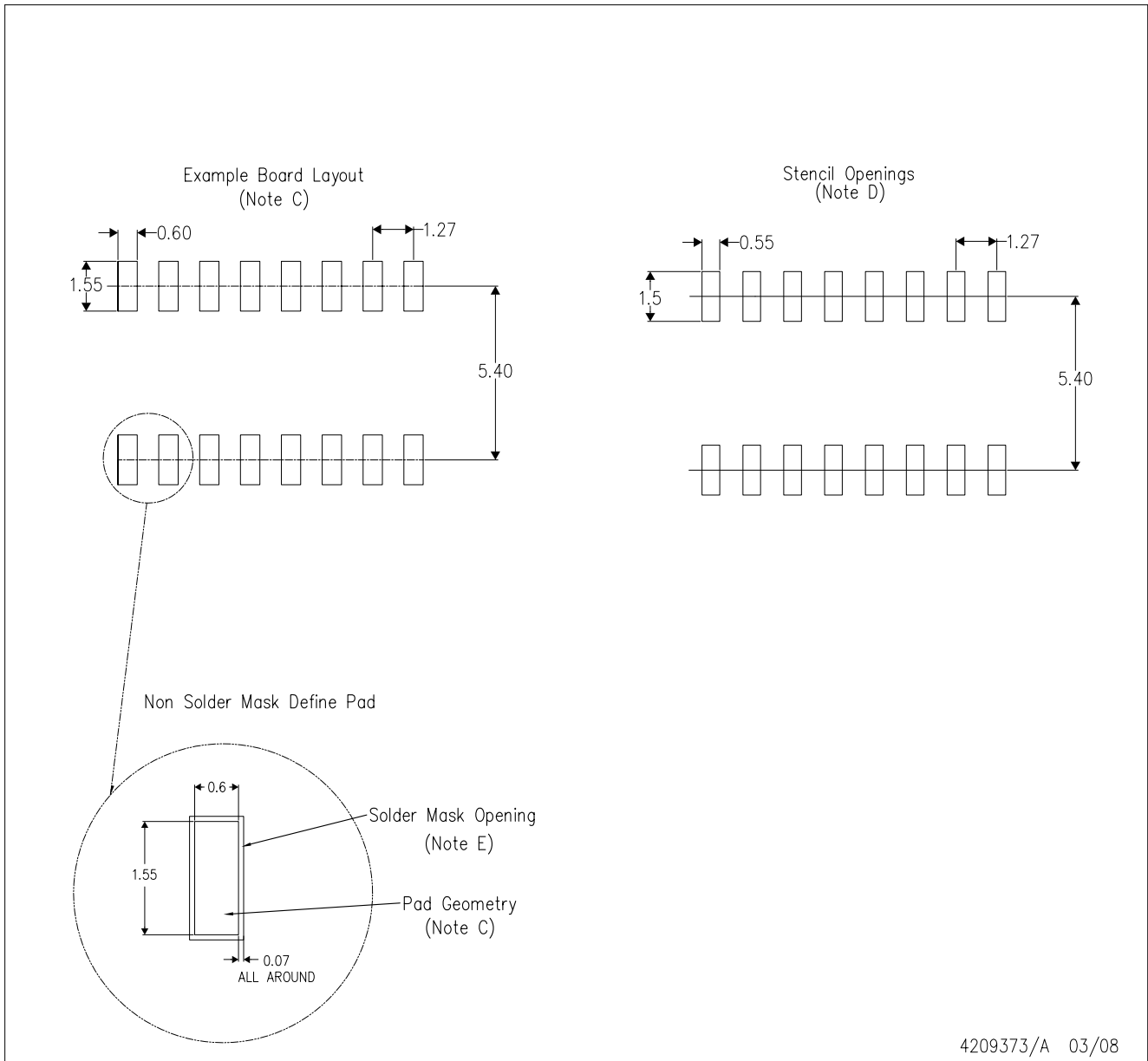
PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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