

CD4000A, CD4001A, CD4002A, CD4025A Types

CMOS NOR Gates

- Dual 3 Input plus Inverter—CD4000A
- Quad 2 Input—CD4001A
- Dual 4 Input—CD4002A
- Triple 3 Input—CD4025A

The RCA-CD4000A, CD4001A, CD4002A, and CD4025A NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Quiescent current specified to 15 V
- Maximum input leakage of 1 μ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

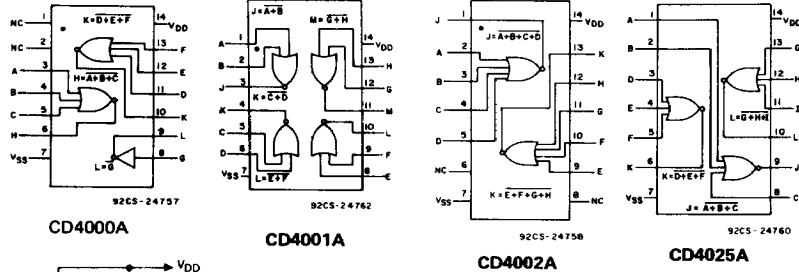
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	12	V

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 15\text{ pF}$, Input t_r , $t_f = 20\text{ ns}$

CHARACTERISTIC	TEST CONDITIONS	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		TYP.	MAX.	TYP.	MAX.	
Propagation Delay Time: High-to-Low Level, t_{PHL}	V_{DD} (Volts)					
	5	35/60	50/95	35/60	80/95	ns
10	25/35	40/60	25/35	55/60		
Low-to-High Level, t_{PLH}	5	35/80	95/120	35/80	120/120	ns
	10	25/40	45/65	25/40	65/65	
Transition Time: High-to-Low Level, t_{THL}	5	65	125	65	200	ns
	10	35	70	35	115	
Low-to-High Level, t_{TLH}	5	65	175	65	300	ns
	10	35	75	35	125	
Input Capacitance, C_i	Any Input	5	—	5	—	pF

Note: Numbers to the right of slash mark are for CD4025A; numbers to the left of slash mark are for 4000A, 4001A, and 4002A.

FUNCTIONAL DIAGRAMS



MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg})	-85 to +160°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
FOR $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5\text{ V}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

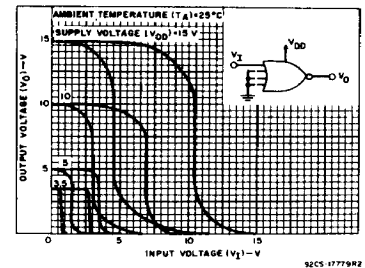


Fig. 1 — Minimum & maximum voltage transfer characteristics.

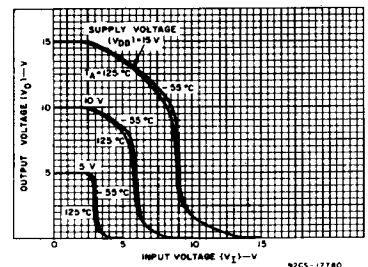


Fig. 2 — Typical voltage transfer characteristics as a function of temperature.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)									UNITS
				D, F, K, H PACKAGES						E PACKAGE			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25		+125	-40	+25		+85		
Quiescent Device Current, I_L Max.	-	-	5	0.05	0.001	0.05	3	0.5	0.005	0.5	15	μA	
	-	-	10	0.1	0.001	0.1	6	5	0.005	5	30		
	-	-	15	2	0.02	2	40	50	0.5	50	500		
Output Voltage: Low Level, V_{OL}	-	0, 5	5	0 Typ.; 0.05 Max									V
	-	0, 10	10	0 Typ.; 0.05 Max									
High Level V_{OH}	-	0, 5	5	4.95 Min.; 5 Typ.									V
	-	0, 10	10	9.95 Min.; 10 Typ.									
Noise Immunity: Inputs Low, V_{NL}	3.6	-	5	1.5 Min.; 2.25 Typ.									V
	7.2	-	10	3 Min.; 4.5 Typ.									
Inputs High V_{NH}	1.4	-	5	1.5 Min.; 2.25 Typ.									V
	2.8	-	10	3 Min.; 4.5 Typ.									
Noise Margin: Inputs Low, V_{NML}	4.5	-	5	1 Min.									V
	9	-	10	1 Min.									
Inputs High, V_{NMH}	0.5	-	5	1 Min.									V
	1	-	10	1 Min.									
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	-	5	0.5	1	0.4	0.28	0.35	1	0.3	0.24	mA	
	0.5	-	10	1.1	2.5	0.9	0.65	0.72	2.5	0.6	0.48		
P-Channel (Source): I_{DP} Min.	2.5	-	5	-0.62	-2	-0.5	-0.35	-0.35	-2	-0.3	-0.24	mA	
	9.5	-	10	-0.62	-1	-0.5	-0.35	-0.3	-1	-0.25	-0.2		
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ± 1 Max.									μA

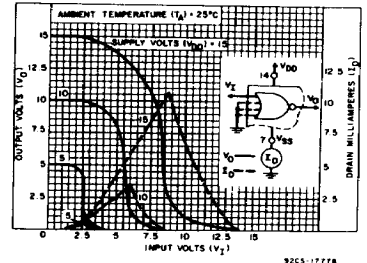


Fig. 3 - Typical current & voltage transfer characteristics.

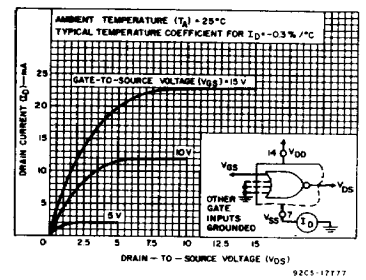


Fig. 4 - Typical n-channel drain characteristics.

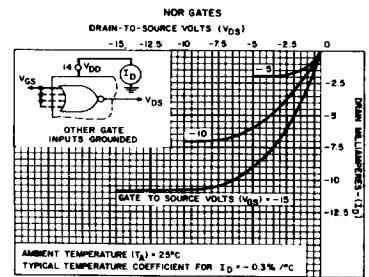


Fig. 5 - Typical p-channel drain characteristics.

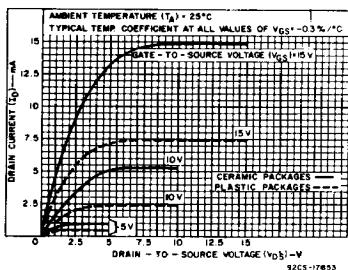


Fig. 6 - Minimum n-channel drain characteristics.

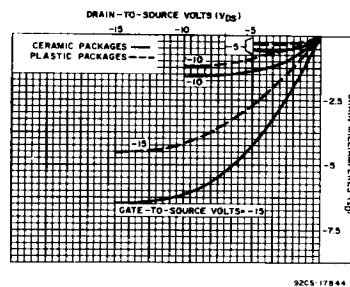


Fig. 7 - Minimum p-channel drain characteristics.

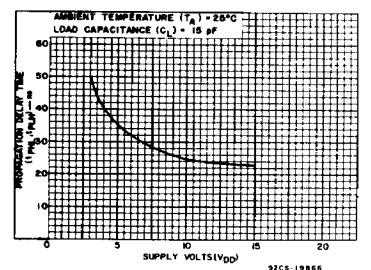


Fig. 8 - Typical propagation delay time vs. V_{DD} .

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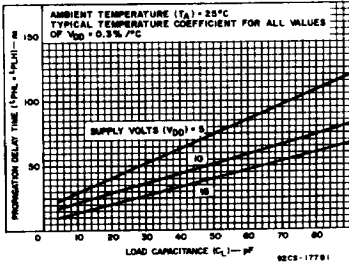


Fig. 9 – Typical propagation delay time vs. C_L .

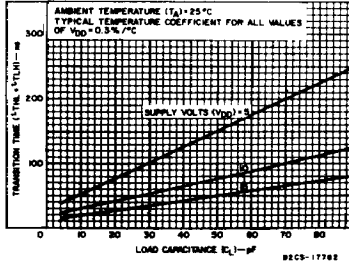


Fig. 10 – Typical transition time vs. C_L .

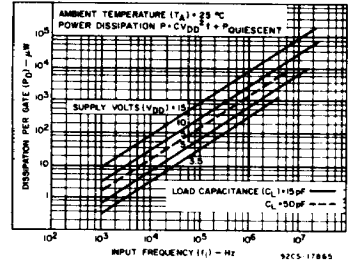


Fig. 11 – Typical dissipation characteristics.

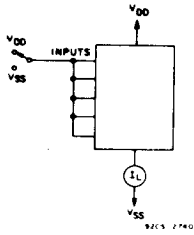


Fig. 12 – Quiescent device current test circuit.

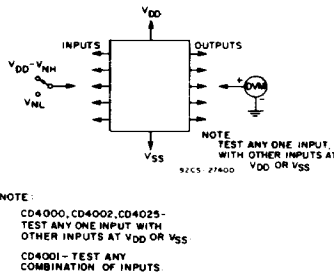


Fig. 13 – Noise immunity test circuit.

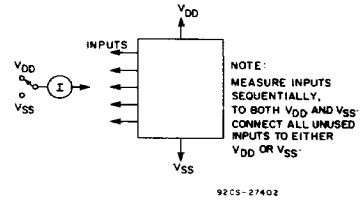


Fig. 14 – Input leakage current test circuit.