CMOS 12-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4040A consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all-0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

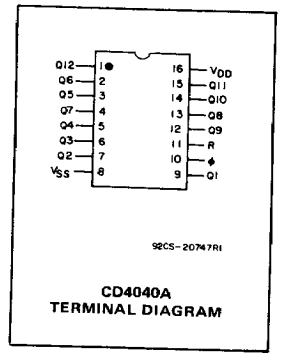
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation . . . 5 MHz (typ.) input pulse rate at $V_{DD} - V_{SS} = 10$ V
- Low output impedance . . . 750 Ω (typ.) at $V_{DD} - V_{SS} = 10$ V and $V_{DS} = 0.5$ V
- Common reset
- Fully static operation
- All 12 buffered outputs available
- Low-power TTL compatible
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Control counters



CD4040A TERMINAL DIAGRAM

RECOMMENDED OPERATING CONDITONS at $T_A = 25°C$, Except as Noted:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges :

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5	400	–	500	–	ns
	10	110	–	125	–	
Input-Pulse Frequency, f_ϕ	5	dc	1.5	dc	1.5	MHz
	10	dc	4	dc	4	
Input-Pulse Rise or Fall Time, $t_{r\phi}, t_{f\phi}$	5	15	–	15	–	μs
	10	15	–	15	–	
Reset Pulse Width, t_W	5	1000	–	1250	–	ns
	10	500	–	600	–	

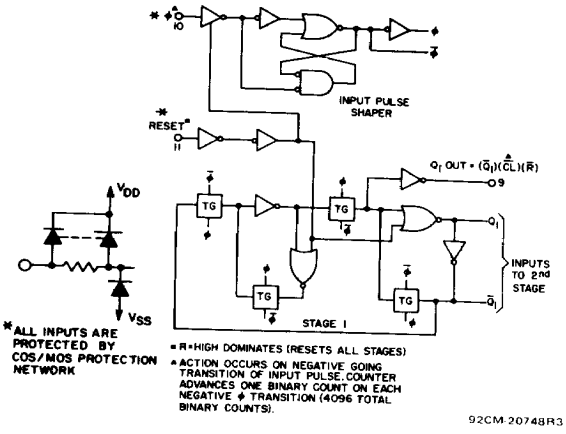


Fig.1 – Logic diagram of CD4040A input pulse shaper and 1 of 12 stages.

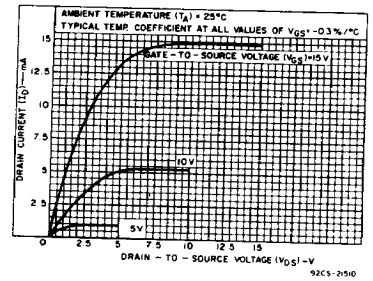


Fig.2 – Typical output n-channel drain characteristics.

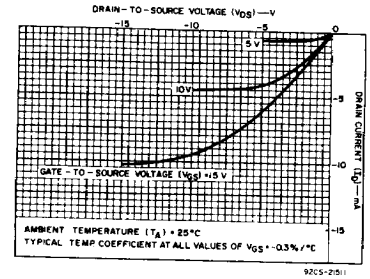


Fig.3 – Typical output p-channel drain characteristics.

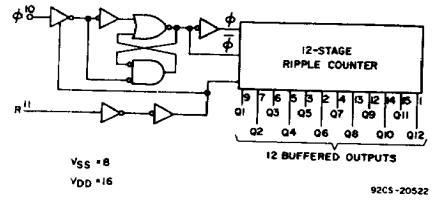


Fig.4 – Functional diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

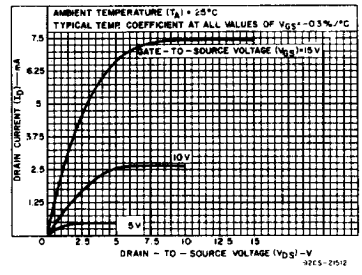


Fig.5 – Minimum output n-channel drain characteristics.

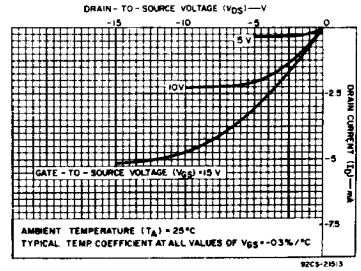


Fig.6 – Minimum output p-channel drain characteristics.

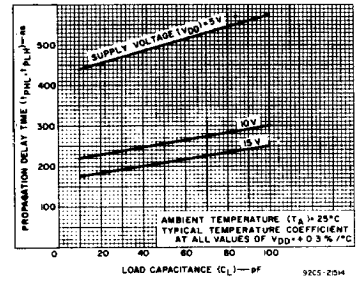


Fig.7 – Typical propagation delay time vs. load capacitance (per stage).

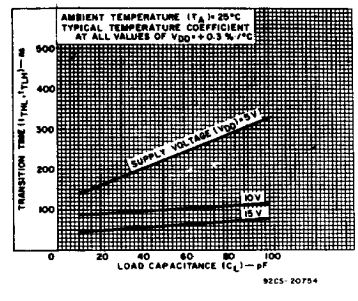


Fig.8 – Typical transition time vs. load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink). I_DN Min.	0.5	–	5	0.22	0.36	0.145	0.102	0.21	0.36	0.08	0.056	mA
	0.5	–	10	0.44	0.75	0.4	0.250	0.42	0.75	0.2	0.14	
P-Channel (Source): I_DP Min.	4.5	–	5	−0.15	−0.25	−0.1	−0.07	−0.15	−0.25	−0.06	−0.04	
	9.5	–	10	−0.03	−0.5	−0.25	−0.175	−0.29	−0.5	−0.15	−0.1	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions		LIMITS						Units
		V_{DD} (V)	D, F, K, H Packages			E Package			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input-Pulse Operation									
Propagation Delay Time, t_{PLH}, t_{PHL}●		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Maximum Input-Pulse Frequency, f_ϕ		5	1.5	2.5	–	1.5	2.5	–	MHz
		10	4	6	–	4	6	–	
Minimum Input-Pulse Width, t_W	f=100 kHZ	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$▲		5	–	–	15	–	–	15	μs
		10	–	–	7.5	–	–	7.5	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}*		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

● Measured from the 50% level of the negative input pulse edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.

▲ Maximum input rise or fall time for functional operation.

* Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).

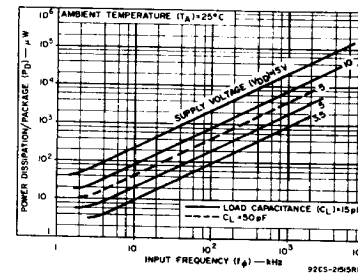


Fig.9 – Typical dissipation characteristics.

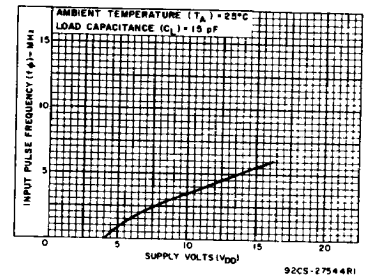


Fig.10 – Typical input-pulse frequency vs. supply voltage.

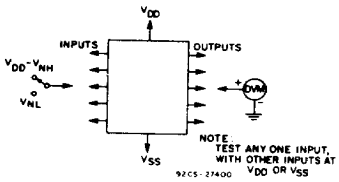


Fig. 11– Noise-immunity test circuit.

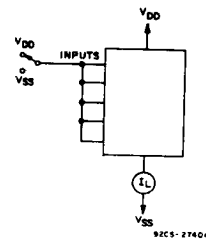


Fig.12 – Quiescent-device-current test circuit.

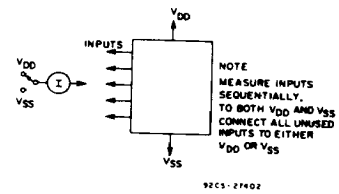


Fig.13 – Input-leakage-current test circuit.