not on the Price List

CMOS 21-Stage Counter

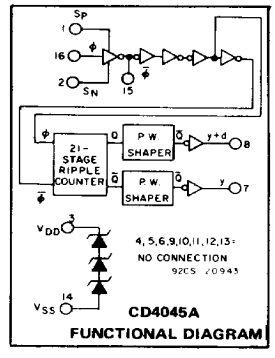
The RCA-CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5-V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 3.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**



FUNCTIONAL DIAGRAM

Features:

- **Microwatt quiescent dissipation . . . . . 2.5 μW (typ.) @ V_{DD} = 5 V; 10 μW (typ.) @ V_{DD} = 10 V**
- **Very low operating dissipation . . . . . 1 mW (typ.); @ V_{DD} = 5 V, fϕ = 1 MHz**
- **Output drivers with sink or source capability . . . . . 7 mA (typ.) @ V_O = 0.5 V, V_{DD} = 5 V (sink) 5 mA (typ.) @ V_O = 4.5 V, V_{DD} = 5 V (source)**
- **Medium speed (typ.) . . . . . fϕ = 5 MHz @ V_{DD} = 5 V fϕ = 10 MHz @ V_{DD} = 10 V**
- **16.5 V zener diode transient protection on chip for automotive use**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W	5 10	115 60	– –	140 75	– –	ns
Input-Pulse Frequency, fϕ	5 10	dc dc	4.4 8.5	dc dc	3.5 6.5	MHz
Input-Pulse Rise or Fall Time, $t_r\phi$, $t_f\phi$	5 10	– –	15 10	– –	15 10	μs

NOTE 1: To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150 Ω current-limiting resistor must be placed in series with the power supply for V_{DD} > 13 V.

NOTE 2: Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in all other CD4000A Series 16-lead devices).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H Packages			E Package			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: ϕ to y or y+d out t_{PLH}, t_{PHL}	5	–	2.2	4.4	–	2.2	5.5	μs
	10	–	1.2	2.4	–	1.2	3.3	
Transition Time: t_{THL}, t_{TLH}	5	–	450	800	–	450	900	ns
	10	–	375	650	–	375	750	
Maximum Input-Pulse Frequency, $f_{m\phi}$	5	4.4	5	–	3.5	5	–	MHz
	10	8.5	10	–	6.5	10	–	
Minimum Input-Pulse Width, t_W	5	–	100	115	–	100	140	ns
	10	–	50	60	–	50	75	
Input-Pulse Rise & Fall Time; $t_r\phi$, $t_f\phi$	5	–	–	15	–	–	15	μs
	10	–	–	10	–	–	10	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

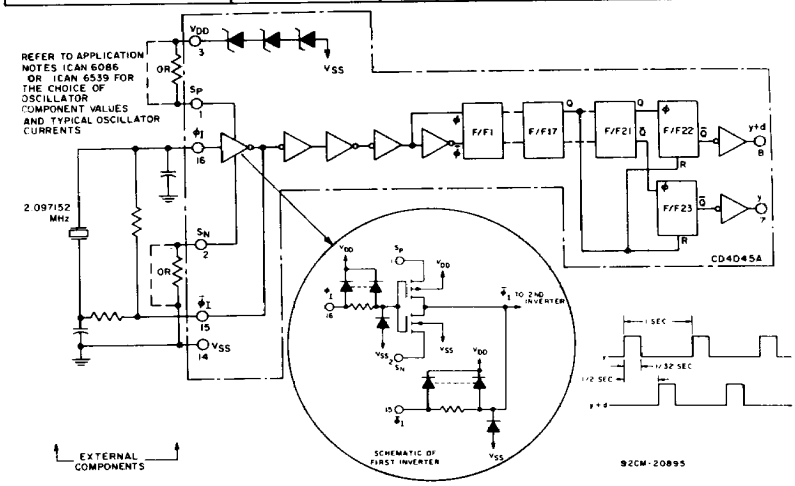


Fig. 3 – CD4045A and outboard components in a typical 21-stage counter application.

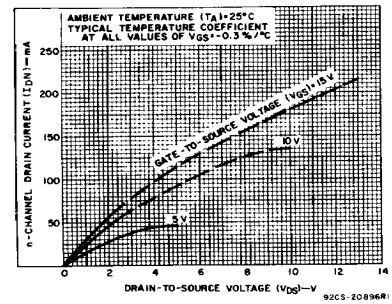


Fig. 1 – Typical output n-channel drain characteristics.

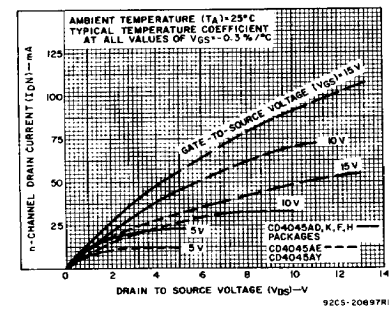


Fig. 2 – Minimum output n-channel drain characteristcs.

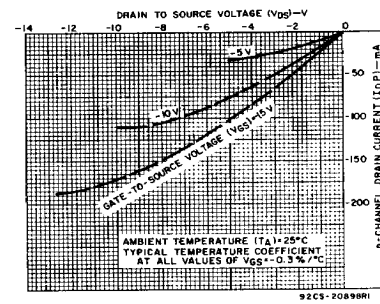


Fig. 4 – Typical output p-channel drain characteristics.

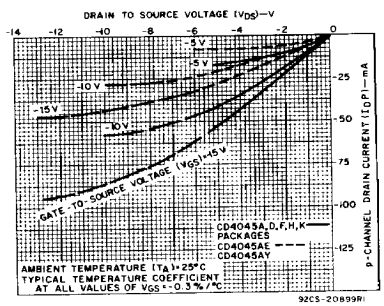


Fig. 5 – Minimum output p-channel drain characteristics.

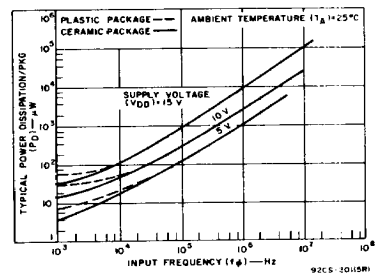


Fig. 6 – Typical dissipation vs input frequency (21 counting stages).

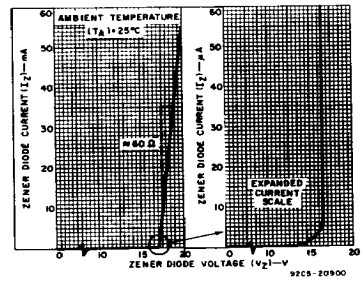


Fig. 7 – Typical zener diode characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_{DN} Min.	0.5	–	5	4.4	7	3.5	2.5	2.2	7	1.8	1.3	mA
	0.5	–	10	6.9	11	6.5	3.9	3.5	11	2.8	2	
p-Channel (Source): I_{DP} Min.	4.5	–	5	−3.1	−5	−2.5	−1.8	−1.6	−5	−1.3	−0.9	
	9.5	–	10	−5.6	−9	−4.5	−3.2	−2.8	−9	−2.3	−1.6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA
Zener Breakdown Voltage, $V_{(BR)Z}$	1–100 μA		Min.	13.3	–	13.5	13.7	13.3	–	13.5	13.6	V
			Typ.	–	16.5	–	–	–	16.5	–	–	
			Max.	17.8	–	18	18.2	17.8	–	18	18.1	

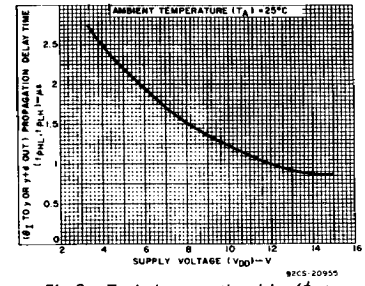


Fig. 8 – Typical propagation delay (ϕ_1 to y or y+d out) vs V_{DD}.

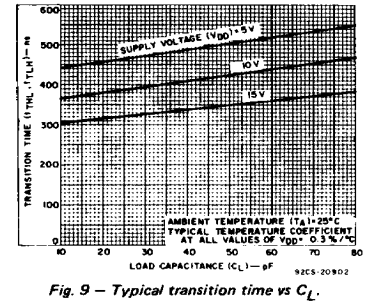


Fig. 9 – Typical transition time vs C_L.

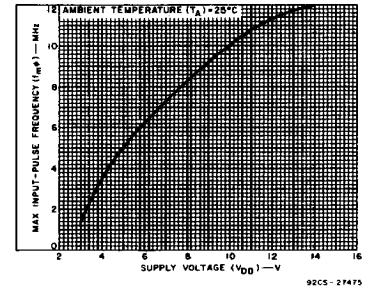


Fig. 10 – Typical maximum input-pulse frequency.

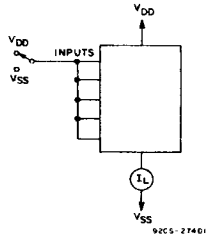


Fig. 11 – Quiescent-device-current test circuit.

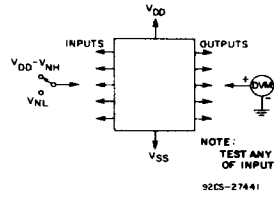


Fig. 12 – Noise-immunity test circuit.

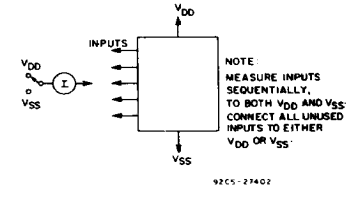


Fig. 13 – Input-leakage-current test circuit.