

CD4049A, CD4050A Types

CMOS Hex Buffer/Converters

CD4049A—Inverting Type
 CD4050A—Non-Inverting Type

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. ($V_{CC}=5\text{ V}$, $V_{OL} \geq 0.4\text{ V}$, and $I_{DN} \geq 3.2\text{ mA}$.)

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069 Hex Inverter is recommended.

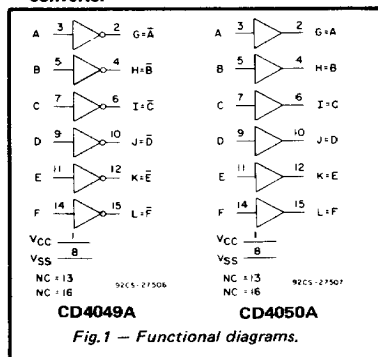
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- Quiescent current specified to 15 μA
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)

Applications:

- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic-level converter



RECOMMENDED OPERATING CONDITIONS at $T_A=25^\circ\text{C}$, Except as Noted.
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A : Full Package-Temperature Range)	3	12	V
Input Voltage Range (V_I)	V_{CC}^*	12	V

*The CD4049 and CD4050 have high-to-low level voltage conversion capability but not low-to-high-level, therefore it is recommended that $V_I \geq V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures ($^\circ\text{C}$)								Units
				D, F, K, H Packages				E Package				
				-55	+25		+125	-40	+25		+85	
Quiescent Device Current, I_L Max.	—	—	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	—	—	10	0.5	0.01	0.5	30	5	0.05	5	70	
	—	—	15	10	0.02	10	100	50	0.05	50	500	
Output Voltage: Low-Level, V_{OL}	—	0, 5	5	0 Typ.; 0.05 Max.								V
High-Level, V_{OH}	—	0, 5	5	4.95 Min.; 5 Typ.								
Noise Immunity: Inputs Low, V_{NL}	3.6	—	5	1.5 Min.; 2.25 Typ.								V
CD4050A	7.2	—	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	1.4	—	5	1.5 Min.; 2.25 Typ.								
All Types	2.8	—	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML} Min.	3.6	—	5	1 Min.; 1.5 Typ.								V
CD4049A	7.2	—	10	2 Min.; 3 Typ.								
Inputs High, V_{NMH} Min.	0.5	—	5	1 Min.								V
CD4050A	1	—	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_{DN} Min.	0.4	—	4.5	3.3	5.2	2.6	1.8	3.1	5.2	2.6	2.1	mA
P-Channel (Source), I_{DP} Min.	0.4	—	5	3.75	6	3	2.1	3.6	6	3	2.5	
	0.5	—	10	10	16	8	5.6	9.6	16	8	6.6	
	4.5	—	5	-0.62	-1	-0.5	-0.35	-0.6	-1	-0.5	-0.4	
	2.5	—	5	-1.85	-2.5	-1.25	-0.9	-1.5	-2.5	-1.25	-1	
	9.5	—	10	-1.85	-2.5	-1.25	-0.9	-1.5	-2.5	-1.25	-1	
Input Leakage Current, I_{IL} , I_{IH} Max.	Any Input	15		$\pm 10^{-5}$ Typ., ± 1 Max.								μA

CD4049A, CD4050A Types

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{STG})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{CC})	
(Voltages referenced to V_{SS} Terminal)	-0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

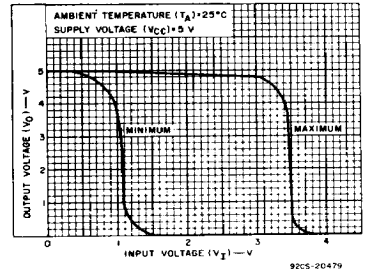


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049A.

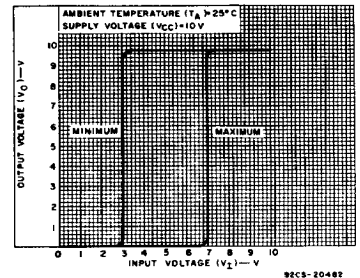


Fig. 5—Minimum and maximum voltage transfer characteristics for CD4050A.

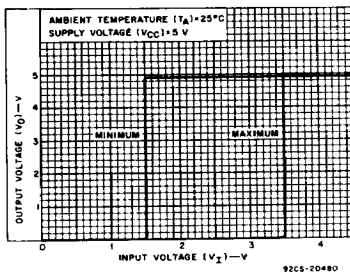


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050A.

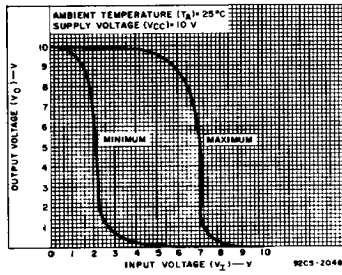


Fig. 4—Minimum and maximum voltage transfer characteristics for CD4049A.

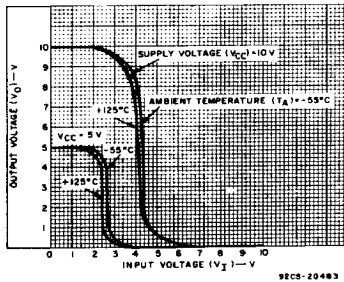


Fig. 6—Typical voltage transfer characteristics as a function of temperature for CD4049A.

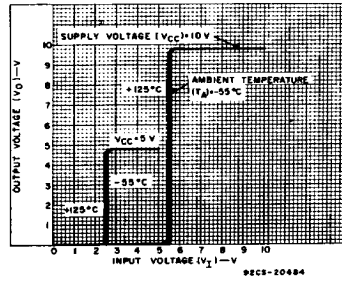


Fig. 7—Typical voltage transfer characteristics as a function of temperature for CD4050A.

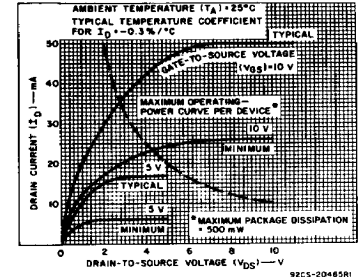


Fig. 8—Typical and minimum n-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

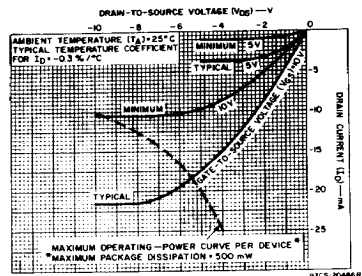


Fig. 9—Typical and minimum p-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

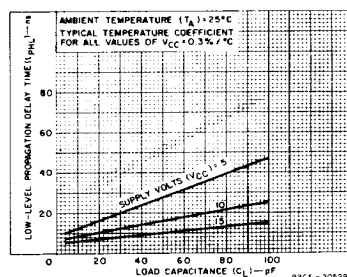


Fig. 10—Typical high-to-low level propagation delay time vs. C_L for CD4049A.

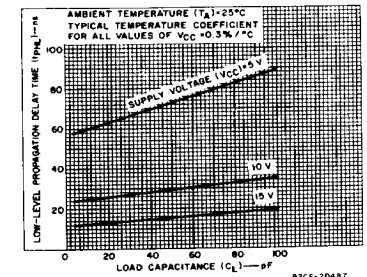


Fig. 11—Typical high-to-low level propagation delay time vs. C_L for CD4050A.

CD4049A, CD4050A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$; Input $t_r, t_f=20\text{ ns}$, $C_L=15\text{ pF}$, $R_I=200\text{ k}\Omega$

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_I	V_{CC}	Typ.	Max.	
Propagation Delay Time: Low-to-High, t_{PLH}	5	5	50	80	ns
			10	10	
	5	5	75	140	
			10	10	
High-to-Low, t_{PHL}	5	5	15	55	ns
			10	10	
	5	5	55	110	
			10	10	
Transition Time: Low-to-High, t_{TLH}	5	5	50	100	ns
			10	10	
	5	5	20	45	
			10	10	
Input Capacitance, C_I	CD4049A	—	—	15	pF
	CD4050A	—	—	5	

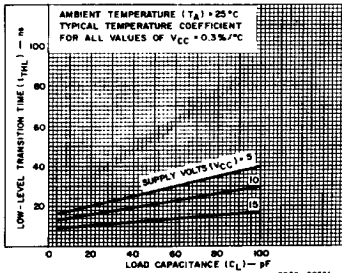


Fig. 14—Typical high-to-low level transition time vs. C_L for CD4049A, CD4050A.

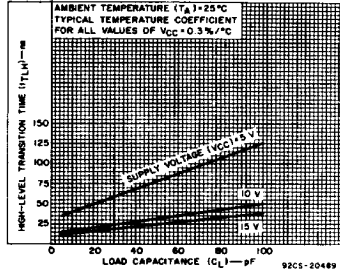


Fig. 15—Typical low-to-high level transition time vs. C_L for CD4049A, CD4050A.

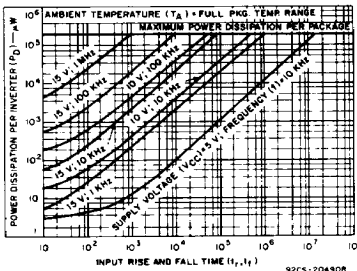


Fig. 17—Typical power dissipation vs. transition time per inverter CD4049A.

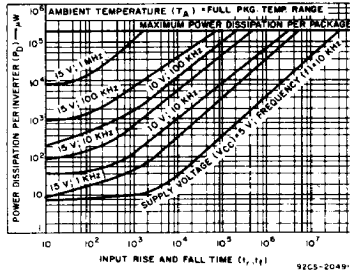


Fig. 18—Typical power dissipation vs. transition time per inverter CD4050A.

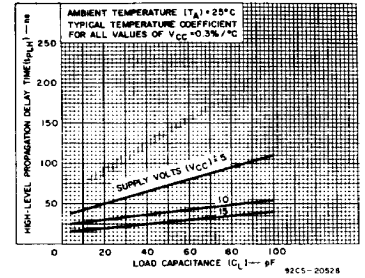


Fig. 12—Typical low-to-high level propagation delay time vs. C_L for CD4049A.

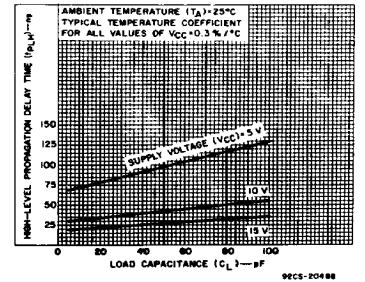


Fig. 13—Typical low-to-high level propagation delay time vs. C_L for CD4050A.

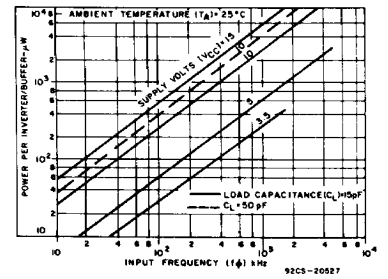


Fig. 16—Typical dissipation characteristics for CD4049A, CD4050A.

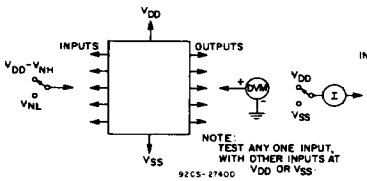


Fig. 19—Noise immunity test circuit.

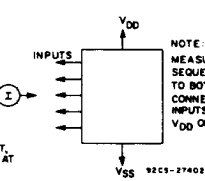


Fig. 20—Input leakage current test circuit.

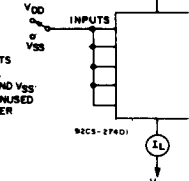


Fig. 21—Quiescent device current test circuit.

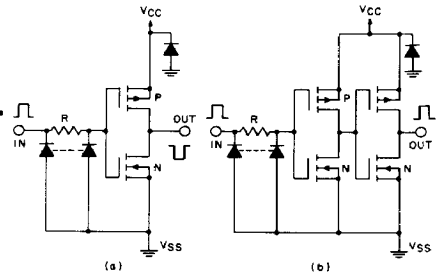


Fig. 22—(a) Schematic diagram of CD4049A, 1 of 6 identical units. (b) Schematic diagram of CD4050A, 1 of 6 identical units.