

CMOS

Binary Rate Multiplier

High-Voltage Types (20-Volt Rating)

■ CD4089B is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used in conjunction with an up/down counter and control logic used to perform arithmetic operations (adds, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4 bits, CD4089B devices may be cascaded in two different modes: an Add mode and a Multiply mode (see Figs. 14 and 15). In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus the output rate will be

$$\frac{11}{16} \times \frac{13}{16} = \frac{143}{256}$$

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DQ INPUT CURRENT, ANY ONE INPUT ±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55°C to +100°C 500mW

For T_A = +100°C to +125°C Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

Features:

- Cascadable in multiples of 4-bits
- Set to "15" input and "15" detect output
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =

- 1 V at V_{DD} = 5 V
- 2 V at V_{DD} = 10 V
- 2.5 V at V_{DD} = 15 V

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Numerical control
- Instrumentation
- Digital filtering
- Frequency synthesis

The CD4089B has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in Fig. 2.

If more than one binary input bit is high, the resulting pulse train is a combination of the separate pulse trains as shown in Fig. 2.

The CD4089B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

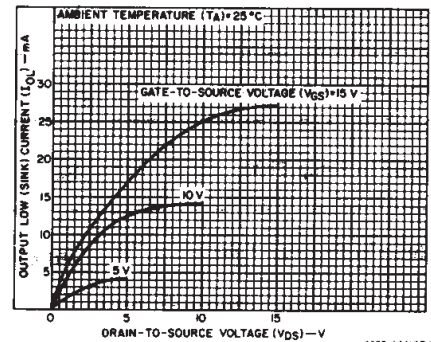
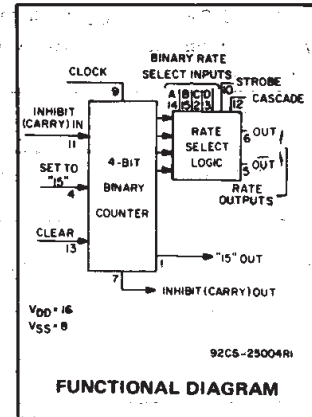


Fig. 1 - Typical output low (sink) current characteristics.

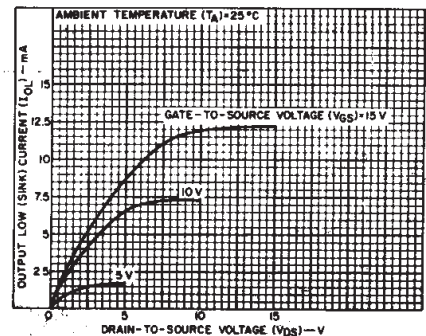


Fig. 2 - Minimum output low (sink) current characteristics.

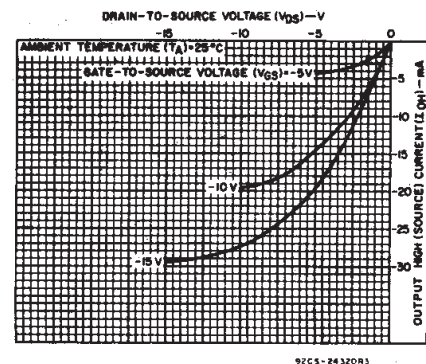


Fig. 3 - Typical output high (source) current characteristics.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4089B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V_{DD} (V) | LIMITS | | UNITS |
|---|--------------|--------|------|---------------|
| | | Min. | Max. | |
| Supply-Voltage Range (For T_A = Full Package-Temperature Range) | | 3 | 18 | V |
| Set or Clear Pulse Width, t_W | 5 | 160 | — | ns |
| | 10 | 90 | — | |
| | 15 | 60 | — | |
| Clock Pulse Width, t_W | 5 | 330 | — | ns |
| | 10 | 170 | — | |
| | 15 | 100 | — | |
| Clock Frequency, f_{CL} | 5 | — | 1.2 | MHz |
| | 10 | dc | 2.5 | |
| | 15 | — | 3.5 | |
| Clock Rise or Fall Time, t_{rCL} or t_{fCL} | 5 | — | — | μs |
| | 10, 15 | — | 15 | |
| Inhibit In Setup Time, t_{SU} | 5 | 100 | — | ns |
| | 10 | 40 | — | |
| | 15 | 20 | — | |
| Inhibit In Removal Time, t_{REM} | 5 | 240 | — | ns |
| | 10 | 130 | — | |
| | 15 | 110 | — | |
| Set Removal Time, t_{REM} | 5 | 150 | — | ns |
| | 10 | 80 | — | |
| | 15 | 50 | — | |
| Clear Removal Time, t_{REM} | 5 | 60 | — | ns |
| | 10 | 40 | — | |
| | 15 | 30 | — | |

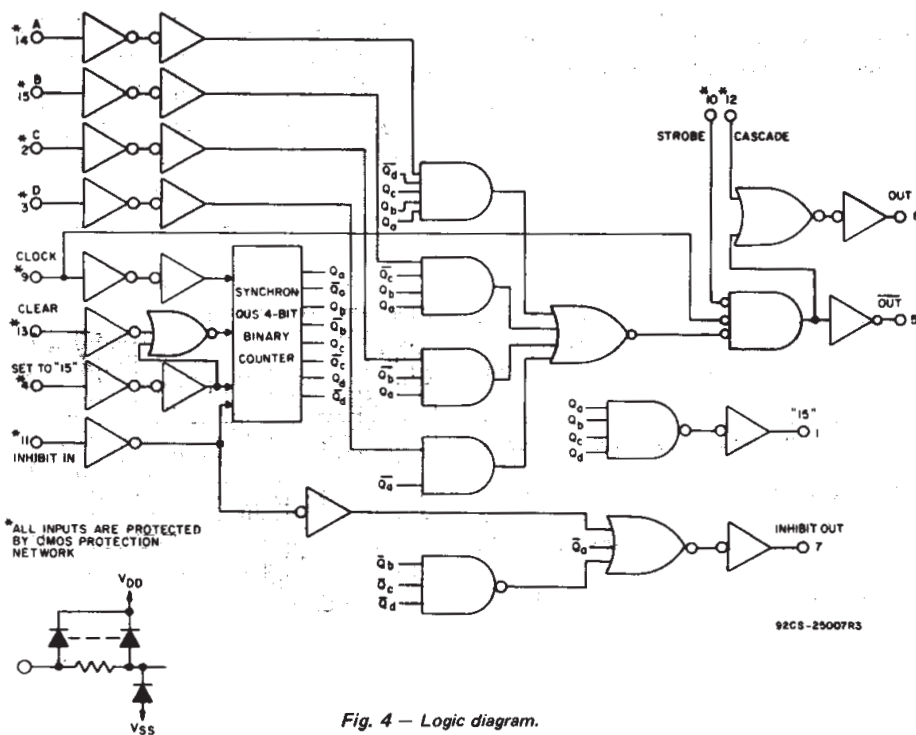


Fig. 4 — Logic diagram.

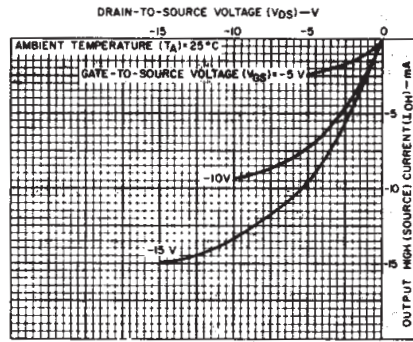


Fig. 5 — Minimum output high (source) current characteristics.

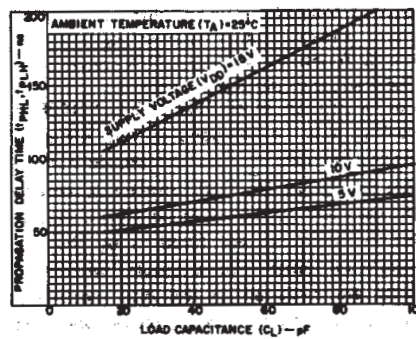


Fig. 6 — Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

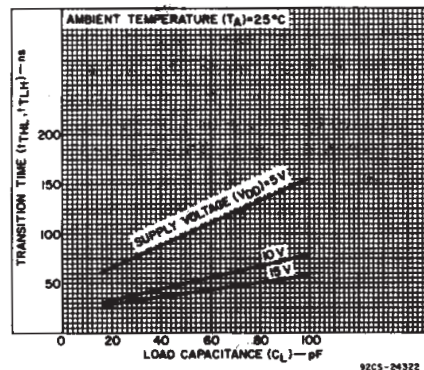


Fig. 7 — Typical transition time as a function of load capacitance.

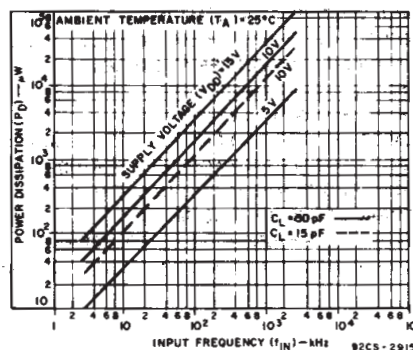


Fig. 8 — Typical dynamic power dissipation as a function of input frequency.

CD4089B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$:
 Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|--|-----------------|----------|------|------|-------|---------------|
| | | VDD V | Min. | Typ. | | Max. |
| Propagation Delay Time, t_{PHL}, t_{PLH} Clock to $\overline{\text{Out}}$ | | 5 | — | 110 | 220 | ns |
| | | 10 | — | 55 | 110 | |
| | | 15 | — | 45 | 90 | |
| Clock or Strobe to Out | | 5 | — | 150 | 300 | ns |
| | | 10 | — | 75 | 150 | |
| | | 15 | — | 60 | 120 | |
| Clock to Inhibit Out High Level to Low Level | | 5 | — | 360 | 720 | ns |
| | | 10 | — | 160 | 320 | |
| | | 15 | — | 110 | 220 | |
| Low Level to High Level | | 5 | — | 250 | 500 | ns |
| | | 10 | — | 100 | 200 | |
| | | 15 | — | 75 | 150 | |
| Clear to Out | | 5 | — | 380 | 760 | ns |
| | | 10 | — | 175 | 350 | |
| | | 15 | — | 130 | 260 | |
| Clock to "9" or "15" Out | | 5 | — | 300 | 600 | ns |
| | | 10 | — | 125 | 250 | |
| | | 15 | — | 90 | 180 | |
| Cascade to Out | | 5 | — | 90 | 180 | ns |
| | | 10 | — | 45 | 90 | |
| | | 15 | — | 35 | 70 | |
| Inhibit In to Inhibit Out | | 5 | — | 160 | 320 | ns |
| | | 10 | — | 75 | 150 | |
| | | 15 | — | 55 | 110 | |
| Set to Out | | 5 | — | 330 | 660 | ns |
| | | 10 | — | 150 | 300 | |
| | | 15 | — | 110 | 220 | |
| Transition Time, t_{THL}, t_{TLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Maximum Clock Frequency, f_{CL} | | 5 | 1.2 | 2.4 | — | MHz |
| | | 10 | 2.5 | 5 | — | |
| | | 15 | 3.5 | 7 | — | |
| Minimum Clock Pulse Width, t_W | | 5 | — | 165 | 330 | ns |
| | | 10 | — | 85 | 170 | |
| | | 15 | — | 50 | 100 | |
| Clock Rise or Fall Time, t_{rCL}, t_{fCL} | | 5 | — | — | 15 | μs |
| | | 10 | — | — | 15 | |
| | | 15 | — | — | 15 | |
| Minimum Set or Clear Pulse Width, t_W | | 5 | — | 80 | 160 | ns |
| | | 10 | — | 45 | 90 | |
| | | 15 | — | 30 | 60 | |
| Minimum Inhibit-In Setup Time, t_{SU} | | 5 | — | 50 | 100 | ns |
| | | 10 | — | 20 | 40 | |
| | | 15 | — | 10 | 20 | |
| Minimum Inhibit In Removal Time, t_{REM} | | 5 | — | 120 | 240 | ns |
| | | 10 | — | 65 | 130 | |
| | | 15 | — | 55 | 110 | |

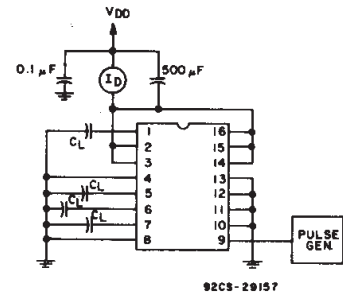


Fig. 9 — Dynamic power dissipation test circuit.

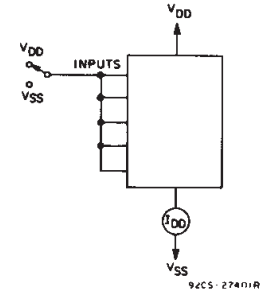


Fig. 10 — Quiescent device current test circuit.

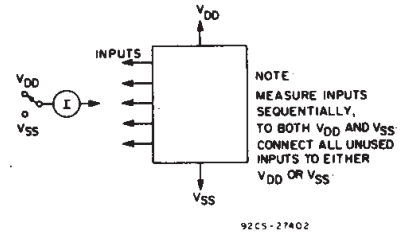


Fig. 11 — Input-current test circuit.

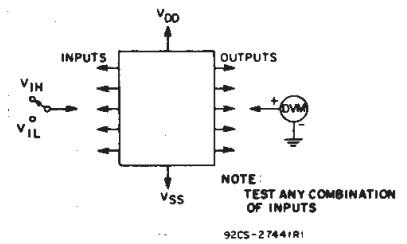
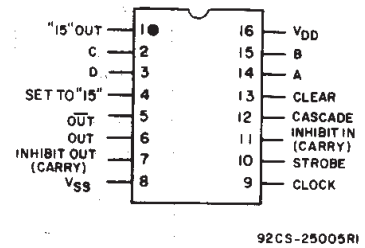


Fig. 12 — Input-voltage test circuit.



TOP VIEW
TERMINAL ASSIGNMENT

3
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HIGH VOLTAGE ICs

CD4089B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ (cont'd)
 Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | | UNITS |
|---------------------------------------|-----------------|---------------|------|------|------|-------|
| | | V_{DD} V | | | | |
| | | | Min. | Typ. | Max. | |
| Minimum Set Removal Time, t_{REM} | | 5 | — | 75 | 150 | ns |
| | | 10 | — | 40 | 80 | |
| | | 15 | — | 25 | 50 | |
| Minimum Clear Removal Time, t_{REM} | | 5 | — | 30 | 60 | ns |
| | | 10 | — | 20 | 40 | |
| | | 15 | — | 15 | 30 | |
| Input Capacitance, C_{IN} | Any Input | — | — | 5 | 7.5 | pF |

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES ($^\circ\text{C}$) | | | | | | | UNITS |
|---|--------------|-----------------|-----------------|---|-----------|---------|---------|-------|---------------|-----------|---------------|
| | | | | | | | +25 | | | | |
| | V_O (V) | V_{IN} (V) | V_{DD} (V) | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, I_{DD} Max. | — | 0,5 | 5 | 5 | 5 | 150 | 150 | — | 0.04 | 5 | μA |
| | — | 0,10 | 10 | 10 | 10 | 300 | 300 | — | 0.04 | 10 | |
| | — | 0,15 | 15 | 20 | 20 | 600 | 600 | — | 0.04 | 20 | |
| | — | 0,20 | 20 | 100 | 100 | 3000 | 3000 | — | 0.08 | 100 | |
| Output Low (Sink) Current I_{OL} Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| Output High (Source) Current, I_{OH} Min. | 4.6 | 0,5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | mA |
| | 2.5 | 0,5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| | 9.5 | 0,10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| | 13.5 | 0,15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| Output Voltage: Low-Level, V_{OL} Max. | — | 0,5 | 5 | 0.05 | | | | — | 0 | 0.05 | V |
| | — | 0,10 | 10 | 0.05 | | | | — | 0 | 0.05 | |
| | — | 0,15 | 15 | 0.05 | | | | — | 0 | 0.05 | |
| Output Voltage: High-Level, V_{OH} Min. | — | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | — | V |
| | — | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | — | |
| | — | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | — | |
| Input Low Voltage V_{IL} Max. | 0.5, 4.5 | — | 5 | 1.5 | | | | — | — | 1.5 | V |
| | 1.9 | — | 10 | 3 | | | | — | — | 3 | |
| | 1.5, 13.5 | — | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, V_{IH} Min. | 0.5, 4.5 | — | 5 | 3.5 | | | | 3.5 | — | — | V |
| | 1.9 | — | 10 | 7 | | | | 7 | — | — | |
| | 1.5, 13.5 | — | 15 | 11 | | | | 11 | — | — | |
| Input Current I_{IN} Max. | — | 0,18 | 18 | ± 0.1 | ± 0.1 | ± 1 | ± 1 | — | $\pm 10^{-5}$ | ± 0.1 | μA |

CD4089B Types

TRUTH TABLE

| INPUTS | | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|-----|--------|-----|-----|-----|-----|--|-------------------------|---------|----------|
| Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care) | | | | | | | | | | Number of Pulses or Output Logic Level (L = Low; H = High) | | | |
| D | C | B | A | CLK | INH IN | STR | CAS | CLR | SET | OUT | $\overline{\text{OUT}}$ | INH OUT | "15" OUT |
| 0 | 0 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | L | H | 1 | 1 |
| 0 | 0 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 2 | 2 | 1 | 1 |
| 0 | 0 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 3 | 3 | 1 | 1 |
| 0 | 1 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 4 | 4 | 1 | 1 |
| 0 | 1 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 5 | 5 | 1 | 1 |
| 0 | 1 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 6 | 6 | 1 | 1 |
| 0 | 1 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 7 | 7 | 1 | 1 |
| 1 | 0 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 1 | 1 |
| 1 | 0 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 9 | 9 | 1 | 1 |
| 1 | 0 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 10 | 10 | 1 | 1 |
| 1 | 0 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 11 | 11 | 1 | 1 |
| 1 | 1 | 0 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 12 | 12 | 1 | 1 |
| 1 | 1 | 0 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 13 | 13 | 1 | 1 |
| 1 | 1 | 1 | 0 | 16 | 0 | 0 | 0 | 0 | 0 | 14 | 14 | 1 | 1 |
| 1 | 1 | 1 | 1 | 16 | 0 | 0 | 0 | 0 | 0 | 15 | 15 | 1 | 1 |
| X | X | X | X | 16 | 1 | 0 | 0 | 0 | 0 | † | † | H | † |
| X | X | X | X | 16 | 0 | 1 | 0 | 0 | 0 | L | H | 1 | 1 |
| X | X | X | X | 16 | 0 | 0 | 1 | 0 | 0 | H | * | 1 | 1 |
| 1 | X | X | X | 16 | 0 | 0 | 0 | 1 | 0 | 16 | 16 | H | L |
| 0 | X | X | X | 16 | 0 | 0 | 0 | 1 | 0 | L | H | H | L |
| X | X | X | X | 16 | 0 | 0 | 0 | X | 1 | L | H | L | H |

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

† Depends on internal state of counter.

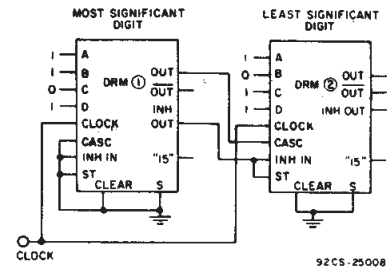


Fig. 13 - Two CD4089B's cascaded in the "Add" mode with a preset number

$$\text{of } 189 \left(\frac{11}{16} + \frac{13}{256} = \frac{189}{256} \right)$$

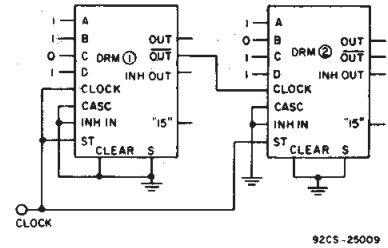
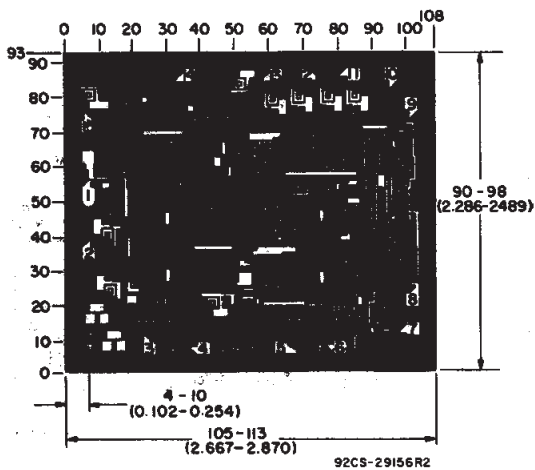


Fig. 14 - Two CD4089B's cascaded in the "Multiply" mode with a preset number

$$\text{of } 143 \left(\frac{11}{16} \times \frac{13}{256} = \frac{143}{256} \right)$$



Dimensions and Pad Layout for CD4089BH

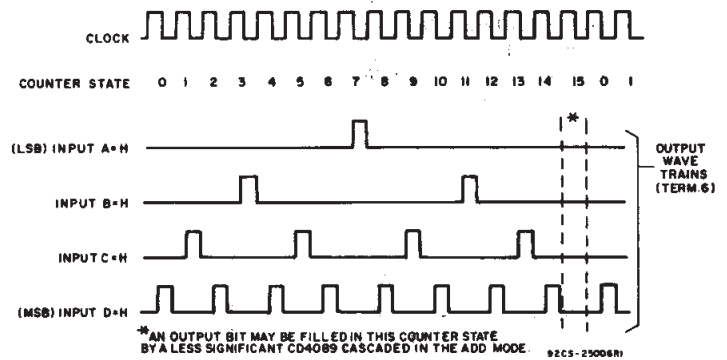


Fig. 15 - Timing diagram.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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