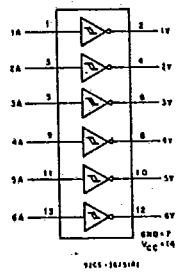
Advance Information

CD54/74AC14
CD54/74ACT14

T-51-21-00



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Hex Inverting Schmitt Trigger

Type Features:
- *Operates with much slower than standard input rise and fall slew rates*
- *Exceptionally high noise immunity*

The RCA CD54/74AC14 and CD54/74ACT14 each contain six inverting Schmitt Triggers in one package. These devices use the RCA ADVANCED CMOS technology.

The CD74AC14 and CD74ACT14 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC14 and CD54ACT14, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:
- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*
- *Greater noise immunity than standard inverters*

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

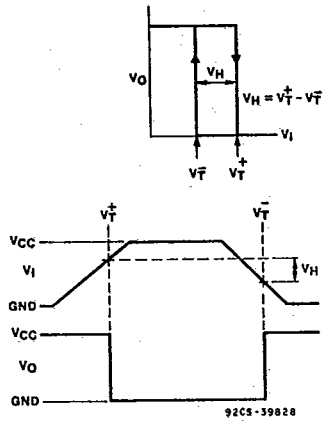


Fig. 1 - Hysteresis definition and characteristic.

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TRUTH TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = High Level
L = Low Level

File Number **1984**

Technical Data

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CD54/74AC14
CD54/74ACT14

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv†:			
at 1.5 V to 5.5 V (AC Types)	0	150	ms/V
at 4.5 V to 5.5 V (ACT Types)	0	20	ns/V

*Unless otherwise specified, all voltages are referenced to ground.
†5 Outputs switching
V_{CC} = 5 V
Load = 500Ω, 50 pF
T_A = Full temperature range
For AC14, V_I = 5.5 V sawtooth
For ACT14, V_I = 3 V sawtooth

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Positive-Going Threshold Voltage V_T^+			5	2.6	3.4	2.6	3.4	2.6	3.4	V
Negative-Going Threshold Voltage V_T^-			5	1.6	2.4	1.6	2.4	1.6	2.4	V
Hysteresis Voltage V_H			5	0.5	—	0.5	—	0.5	—	V
High-Level Output Voltage V_{OH}	V_T^+ or V_T^-	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_T^+ or V_T^-	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current,SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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Technical Data

T-51-21

CD54/74AC14
CD54/74ACT14

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Positive-Going Threshold Voltage V_T^+			5	1.4	2	1.4	2	1.4	2	V
Negative-Going Threshold Voltage V_T^-			5	0.9	1.3	0.9	1.3	0.9	1.3	V
Hysteresis Voltage V_H			5	0.4	—	0.4	—	0.4	—	V
High-Level Output Voltage V_{OH}	V_T^+ or V_T^-	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_T^+ or V_T^-	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current,SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1	—	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
ALL	0.21

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

T-51-21

CD54/74AC14
CD54/74ACT14

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

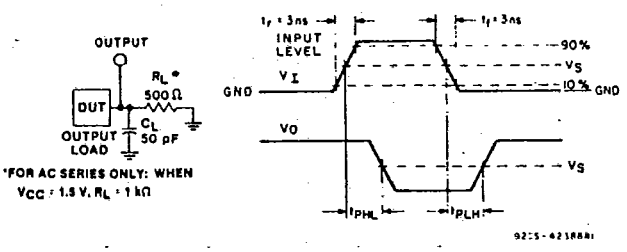
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH} t_{PHL}	5†	2.7	9.5	2.6	10.5	ns
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH}	5†	3.7	13.2	3.6	14.5	ns
	t_{PHL}		2.4	8.6	2.4	9.5	
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

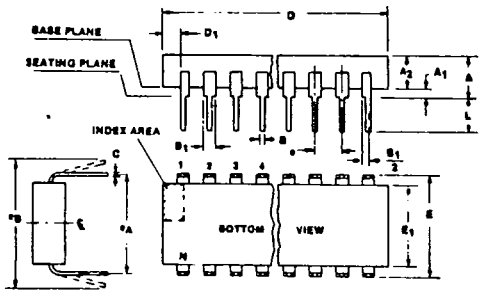


	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

Dual-In-Line Plastic Packages

T-90-20



(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

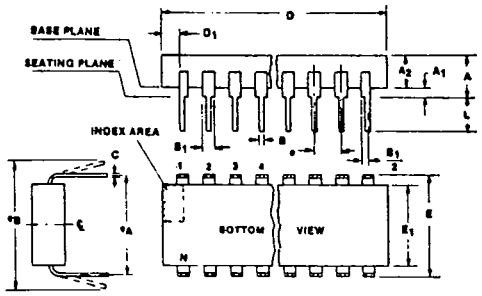
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

   $1, N, \frac{N}{2}, \frac{N}{2}+1.$

4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

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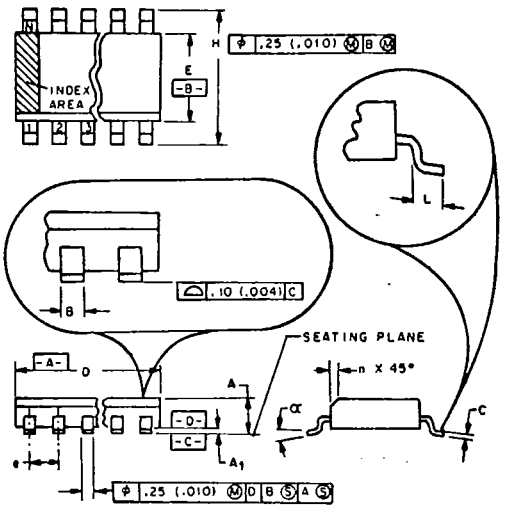
Dual-In-Line Small-Outline Plastic Packages

T-90-20



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

M Suffix (JEDEC MS-012AB)
14-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38924R2

M Suffix (JEDEC MS-012AC)
16-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38925R2

M Suffix (JEDEC MS-013AC)
20-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38926R2

M Suffix (JEDEC MS-013AD)
24-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

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