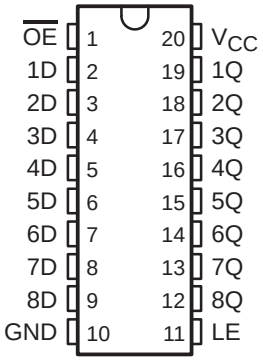
- **2-V to 6-V V_{CC} Operation Range**
- **Wide Operating Temperature Range of –55°C to 125°C**
- **3-State Outputs Directly Drive Bus Lines**
- **Balanced Propagation Delays and Transition Times**
- **Standard Outputs Drive up to 10 LS-TTL Loads**
- **Significant Power Reduction Compared to LS-TTL Logic ICs**

CD54HC573 . . . F PACKAGE
CD74HC573 . . . E OR M PACKAGE
(TOP VIEW)



description

The ’HC573 devices are octal transparent D-type latches designed for 2-V to 6-V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74HC573E	CD74HC573E
	SOIC – M	Tube	CD74HC573M	HC573M
		Tape and reel	CD74HC573M96	
	CDIP – F	Tube	CD54HC573F	CD54HC573F
		Tube	CD54HC573F3A	CD54HC573F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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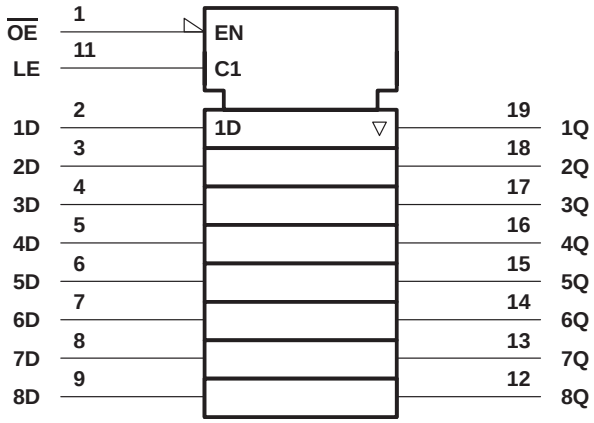
FUNCTION TABLE
(each latch)

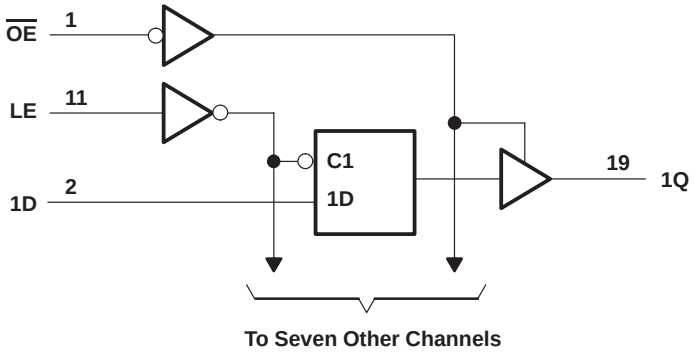
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output drain current per output, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous output source or sink current per output, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): E package . . . . . 80°C/W
M package . . . . . 86°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V		1000	ns
		V_{CC} = 4.5 V		500	
		V_{CC} = 6 V		400	
T_A	Operating free-air temperature		–55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		T_A = –40°C TO 85°C		T_A = –55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9		1.9		1.9		V
			4.5 V	4.4		4.4		4.4		
			6 V	5.9		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98		3.84		3.7		
		I_{OH} = –7.8 mA	6 V	5.48		5.34		5.2		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.1		0.1		0.1	V
			4.5 V		0.1		0.1		0.1	
			6 V		0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.26		0.33		0.4	
		I_{OL} = 7.8 mA	6 V		0.26		0.33		0.4	
I_I	V_I = V_{CC} or 0		6 V		±0.1		±1		±1	μA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.5		±5		±10	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V		8		80		160	μA
C_i					10		10		10	pF
C_o					20		20		20	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V_{CC}	T_A = 25°C		T_A = –40°C TO 85°C		T_A = –55°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		100		120		ns
		4.5 V	16		20		24		
		6 V	14		17		20		
t_{su}	Setup time, data before LE↓	2 V	50		65		75		ns
		4.5 V	10		13		15		
		6 V	9		11		13		
t_h	Hold time, data after LE↓	2 V	40		50		60		ns
		4.5 V	8		10		12		
		6 V	7		9		10		

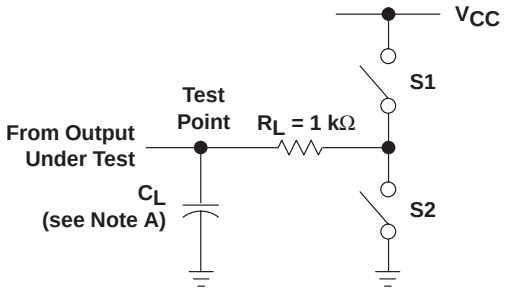
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C		T_A = –40°C TO 85°C		T_A = –55°C TO 125°C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 50 pF	2 V		175		220		265	ns
				4.5 V		35		44		53	
				6 V		30		37		45	
	LE	Q	C_L = 50 pF	2 V		175		220		265	
				4.5 V		35		44		53	
				6 V		30		37		45	
t_{en}	$\overline{OE}$	Q	C_L = 50 pF	2 V		150		190		225	ns
				4.5 V		30		38		45	
				6 V		26		33		38	
t_{dis}	$\overline{OE}$	Q	C_L = 50 pF	2 V		150		190		225	ns
				4.5 V		30		38		45	
				6 V		26		33		38	
t_t		Q	C_L = 50 pF	2 V		60		75		90	ns
				4.5 V		12		15		18	
				6 V		10		13		15	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

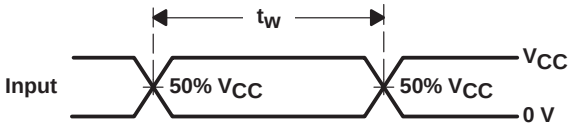
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	51	pF

PARAMETER MEASUREMENT INFORMATION

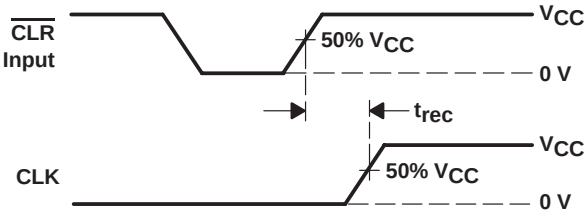


LOAD CIRCUIT

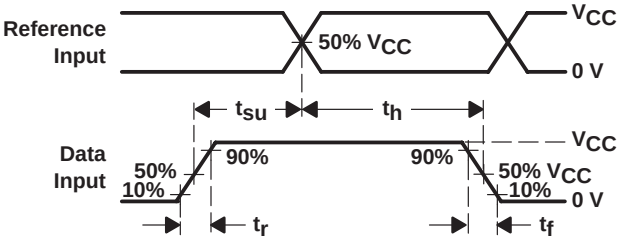
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



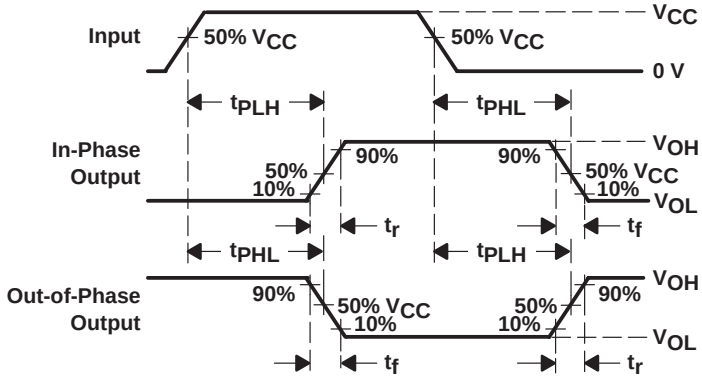
VOLTAGE WAVEFORMS
PULSE DURATION



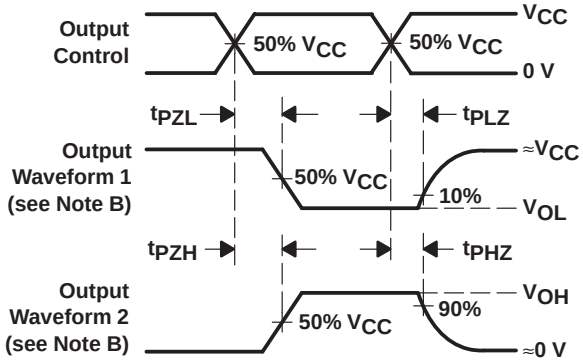
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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