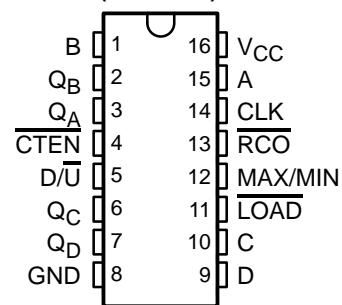


CD54HC190, CD74HC190 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

- 2-V to 6-V V_{CC} Operation ('HC190, 191)
- 4.5-V to 5.5-V V_{CC} Operation ('HCT191)
- Wide Operating Temperature Range of -55°C to 125°C
- Synchronous Counting and Asynchronous Loading
- Two Outputs for n-Bit Cascading
- Look-Ahead Carry for High-Speed Counting
- Balanced Propagation Delays and Transition Times
- Standard Outputs Drive Up To 15 LS-TTL Loads
- Significant Power Reduction Compared to LS-TTL Logic ICs

CD54HC190, 191; CD54HCT191 . . . F PACKAGE
CD74HC190 . . . E OR M PACKAGE
CD74HC191, CD74HCT191 . . . E PACKAGE
(TOP VIEW)



description/ordering information

The CD54/74HC190 are asynchronously presettable BCD decade counters, whereas the CD54/74HC191 and CD54/74HCT191 are asynchronously presettable binary counters.

Presetting the counter to the number on preset data inputs (A–D) is accomplished by a low asynchronous parallel load ($\overline{\text{LOAD}}$) input. Counting occurs when $\overline{\text{LOAD}}$ is high, count enable ($\overline{\text{CTEN}}$) is low, and the down/up ($\text{D}/\overline{\text{U}}$) input is either high for down counting or low for up counting. The counter is decremented or incremented synchronously with the low-to-high transition of the clock.

When an overflow or underflow of the counter occurs, the MAX/MIN output, which is low during counting, goes high and remains high for one clock cycle. This output can be used for look-ahead carry in high-speed cascading (see Figure 1). The MAX/MIN output also initiates the ripple clock ($\overline{\text{RCO}}$) output, which is normally high, goes low and remains low for the low-level portion of the clock pulse. These counters can be cascaded using $\overline{\text{RCO}}$ (see Figure 2).

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it returns to the normal sequence in one or two counts, as shown in the state diagrams (see Figure 3).

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	PDIP – E	Tube	CD74HC190E	CD74HC190E
			CD74HC191E	CD74HC191E
			CD74HCT191E	CD74HCT191E
	SOIC – M	Tube	CD74HC190M	HC190M
		Tape and reel	CD74HC190M96	
	CDIP – F	Tube	CD54HC190F3A	CD54HC190F3A
			CD54HC191F3A	CD54HC191F3A
			CD54HCT191F3A	CD54HCT191F3A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

CD54HC190, CD74HC190
CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

FUNCTION TABLE

INPUTS				FUNCTION
LOAD	CTEN	D/U	CLK	
H	L	L	┐	Count up
H	L	H	┐	Count down
L	X	X	X	Asynchronous preset
H	H	X	X	No change

D/U or CTEN should be changed only when clock is high.

X = Don't care

┐ Low-to-high clock transition

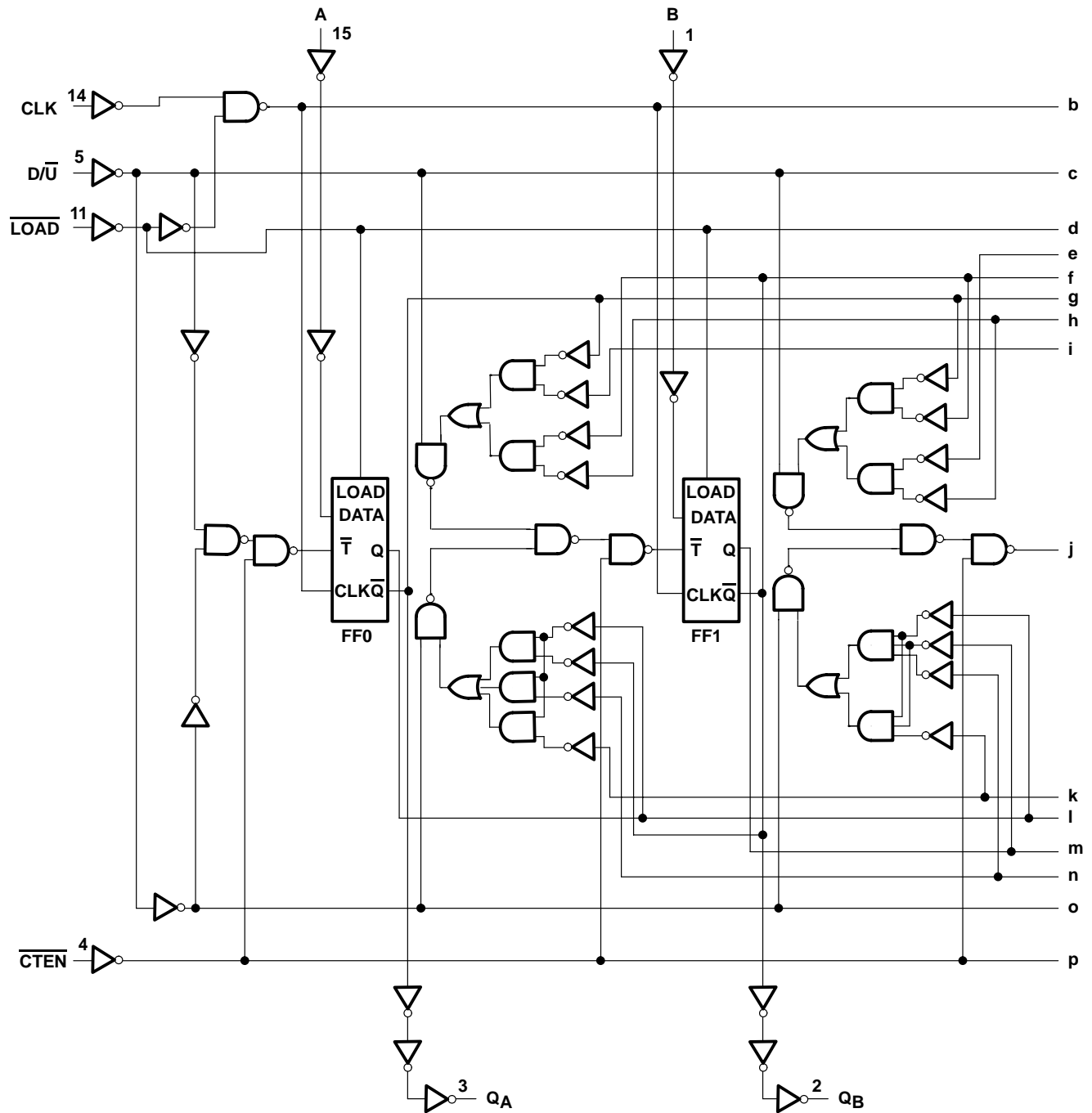


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CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

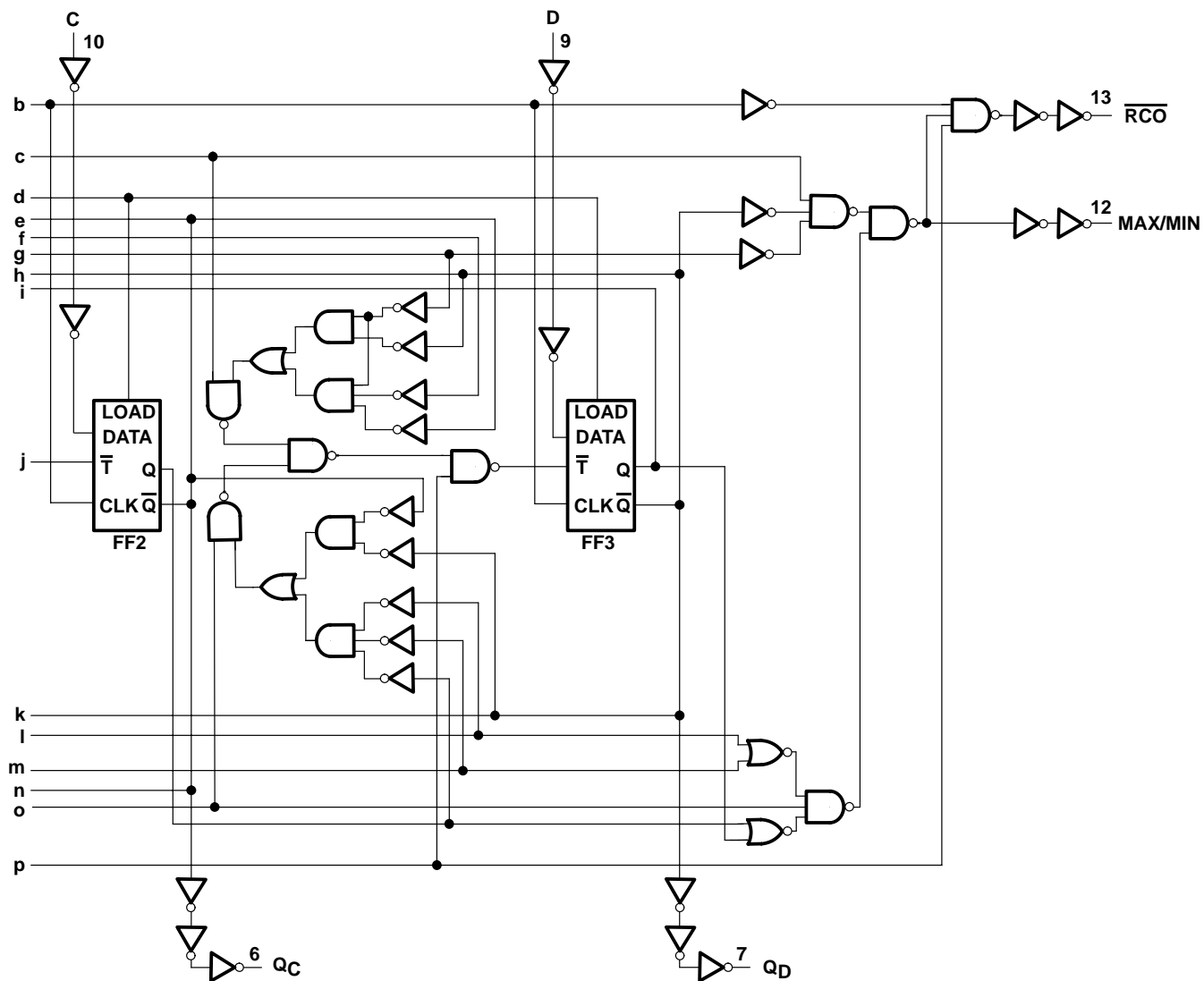
'HC190 logic diagram



**CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

SCHS275C – MARCH 2002 – REVISED MAY 2003

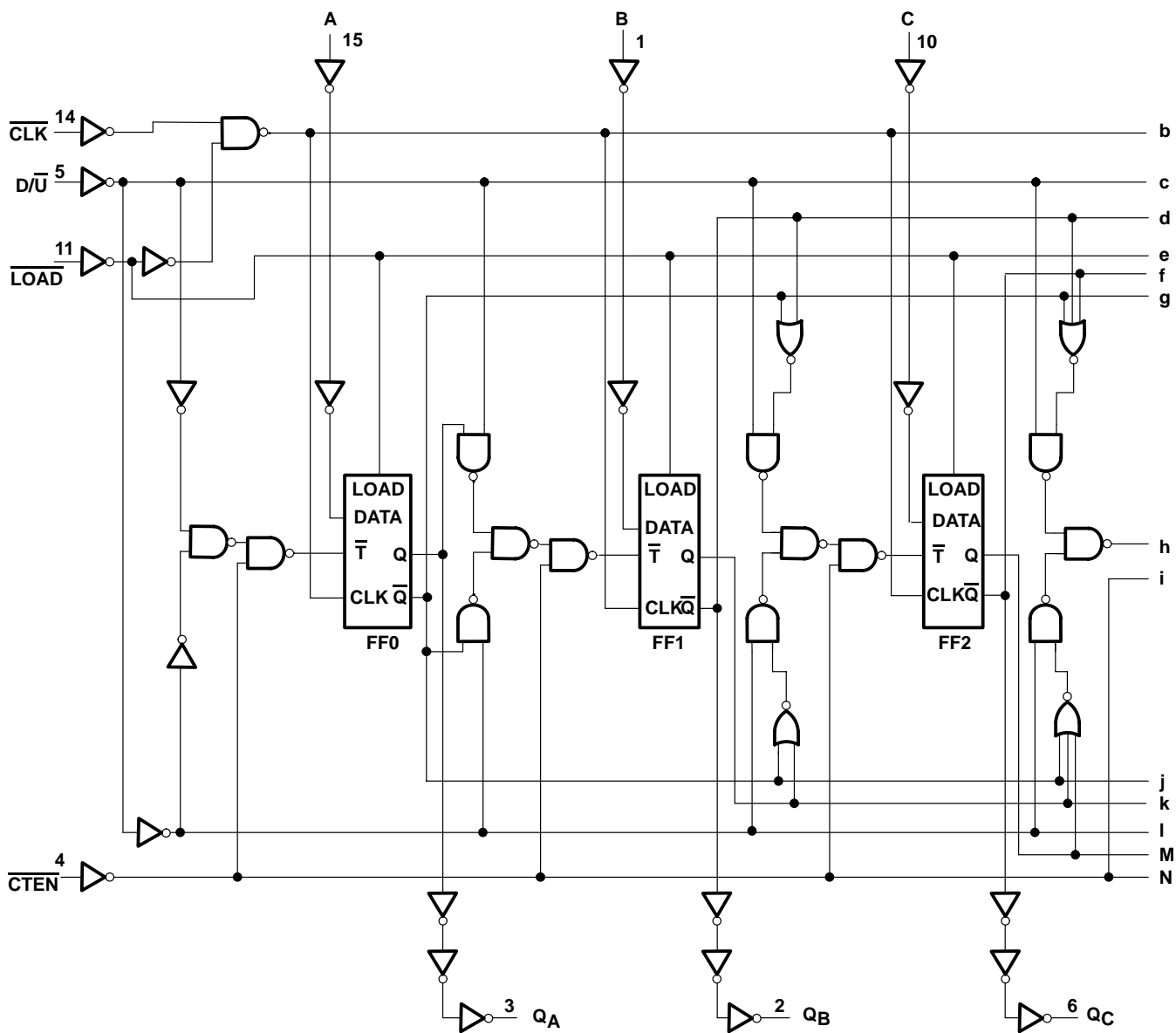
'HC190 logic diagram (continued)



CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

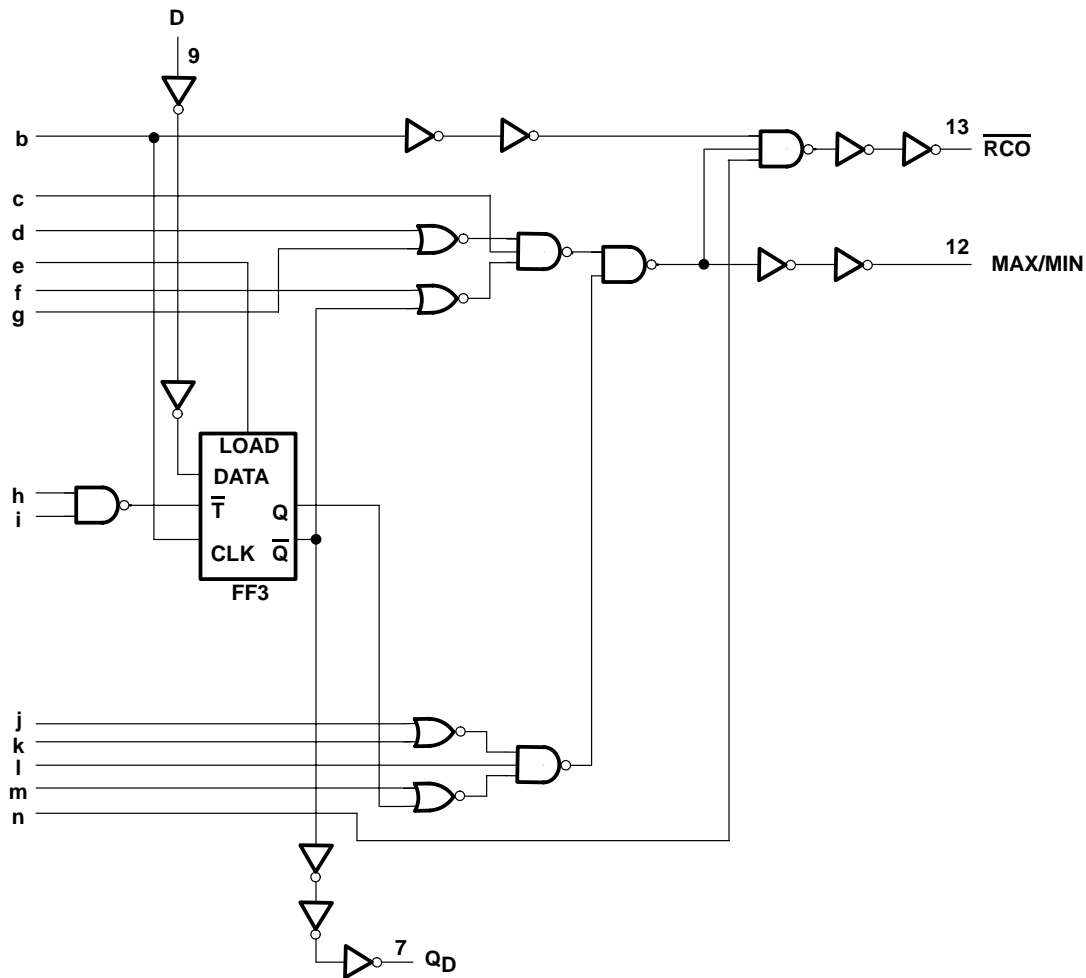
'HC191, 'HCT191 logic diagram



CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

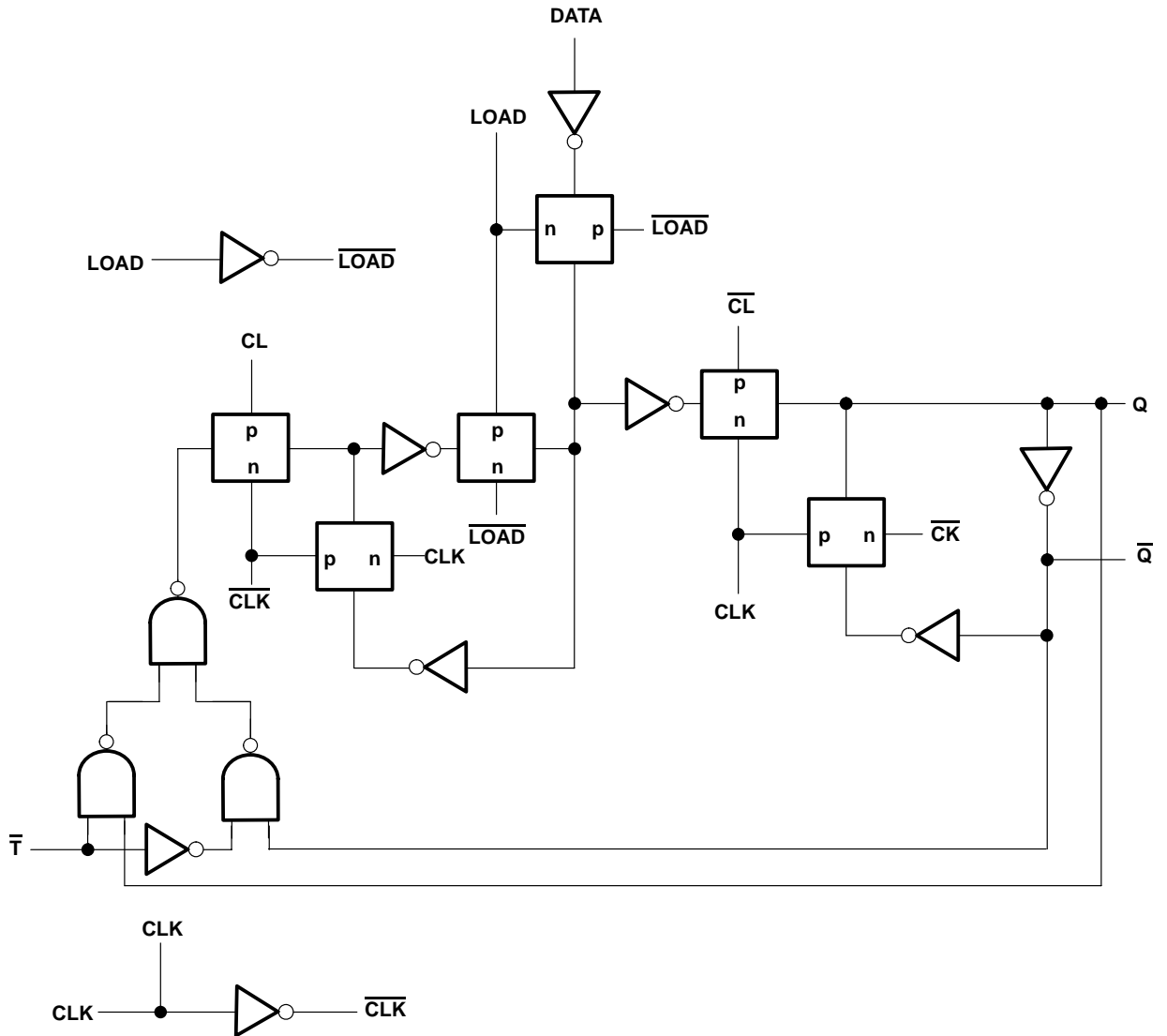
'HC191, 'HCT191 logic diagram (continued)



CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

'HC190 and 'HC191/HCT191 flip-flop



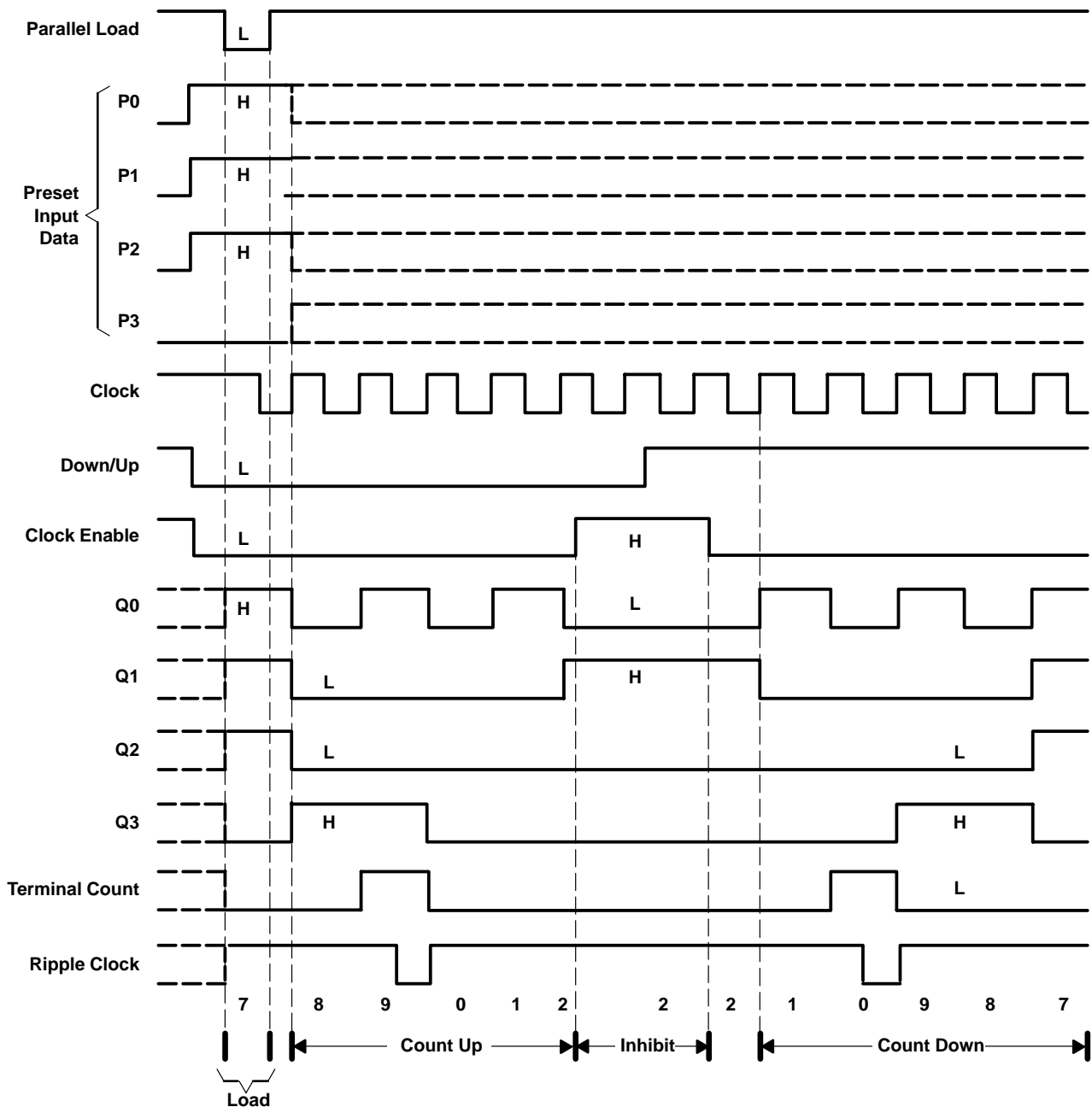
**CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL**

SCHS275C – MARCH 2002 – REVISED MAY 2003

typical load, count, and inhibit sequence for 'HC190

The following sequence is illustrated below:

1. Load (preset) to BCD 7
2. Count up to 8, 9 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 9, 8, and 7



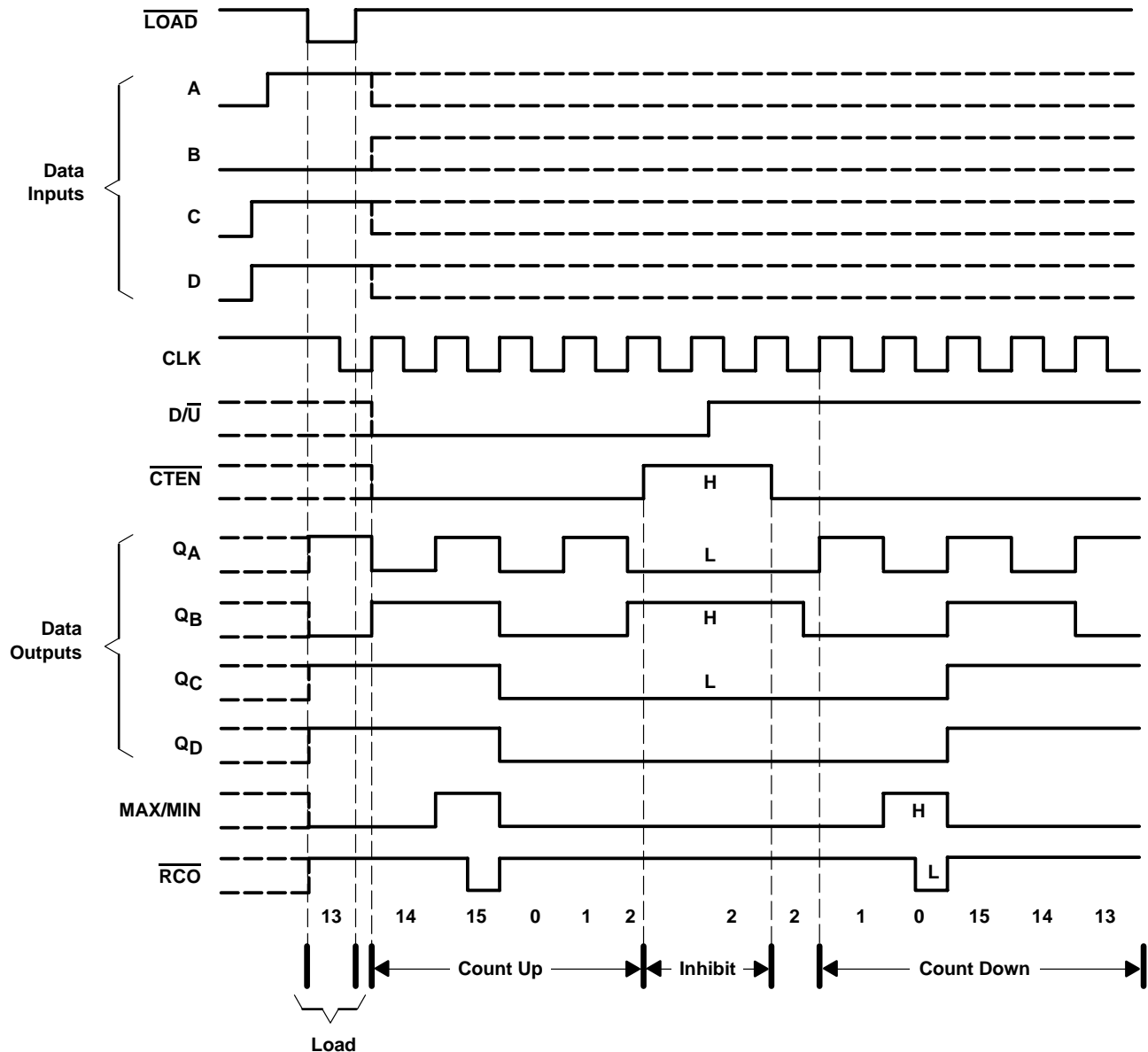
CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

typical load, count, and inhibit sequence for 'HC191 and 'HCT191

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL
 SCHS275C – MARCH 2002 – REVISED MAY 2003

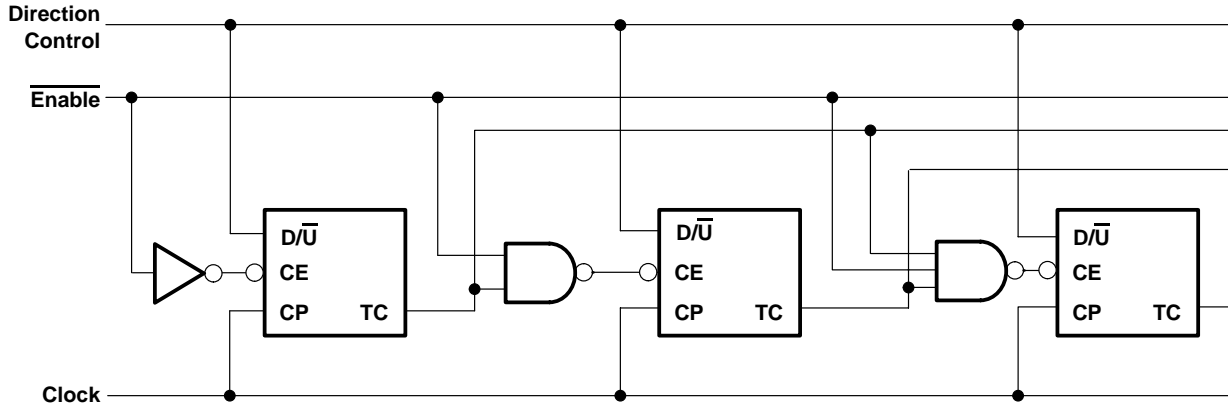


Figure 1. 'HC190 Synchronous n-Stage Counter With Parallel Gated Terminal Count

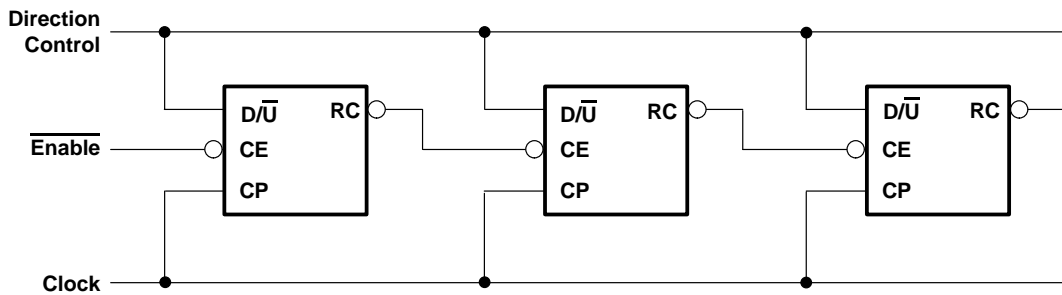
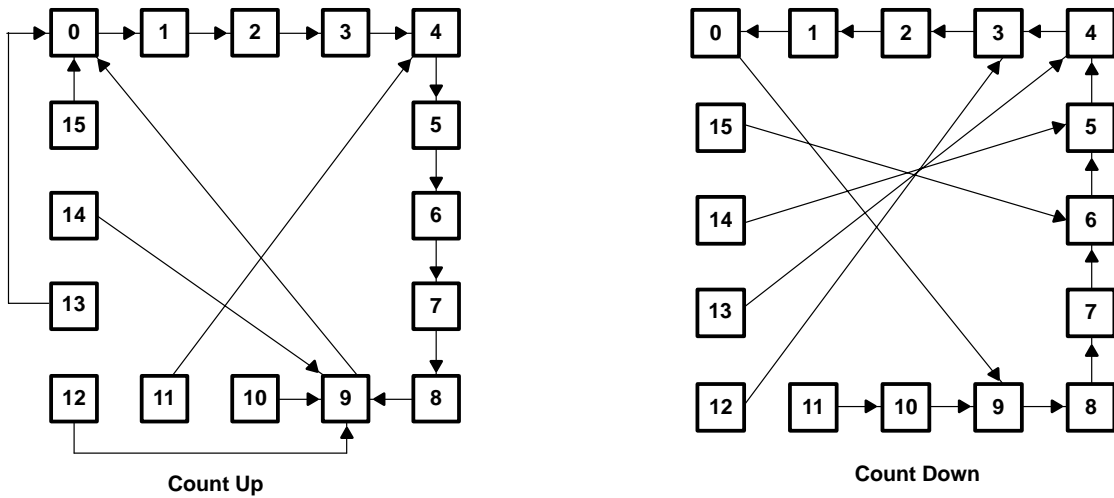


Figure 2. 'HC191, 'HCT191 Synchronous n-Stage Counter With Parallel Gated Terminal Count



NOTE: Illegal states in BCD counters corrected in one count

NOTE: Illegal states in BCD counters corrected in one or two counts

Figure 3. 'HC190 State Diagram

CD54HC190, CD74HC190
CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output drain current per output, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous output source or sink current per output, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions for 'HC190 and 'HC191 (see Note 3)

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	6	2	6	2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$		1.5	1.5	1.5		V
		$V_{CC} = 4.5\text{ V}$		3.15	3.15	3.15		
		$V_{CC} = 6\text{ V}$		4.2	4.2	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5		0.5		V
		$V_{CC} = 4.5\text{ V}$		1.35		1.35		
		$V_{CC} = 6\text{ V}$		1.8		1.8		
V_I	Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2\text{ V}$		1000		1000		ns
		$V_{CC} = 4.5\text{ V}$		500		500		
		$V_{CC} = 6\text{ V}$		400		400		

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for 'HCT191 (see Note 4)

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		0.8		V
V_I	Input voltage	V_{CC}		V_{CC}		V_{CC}		V
V_O	Output voltage	V_{CC}		V_{CC}		V_{CC}		V
t_t	Input transition (rise and fall) time	500		500		500		ns

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



CD54HC190, CD74HC190
CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

'HC190, 'HC191

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C		T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.9	1.9			V	
			4.5 V	4.4	4.4	4.4				
			6 V	5.9	5.9	5.9				
		I _{OH} = -4 mA	4.5 V	3.98	3.7	3.84				
		I _{OH} = -5.2 mA	6 V	5.48	5.2	5.34				
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.1	0.1	0.1			V	
			4.5 V	0.1	0.1	0.1				
			6 V	0.1	0.1	0.1				
		I _{OL} = 4 mA	4.5 V	0.26	0.4	0.33				
		I _{OL} = 5.2 mA	6 V	0.26	0.4	0.33				
I _I	V _I = V _{CC} or 0		6 V	±0.1		±1		±1		μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V	8		160		80		μA
C _i				10		10		10		pF

'HCT191

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4			4.4		4.4	V	
		I _{OH} = -4 mA		3.98			3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5 V			0.1		0.1		V	
		I _{OL} = 4 mA				0.26		0.4			0.33
I _I	V _I = V _{CC} to GND		5.5 V			±0.1		±1		μA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		5.5 V			8		160		μA	
ΔI _{CC} †	One input at V _{CC} - 2.1 V, Other inputs at 0 or V _{CC}		4.5 V to 5.5 V		100	360		490		450	μA
C _i						10		10		10	pF

† Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

HCT INPUT LOADING TABLE

INPUTS	UNIT LOADS
A-D	0.4
CLK	1.5
$\overline{\text{LOAD}}$	1.5
$\overline{\text{D/U}}$	1.2
$\overline{\text{CTEN}}$	1.5

Unit load is ΔI_{CC} limit specified in electrical characteristics table, (e.g., 360 μA max at 25°C).



CD54HC190, CD74HC190
CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

'HC190, 'HC191 timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

		V _{CC}	T _A = 25°C		T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency†	2 V	6		4		5		MHz
		4.5 V	30		20		25		
		6 V	35		23		29		
t _w	$\overline{\text{LOAD}}$ low	2 V	80	120		100		ns	
		4.5 V	16	24		20			
		6 V	14	20		17			
	CLK high or low	2 V	100	150		125			
		4.5 V	20	30		25			
		6 V	17	26		21			
t _{su}	Data before $\overline{\text{LOAD}}\uparrow$	2 V	60	90		75		ns	
		4.5 V	12	18		15			
		6 V	10	15		13			
	$\overline{\text{CTEN}}$ before CLK \uparrow	2 V	60	90		75			
		4.5 V	12	18		15			
		6 V	10	15		13			
	D/ $\overline{\text{U}}$ before CLK \uparrow	2 V	90	135		115			
		4.5 V	18	27		23			
		6 V	15	23		20			
t _h	Data before $\overline{\text{LOAD}}\uparrow$	2 V	2	2		2		ns	
		4.5 V	2	2		2			
		6 V	2	2		2			
	$\overline{\text{CTEN}}$ before CLK \uparrow	2 V	2	2		2			
		4.5 V	2	2		2			
		6 V	2	2		2			
	D/ $\overline{\text{U}}$ before CLK \uparrow	2 V	0	0		0			
		4.5 V	0	0		0			
		6 V	0	0		0			
t _{rec}	$\overline{\text{LOAD}}$ inactive before CLK \uparrow	2 V	60	90		75		ns	
		4.5 V	12	18		15			
		6 V	10	15		13			

† Applies to noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, $\overline{\text{CTEN}}$ -to-clock setup times, and $\overline{\text{CTEN}}$ -to-clock hold times determine maximum clock frequency. For example, with these HC devices:

$$f_{\text{max}}(\text{CLK}) = \frac{1}{\text{CLK-to-MAX/MIN propagation delay} + \overline{\text{CTEN-to-CLK}} \text{ setup time} + \overline{\text{CTEN-to-CLK}} \text{ hold time}} = \frac{1}{42 + 12 + 2} \approx 18 \text{ MHz}$$



CD54HC190, CD74HC190
CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

'HC190, 'HC191

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -55°C TO 125°C		T _A = -40°C TO 85°C		UNIT						
					MIN	TYP	MAX	MIN	MAX	MIN	MAX							
f _{max}				2 V	6			4		5	MHz							
				4.5 V	30			20		25								
				6 V	35			23		29								
t _{pd}	$\overline{\text{LOAD}}$	Q	C _L = 50 pF	2 V		195		295		245	ns							
				4.5 V		39		59		49								
				6 V		33		50		42								
	A, B, C, or D	Q	C _L = 50 pF	2 V		175		265		220								
				4.5 V		35		53		44								
				6 V		30		45		37								
	CLK	Q	C _L = 50 pF	2 V		170		255		215								
				4.5 V		34		51		43								
				6 V		29		43		37								
	CLK	$\overline{\text{RCO}}$	C _L = 50 pF	2 V		125		190		155								
				4.5 V		25		38		31								
				6 V		21		32		26								
	CLK	MAX/MIN	C _L = 50 pF	2 V		210		315		265								
				4.5 V		42		63		53								
				6 V		36		54		45								
	D/ $\overline{\text{U}}$	$\overline{\text{RCO}}$	C _L = 50 pF	2 V		150		225		190								
				4.5 V		30		45		38								
				6 V		26		38		33								
	D/ $\overline{\text{U}}$	MAX/MIN	C _L = 50 pF	2 V		165		250		205								
				4.5 V		33		50		41								
				6 V		28		43		35								
	$\overline{\text{CTEN}}$	$\overline{\text{RCO}}$	C _L = 50 pF	2 V		125		190		155								
				4.5 V		25		38		31								
				6 V		21		32		26								
	C _L = 15 pF	5 V	16	14	14	10	18	12	10	13								
												2 V		75		110		95
												4.5 V		15		22		19
	6 V	13	19	16														



CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

'HCT191

timing requirements over recommended operating free-air temperature range $V_{CC} = 4.5\text{ V}$ (unless otherwise noted) (see Figure 5)

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	30		20		25		MHz
t_w	Pulse duration	$\overline{\text{LOAD}}$ low		16	24	20		ns
		CLK high or low		20	30	25		
t_{su}	Setup time	Data before $\overline{\text{LOAD}}\uparrow$		12	18	15		ns
		$\overline{\text{CTEN}}$ before $\text{CLK}\uparrow$		12	18	15		
		$\text{D}/\overline{\text{U}}$ before $\text{CLK}\uparrow$		18	27	23		
t_h	Hold time	Data before $\overline{\text{LOAD}}\uparrow$		2	2	2		ns
		$\overline{\text{CTEN}}$ before $\text{CLK}\uparrow$		2	2	2		
		$\text{D}/\overline{\text{U}}$ before $\text{CLK}\uparrow$		0	0	0		
t_{rec}	Recovery time	$\overline{\text{LOAD}}$ inactive before $\text{CLK}\uparrow$		12	18	15		ns

'HCT191

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C}$ TO 125°C		$T_A = -40^\circ\text{C}$ TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}				4.5 V	30			20		25	MHz	
t_{pd}	$\overline{\text{LOAD}}$	Q	$C_L = 50\text{ pF}$	4.5 V		40		60		50	ns	
			$C_L = 15\text{ pF}$	5 V		17						
	A, B, C, or D	Q	$C_L = 50\text{ pF}$	4.5 V		38		57		48		
			$C_L = 15\text{ pF}$	5 V		16						
	CLK	$\overline{\text{RCO}}$	$C_L = 50\text{ pF}$	4.5 V		35		53		44		
			$C_L = 15\text{ pF}$	5 V		14						
	CLK	Q	$C_L = 50\text{ pF}$	4.5 V		27		41		34		
			$C_L = 15\text{ pF}$	5 V		11						
	CLK	MAX/MIN	$C_L = 50\text{ pF}$	4.5 V		42		63		53		
			$C_L = 15\text{ pF}$	5 V		18						
	$\text{D}/\overline{\text{U}}$	$\overline{\text{RCO}}$	$C_L = 50\text{ pF}$	4.5 V		30		45		38		
			$C_L = 15\text{ pF}$	5 V		12						
	$\text{D}/\overline{\text{U}}$	MAX/MIN	$C_L = 50\text{ pF}$	4.5 V		38		57		48		
			$C_L = 15\text{ pF}$	5 V		16						
$\overline{\text{CTEN}}$	$\overline{\text{RCO}}$	$C_L = 50\text{ pF}$	4.5 V		27		41		34			
		$C_L = 15\text{ pF}$	5 V		11							
t_t		Any	$C_L = 50\text{ pF}$	4.5 V		15		22		19	ns	



CD54HC190, CD74HC190
CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

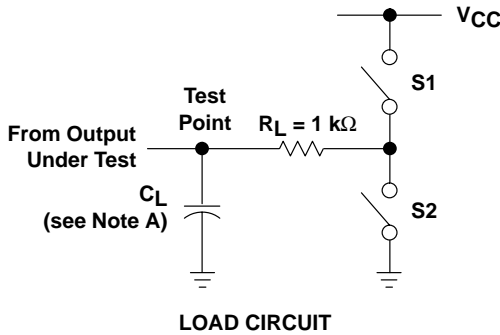
PARAMETER		TYP	UNIT
C_{pd} Power dissipation capacitance	'HC190	59	pF
	'HC191	55	
	'HCT191	68	



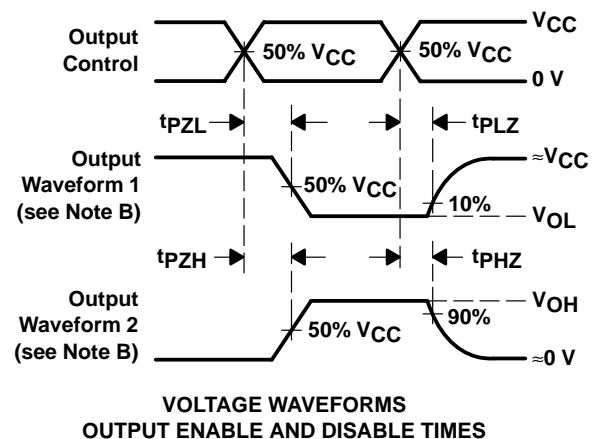
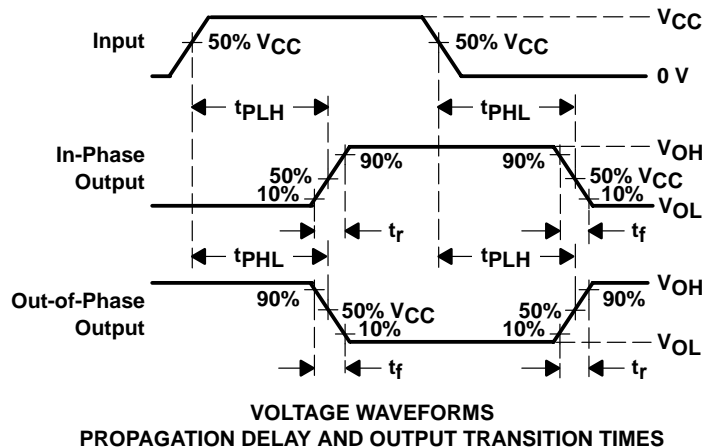
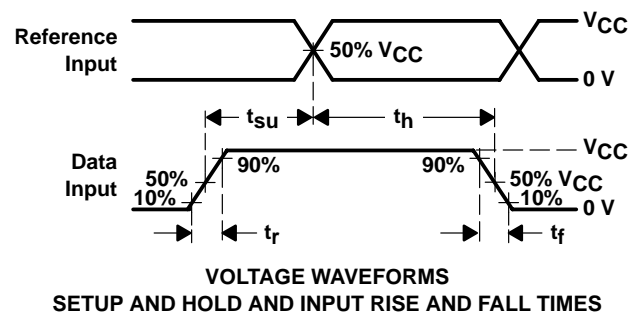
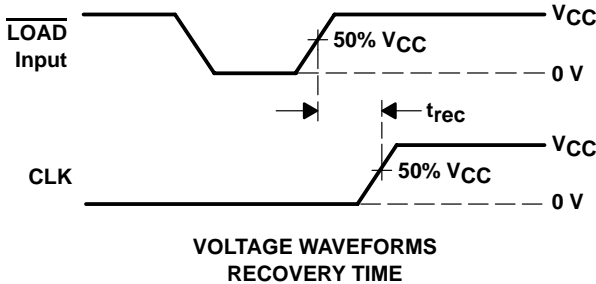
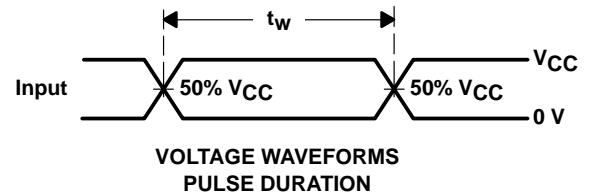
CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

PARAMETER MEASUREMENT INFORMATION – 'HC190, 'HC191



PARAMETER	S1	S2	
t_{en}	t_{pZH}	Open	Closed
	t_{pZL}	Closed	Open
t_{dis}	t_{pHZ}	Open	Closed
	t_{pLZ}	Closed	Open
t_{pd} or t_f	Open	Open	



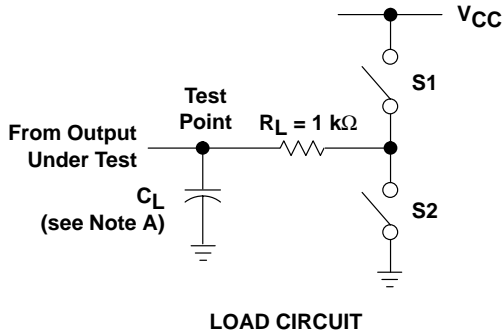
- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - G. t_{pZL} and t_{pZH} are the same as t_{en} .
 - H. t_{pLH} and t_{pHL} are the same as t_{pd} .

Figure 4. Load Circuit and Voltage Waveforms

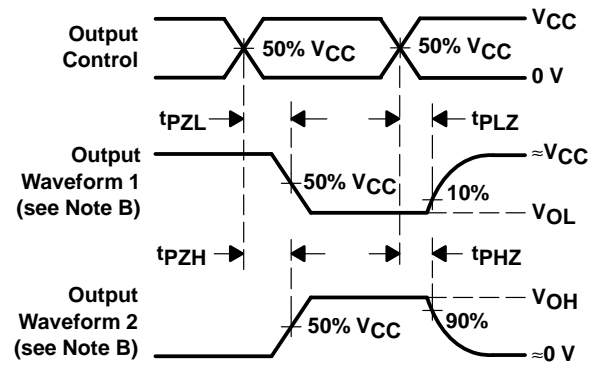
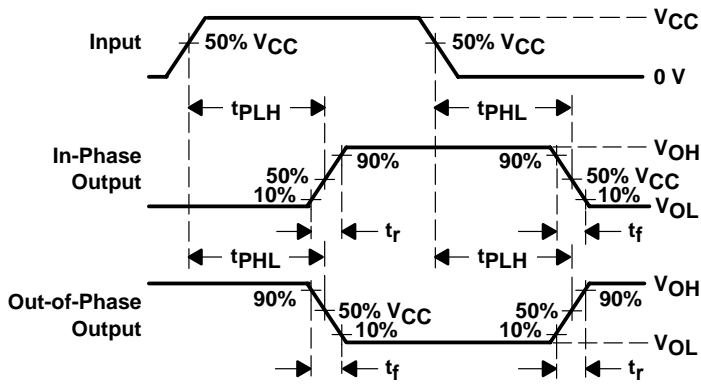
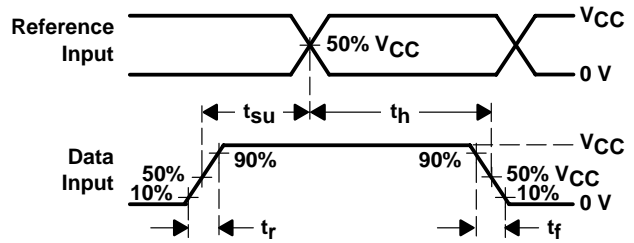
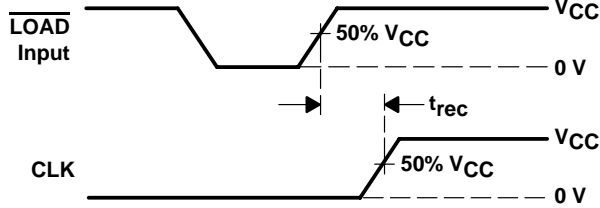
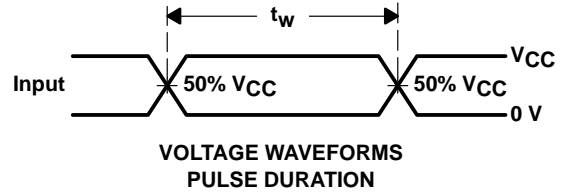
CD54HC190, CD74HC190
 CD54HC191, CD74HC191, CD54HCT191, CD74HCT191
 SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

SCHS275C – MARCH 2002 – REVISED MAY 2003

PARAMETER MEASUREMENT INFORMATION – 'HCT191



PARAMETER	S1	S2	
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t	Open	Open	



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



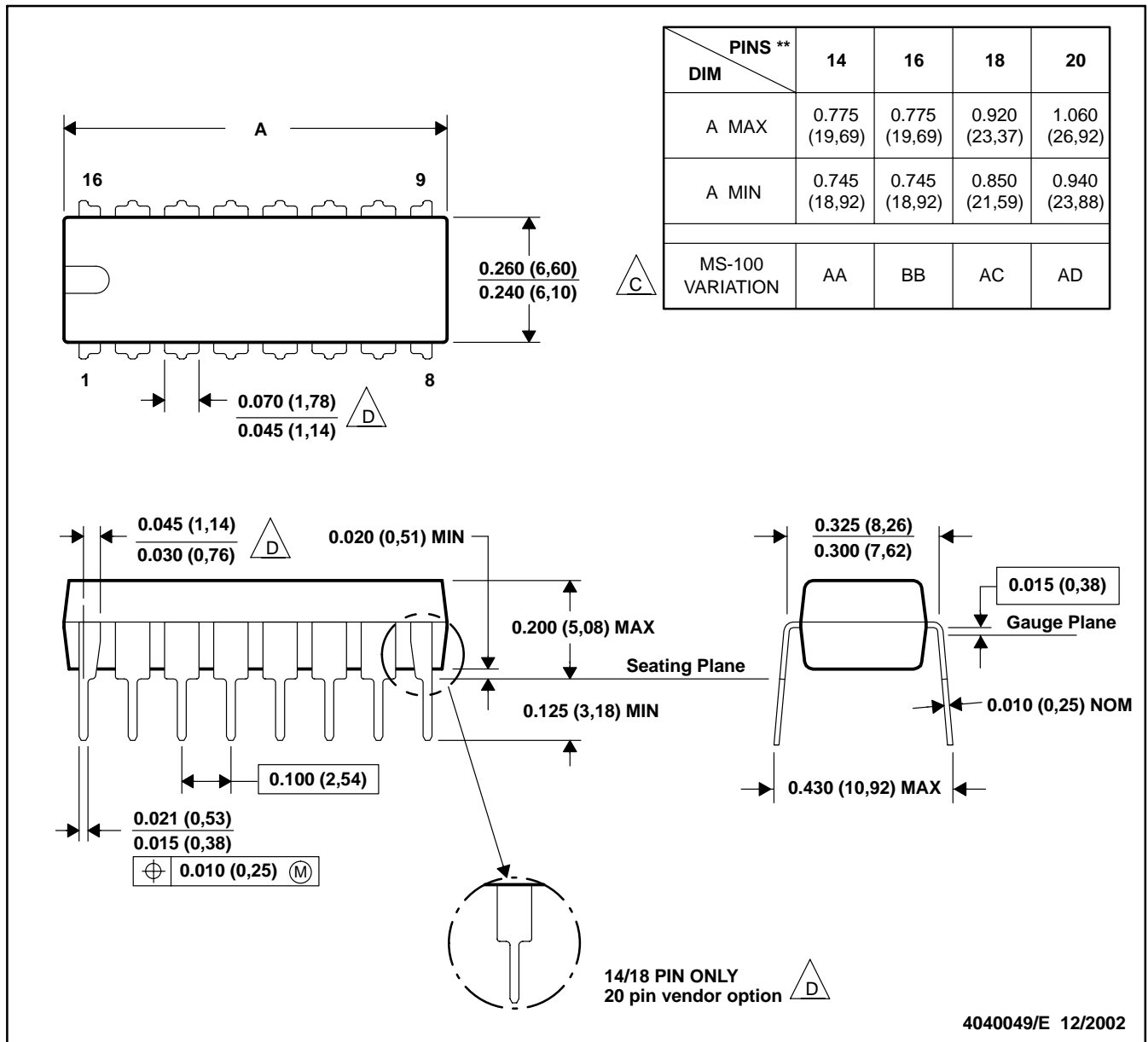
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

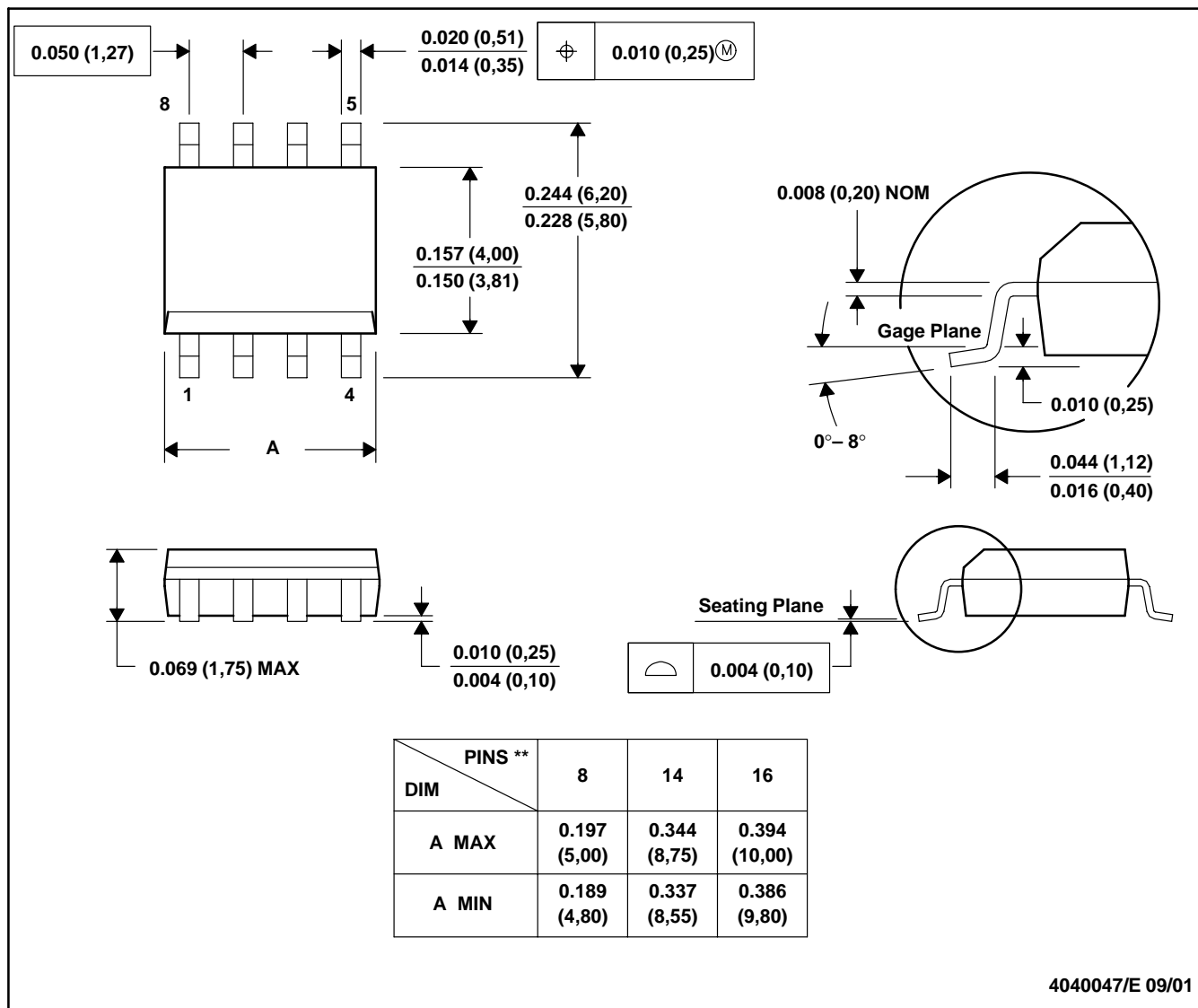


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



4040047/E 09/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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