COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

12-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER

- QUIESCENT CURRENT SPECIFIED TO 15V (see page 10)
- MAX. INPUT LEAKAGE CURRENT 1 μA @ 15V (FULL TEMP. RANGE)
- HIGH NOISE IMMUNITY 45% of V_{DD} (TYP.)
- MEDIUM SPEED OPERATION: 5 MHz (TYP.) INPUT PULSE RATE at V_{DD}-V_{SS}= 10V
- LOW "1" and "0" OUTPUT LEVEL IMPEDANCE: 750Ω (TYP.) at V_{DD}-V_{SS}= 10V and V_{DS}= 0.5V
- FULLY STATIC OPERATION
- ALL 12 BUFFERED OUTPUTS AVAILABLE
- LOW-POWER TTL COMPATIBLE
- COMMON RESET

The **HBC 4040A** (extended temperature range) and **HBF 4040A** (standard temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. **HBC/HBF 4040A** consists of an input-pulse-shaping circuit and 12 ripple-carry binary counter stages. Resetting the counter to the all 0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse. All inputs and outputs are fully buffered.

ABSOLUTE MAXIMUM RATINGS

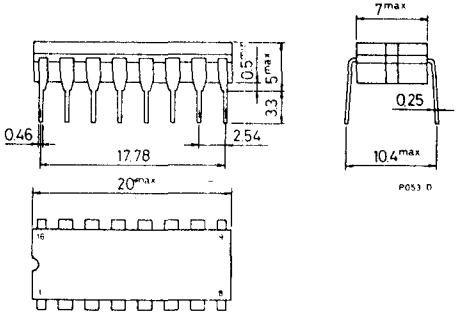
V_{DD}-V_{SS}	Supply voltage	-0.5 to 15 V
V_I	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package)	200 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature: for **HBC** types	-55 to 125 °C
	for **HBF** types	-40 to 85 °C

ORDERING NUMBERS:

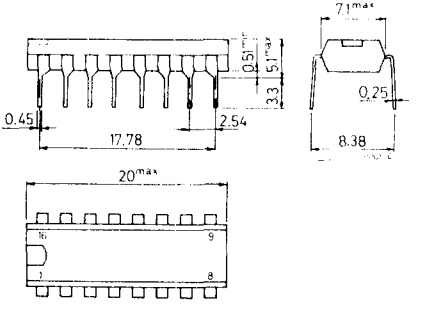
HBC 4040 AD for dual in-line ceramic package
HBC 4040 AF for dual in-line ceramic package, frit seal (extended temperature range)
HBC 4040 AK for ceramic flat package
HBF 4040 AE for dual-line plastic package
HBF 4040 AF for dual in-line ceramic package, frit seal (standard temperature range)

MECHANICAL DATA (dimensions in mm)

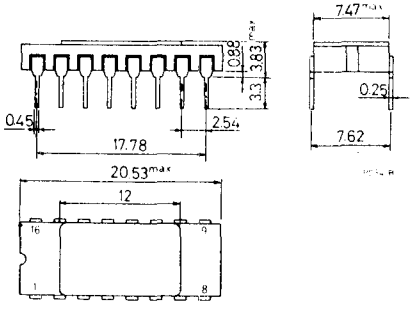
Dual in-line ceramic package
for HBC/HBF 4040 AF



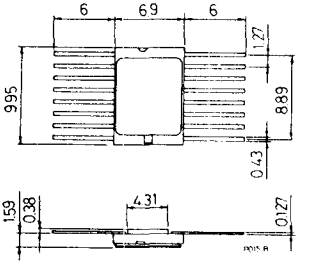
Dual in-line plastic package
for HBF 4040 AE



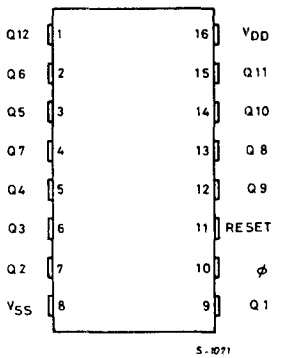
Dual in-line ceramic package
for HBC 4040 AD



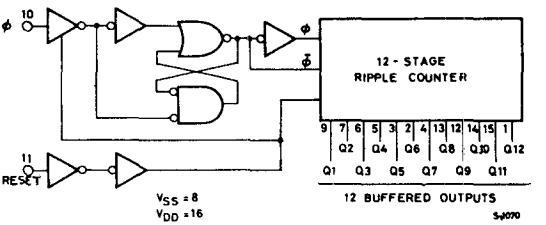
Ceramic flat package
for HBC 4040 AK



CONNECTION DIAGRAM

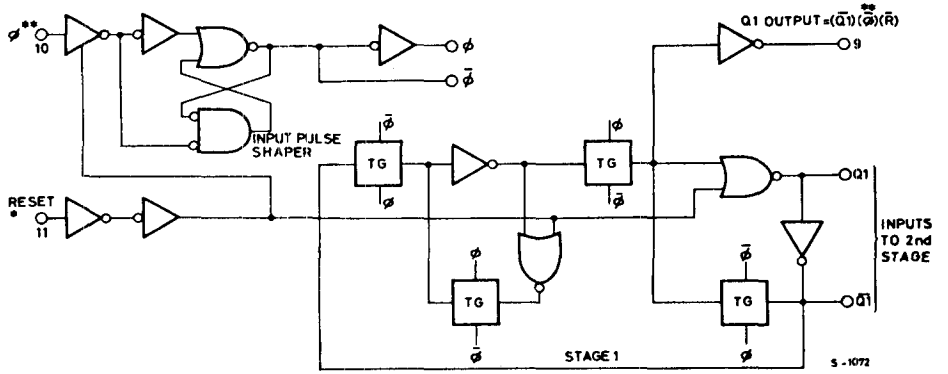


BLOCK DIAGRAM



LOGIC DIAGRAM

Input pulse shaper and 1 of 12 stages

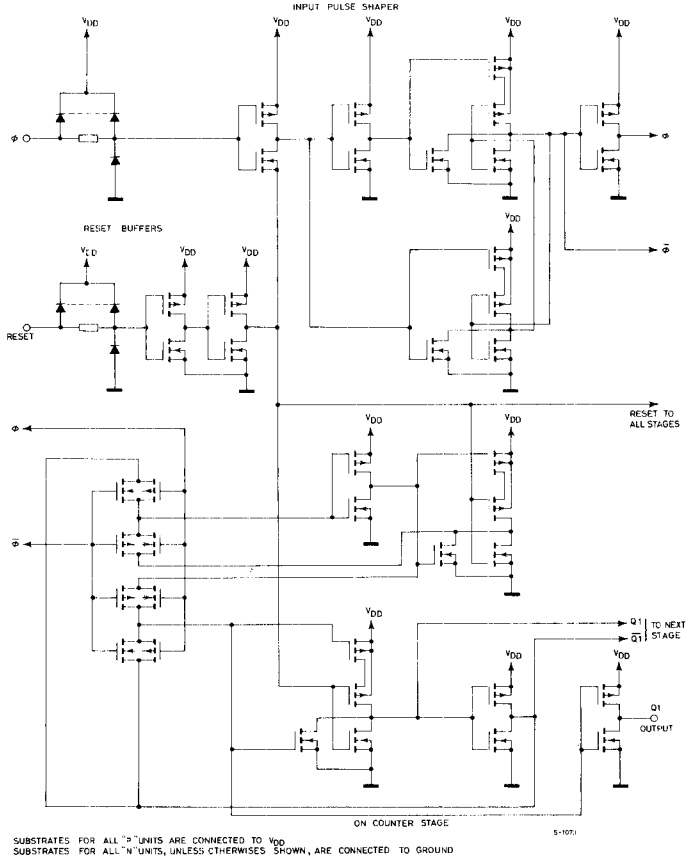


* R-HIGH DOMINATES (RESETS ALL STAGES)

** ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE, COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE ϕ TRANSITION (4096 TOTAL BINARY COUNTS)

SCHEMATIC DIAGRAM

Input shaping, reset buffers, and one counter stage



RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage		3 to 15	V
V_i*	Input voltage		V_{DD} to V_{SS}	
T_{op}	Operating temperature:	for **HBC** types	-55 to 125	°C
		for **HBF** types	-40 to 85	°C

*This is measured with respect to the V_{SS} pin voltage

STATIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
HBC types (extended temperature range)						
I_L	Quiescent current (for values at 15V see page 10)	V_{DD} = 5V				
		at T_{amb} = -55°C			15	μA
		at T_{amb} = 25°C		0.5	15	μA
		at T_{amb} = 125°C			900	μA
		V_{DD} = 10V				
		at T_{amb} = -55°C			25	μA
		at T_{amb} = 25°C		1	25	μA
		at T_{amb} = 125°C			1500	μA
V_{OH}	Output high voltage	Fanout of 50 COS/MOS inputs				
		V_{DD} = 5V				
		at T_{amb} = -55°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 125°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -55°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 125°C	9.95			V
V_{OL}	Output low voltage	Fanout of 50 COS/MOS inputs				
		V_{DD} = 5V or 10V				
		at T_{amb} = -55°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 125°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb} = -55°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 125°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb} = -55°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 125°C	3			V

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions		Min.	Typ.	Max.	Unit
V_{NL}	Noise immunity	V_{DD}= 5V	V_o = 0.8V				
			at T_{amb}= -55°C	1.5			V
			at T_{amb}= 25°C	1.5	2.25		V
			at T_{amb}= 125°C	1.4			V
		V_{DD}= 10V	V_o = 1V				
			at T_{amb}= -55°C	3			V
			at T_{amb}= 25°C	3		4.5	V
			at T_{amb}= 125°C	2.9			V
I_DN	Output drive current N-channel	V_{DD}= 5V	V_o = 0.5V				
			at T_{amb}= -55°C	0.22			mA
			at T_{amb}= 25°C	0.145	0.36		mA
			at T_{amb}= 125°C	0.102			mA
		V_{DD}= 10V	V_o = 0.5V				
			at T_{amb}= -55°C	0.44			mA
			at T_{amb}= 25°C	0.4	0.75		mA
			at T_{amb}= 125°C	0.250			mA
I_DP	Output drive current P-channel	V_{DD}= 5V	V_o = 4.5V				
			at T_{amb}= -55°C	-0.15			mA
			at T_{amb}= 25°C	-01	-0.25		mA
			at T_{amb}= 125°C	-0.07			mA
		V_{DD}= 10V	V_o = 9.5V				
			at T_{amb}= -55°C	-0.3			mA
			at T_{amb}= 25°C	-0.25	-0.5		mA
			at T_{amb}= 125°C	-0.175			mA
I_{IH}, I_{IL}	Input leakage current	V_{DD}= 15V (any input)			$\pm10^{-5}$	±1	μA

HBF types (standard temperature range)

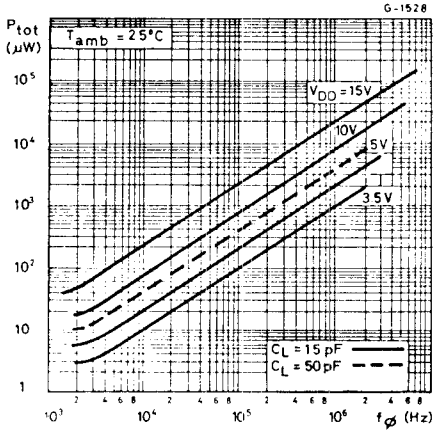
I_L	Quiescent current (for values at 15V see page 10)	V_{DD}= 5V					
			at T_{amb}= -40°C			50	μA
			at T_{amb}= 25°C		1	50	μA
			at T_{amb}= 85°C			700	μA
		V_{DD}= 10V					
			at T_{amb}= -40°C			100	μA
			at T_{amb}= 25°C		2	100	μA
			at T_{amb}= 85°C			1400	μA

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{OH}	Output high voltage	V_{DD} = 5V				
		at T_{amb} = -40°C	4.99			V
		at T_{amb} = 25°C	4.99	5		V
		at T_{amb} = 85°C	4.95			V
		V_{DD} = 10V				
		at T_{amb} = -40°C	9.99			V
		at T_{amb} = 25°C	9.99	10		V
		at T_{amb} = 85°C	9.95			V
V_{OL}	Output low voltage	Fanout of 50 COS/MOS inputs				
		V_{DD} = 5V or 10V				
		at T_{amb} = -40°C			0.01	V
		at T_{amb} = 25°C		0	0.01	V
		at T_{amb} = 85°C			0.05	V
V_{NH}	Noise immunity	V_{DD} = 5V V_o = 4.2V				
		at T_{amb} = -40°C	1.4			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 85°C	1.5			V
		V_{DD} = 10V V_o = 9V				
		at T_{amb} = -40°C	2.9			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 85°C	3			V
V_{NL}	Noise immunity	V_{DD} = 5V V_o = 0.8V				
		at T_{amb} = -40°C	1.5			V
		at T_{amb} = 25°C	1.5	2.25		V
		at T_{amb} = 85°C	1.4			V
		V_{DD} = 10V V_o = 1V				
		at T_{amb} = -40°C	3			V
		at T_{amb} = 25°C	3	4.5		V
		at T_{amb} = 85°C	2.9			V
I_DN	Output drive current N-channel	V_{DD} = 5V V_o = 0.5V				
		at T_{amb} = -40°C	0.21			mA
		at T_{amb} = 25°C	0.056	0.08		mA
		at T_{amb} = 85°C	0.15			mA

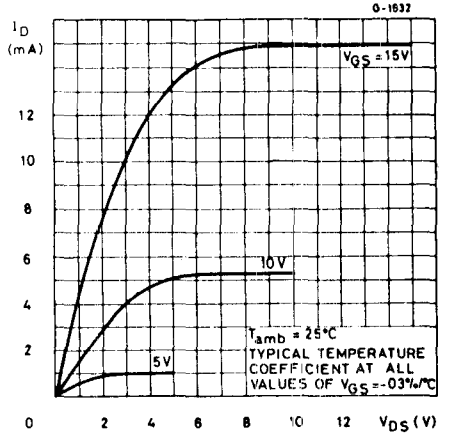
STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
I_DN	Output drive current N-channel	V_{DD}= 10V V_o = 0.5V				
		at T_{amb}= -40°C		0.42		mA
		at T_{amb}= 25°C		0.2	0.75	mA
		at T_{amb}= 85°C		0.14		mA
I_DP	Output drive current P-channel	V_{DD}= 5V V_o = 4.5V				
		at T_{amb}= -40°C		-0.45		mA
		at T_{amb}= 25°C		-0.06	-0.25	mA
		at T_{amb}= 85°C		-0.04		mA
		V_{DD}=10V V_o = 9.5V				
		at T_{amb}= -40°C		-0.29		mA
		at T_{amb}= 25°C		-0.15	-0.5	mA
		at T_{amb}= 85°C		-0.1		mA
I_{IH}, I_{IL}	Input leakage current	V_{DD}= 15V (any input)		$\pm 10^{-5}$	±1	μA

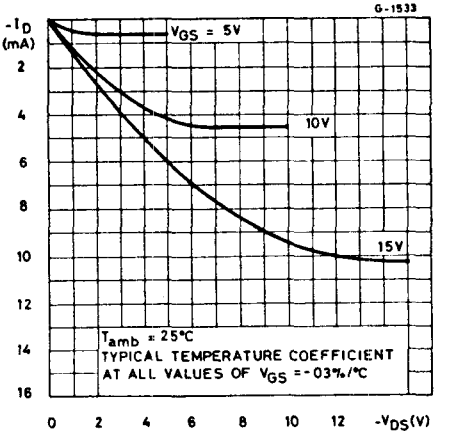


Typical power dissipation characteristics

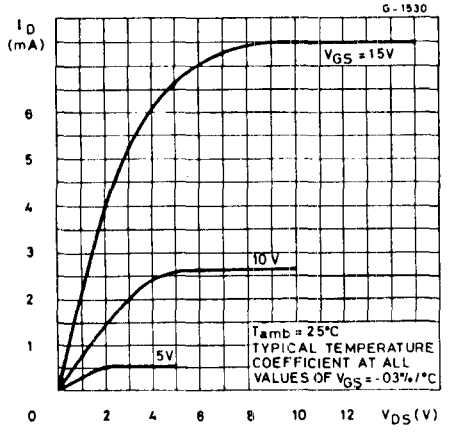
Typical N-channel drain characteristics



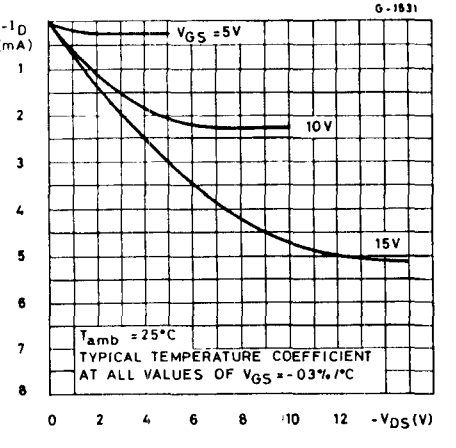
Typical P-channel drain characteristics



Minimum N-channel drain characteristics



Minimum P-channel drain characteristics



DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns, except $t_{\phi r}$ and $t_{\phi f}$)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT PULSE OPERATION					
t_{PLH},* t_{PHL} Propagation delay time	V_{DD} = 5V				
	for **HBC** types		450	900	ns
	for **HBF** types		450	950	ns
	V_{DD} = 10V				
	for **HBC** types		225	450	ns
	for **HBF** types		225	475	ns
t_{TLH}, t_{THL} Transition time	V_{DD} = 5V				
	for **HBC** types		150	300	ns
	for **HBF** types		150	350	ns
	V_{DD} = 10V				
	for **HBC** types		75	150	ns
	for **HBF** types		75	175	ns
t_{pwH}, t_{pwL} Minimum input pulse width	V_{DD} = 5V				
	for **HBC** types		200	400	ns
	for **HBF** types		200	500	ns
	V_{DD} = 10V				
	for **HBC** types		75	110	ns
	for **HBF** types		75	125	ns
$t_{\phi r}$,** $t_{\phi f}$ Clock rise and fall time	V_{DD} = 5V				
	for **HBC** types			15	μs
	for **HBF** types			15	μs
	V_{DD} = 10V				
	for **HBC** types			7.5	μs
	for **HBF** types			7.5	μs
f_{max} Maximum input pulse frequency	V_{DD} = 5V				
	for **HBC** types	1	1.75		MHz
	for **HBF** types	0.9	1.75		MHz
	V_{DD} = 10V				
	for **HBC** types	3.5	5		MHz
	for **HBF** types	3.25	5		MHz
C_i Input capacitance	Any input for **HBC** and **HBF** types		5		pF

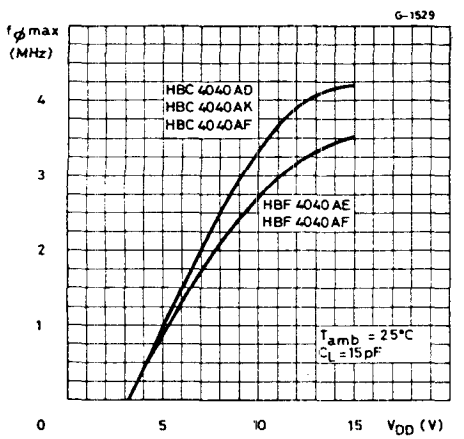
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
RESET OPERATION					
t_{PHL} Propagation delay time	V_{DD} = 5V				
	for **HBC** types		500	1000	ns
	for **HBF** types		500	1250	ns
	V_{DD} = 10V				
	for **HBC** types		250	500	ns
	for **HBF** types		250	600	ns
t_{pwH}*** Minimum reset pulse width	V_{DD} = 5V				
	for **HBC** types		500	1000	ns
	for **HBF** types		500	1250	ns
	V_{DD} = 10V				
	for **HBC** types		250	500	ns
	for **HBF** types		250	600	ns

* Measured from the 50% level of the negative clock edge to the 50% level of either the positive or negative edge of the Q1 output (pin 9); or measured from the negative edge of Q1 through Q11 outputs to the positive or negative edge of the next higher output.

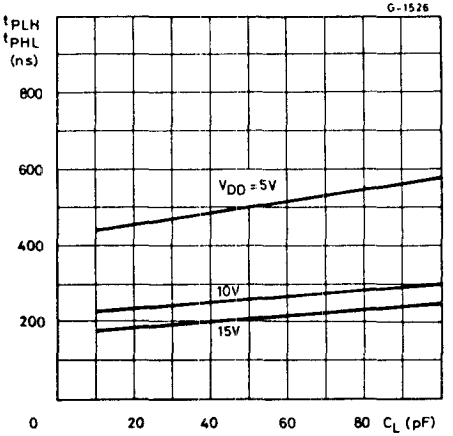
** Maximum input rise or fall time for functional operation.

*** Measured from the positive edge of the reset pulse to the negative edge of any output (Q1 to Q12).



Maximum input pulse frequency vs. supply voltage

Typical propagation delay time vs. load capacitance (per stage)



Typical transition time vs. load capacitance