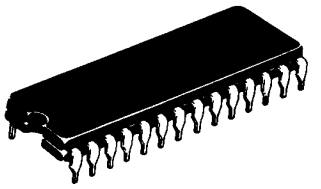
HMCS42(HD38702)

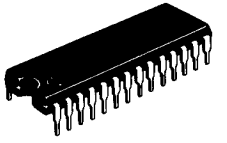
The HMCS42 is the PMOS 4-bit single chip microcomputer which contains ROM, RAM and I/O on single chip. The HMCS42 is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The PMOS technology of the HMCS42 provides high voltage I/O capability for direct driving vacuum-fluorescent display.

HMCS42



(DP-28)

HMCS42

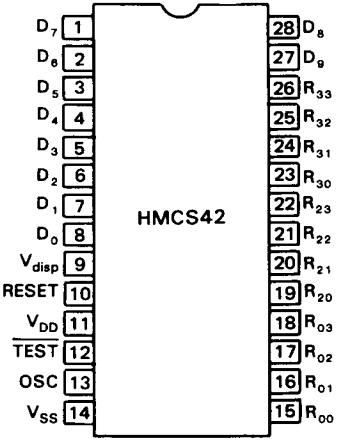


(DP-28S)

■ **FEATURES**

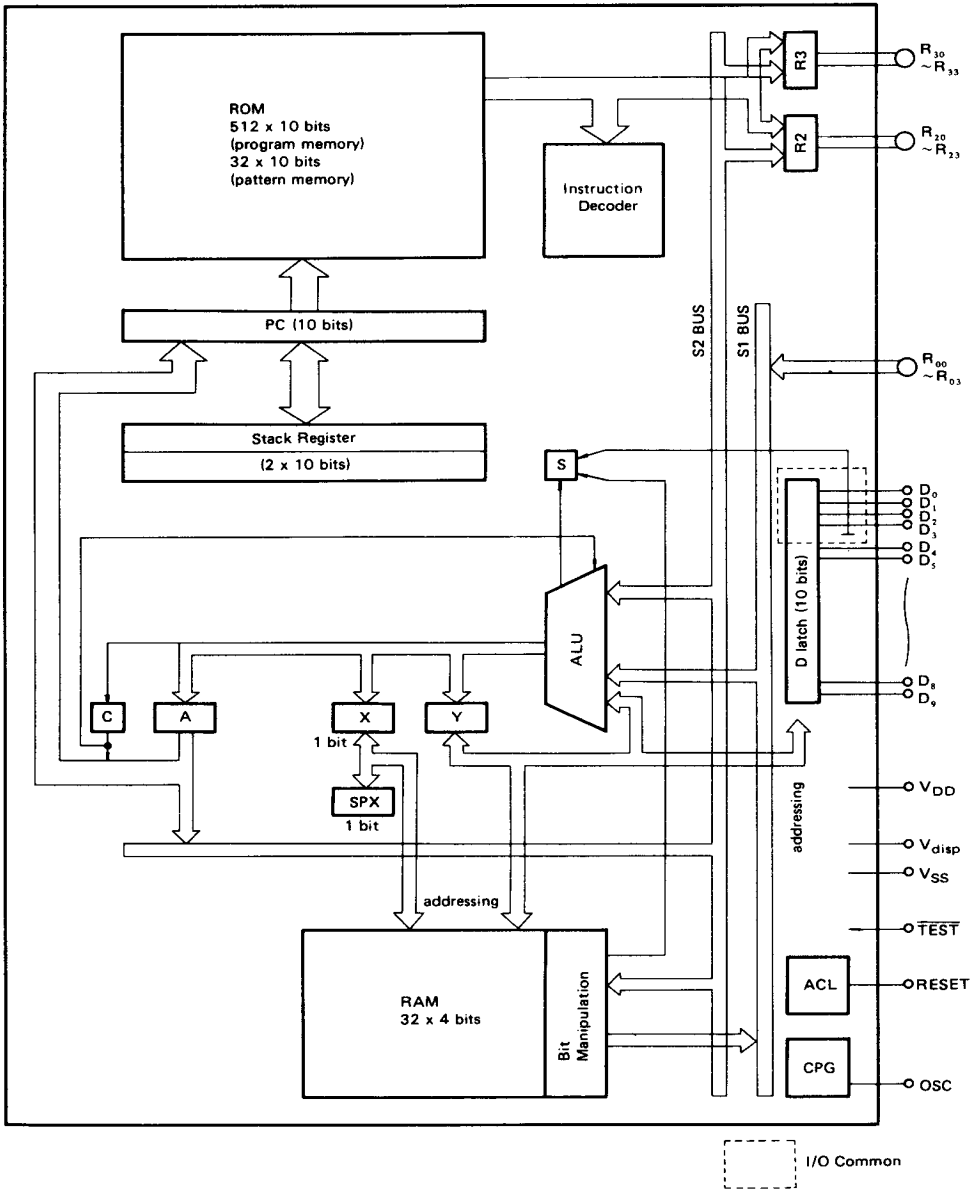
- 4-bit Architecture
- 512 Words of Program ROM (10 bits/Word)
  32 Words of Pattern ROM (10 bits/Word)
- 32 Digits of Data RAM (4 bits/Digit)
- 22 I/O Lines
- 10 μsec Instruction Cycle Time
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  — Table Look Up Capability —
- Bit Manipulation Instructions for Both RAM and I/O
- High Voltage I/O Capability, −49V max.
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or Open Drain
- Built-in RC Oscillator
- Built-in Power-on Reset Circuit
- PMOS Technology
- Single, −10V Power Supply

■ **PIN ARRANGEMENT**



(Top View)

■ BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Remarks
Pin Voltage (1)	$-V_{T1}$	−0.3 to +18	V	Except for pins specified by $-V_{T2}$
Pin Voltage (2)	$-V_{T2}$	−0.3 to +50	V	Applied to high break-down voltage pins [Note 3]
Maximum Power Consumption	P_C	400	mW	
Maximum Total Output Current	$-\Sigma I_o$	45	mA	[Note 4]
Operating Temperature	T_{opr}	−20 to +75	°C	
Storage Temperature	T_{stg}	−55 to +125	°C	

[NOTE 1] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could affect reliability of LSI.
[NOTE 2] All voltages are with respect to V_{SS}.
[NOTE 3] High break-down voltage pins can be specified by user among the following pins. They are specified at ROM ordering using the "Mask Option List". (Unspecified pins are low break-down voltage pins.)
D_0 to D_3, R_{00} to R_{03}, R_{20} to R_{23}, R_{30} to R_{33}, RESET, V_{disp}
Other pins cannot be specified as high break-down voltage pin.
[NOTE 4] Maximum Total Output Current is the total sum of output currents which can flow out simultaneously from output pins and I/O common pins.

■ ELECTRICAL CHARACTERISTICS-1 ($-V_{DD}$=10V±10%, $-V_{disp}$=49V max., Ta=−20 to +75°C)

Item	Symbol	Test Conditions	Value min	Value typ	Value max	Unit	Note
Input "Low" Voltage (1)	$-V_{IL1}$	$-V_{DD}$=9V	4.0	–	49	V	3
		$-V_{DD}$=11V	4.7				
Input "Low" Voltage (2)	$-V_{IL2}$	$-V_{DD}$=9V	4.0	–	49	V	4
		$-V_{DD}$=11V	4.7				
Input "High" Voltage (1)	$-V_{IH1}$		–	–	2.55	V	3
Input "High" Voltage (2)	$-V_{IH2}$		–	–	2.0	V	4
Output "Low" Voltage (1)	$-V_{OL1}$	$-V_{disp}$=49V	45	–	–	V	5
Output "Low" Voltage (2)	$-V_{OL2}$	56kΩ to −49V	45	–	–	V	6
Output "High" Voltage (1)	$-V_{OH1}$	$-I_{OH}$=3mA	–	–	1.8	V	7
Output "High" Voltage (2)	$-V_{OH2}$	$-I_{OH}$=10mA	–	–	1.8	V	8
Input Leakage Current	$-I_{IL}$	$-V_{in}$=0 to 49V	–	–	50	μA	9
Pull up MOS Current	I_P	$-V_{disp}$=45V	100	–	400	μA	2
Supply Current	$-I_{DD}$		–	–	20	mA	
External Clock Operation							
External Clock Frequency	f_{cp}		200	–	440	kHz	
External Clock Duty	Duty		45	50	55	%	
External Clock Rise Time	t_{rcp}		0	–	0.2	μs	
External Clock Fall Time	t_{fcp}		0	–	0.2	μs	
External Clock "Low" Level	$-V_{CPL}$	$-V_{DD}$=9V	4.0	–	17	V	
		$-V_{DD}$=11V	4.7				
External Clock "High" Level	$-V_{CPH}$		–	–	1.0	V	
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{cp}$	9.1	–	20	μs	
Internal Clock Operation (R_f C_f Oscillation)							
Clock Oscillation Frequency	f_{OSC}	R_f=30kΩ±2%, C_f=100pF±5%	320	–	480	kHz	
Instruction Cycle Time	T_{inst}	$T_{inst}=4/f_{OSC}$	8.4	–	12.5	μs	

Specifications of low break-down voltage pins specified by user are as follows.
($-V_{DD}=10V\pm10\%$, $-V_{disp}=17V$ max., Ta = −20 to +75°C)

Item	Symbol	Test Conditions	Value			Unit	Note
			min	typ	max		
Input "Low" Voltage (1)	$-V_{IL1}$	$-V_{DD}=9V$	4.0	—	17	V	3
		$-V_{DD}=11V$	4.7				
Input "Low" Voltage (2)	$-V_{IL2}$	$-V_{DD}=9V$	4.0	—	17	V	4
		$-V_{DD}=11V$	4.7				
Output "Low" Voltage (1)	$-V_{OL1}$	$-V_{disp}=10V$	8.5	—	—	V	5
Output "Low" Voltage (2)	$-V_{OL2}$	56kΩ to −10V	8.5	—	—	V	6
Input Leakage Current	$-I_{IL}$	$-V_{in}=0$ to 17V	—	—	5	μA	9
Pull up MOS Current	I_P	$-V_{disp}=10V$	80	—	350	μA	2

[NOTE 1] All voltages are with respect to V_{SS}.
[NOTE 2] Pull up MOS current (the current which flows in V_{disp} through pull up MOS when the pin is connected to V_{SS}) varies with the value of V_{disp}. It is shown in Figure 1.

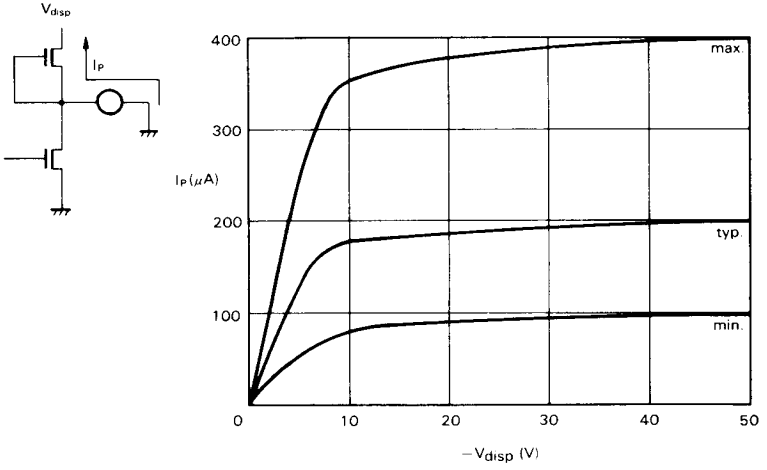

Figure 1 I_P vs. V_{disp}

[NOTE 3] This is applied to D_0 to D_3, R_{00} to R_{03}.
[NOTE 4] This is applied to RESET. The HMCS42 is in the reset state when RESET is at "1" (High) level, and in the operating state at "0" (Low) level. When Built-in Reset is used, RESET should be connected to V_{DD}.
[NOTE 5] This is applied to With Pull up MOS pins.
[NOTE 6] This is applied to No Pull up MOS pins.
[NOTE 7] This is applied to R_{20} to R_{23}, R_{30} to R_{33}.
[NOTE 8] This is applied to D_0 to D_9.
[NOTE 9] Pull up MOS current is excluded.

■ **ELECTRICAL CHARACTERISTICS-2** (Ta = −20 to +75°C)

• **Reset**

Item	Symbol	Test Conditions	Value		Unit
			min	max	
Power Supply Fall Time	t_{fDD}	Built-in Reset	0.1	10	ms
Power Supply OFF Time	t_{OFF}	Built-in Reset	1	–	ms
RESET Pulse Width (1)	t_{RST1}	External Reset −V_{DD}=9 to 11V	1	–	ms
RESET Pulse Width (2)	t_{RST2}	External Reset −V_{DD}=9 to 11V	$2 \cdot T_{inst}$	–	μs
RESET Fall Time	t_{fRST}		–	20	ms
RESET Rise Time	t_{rRST}		–	20	ms

[NOTE] All voltages are with respect to V_{SS}.

■ **SIGNAL DESCRIPTION**

The input and output signals for the HMCS42, shown in PIN ARRANGEMENT, are described in the following paragraphs.

• **V_{DD} and V_{SS}**

Power is supplied to the HMCS42 using these pins. V_{DD} is power of logic parts and V_{SS} is ground connection.

• **V_{disp}**

V_{disp} is used as power supply of Pull up MOS and has no relation to internal logic operation.

• **RESET**

This pin resets the HMCS42 independently of the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS42. The HMCS42 can be reset by pulling RESET high.

Refer to RESET FUNCTION for additional information.

• **OSC**

This pin provides control input for the Built-in oscillator circuit. Resistor, capacitor, and external oscillator can be connected to this pin to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on this pin should be minimized.

Refer to OSCILLATOR for recommendations about this pin.

• **$\overline{TEST}$**

This pin is not for user application and must be connected to V_{SS}.

• **R_{00} to R_{03}**

These 4 lines are arranged into one 4-bit Data Input Channel. It is directly addressed by the operand of input instruction.

Refer to INPUT/OUTPUT for additional information.

• **R_{20} to R_{23}, R_{30} to R_{33}**

These 8 lines are arranged into two 4-bit Data Output Channels. The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of output instruction.

Refer to INPUT/OUTPUT for additional information.

• **D_0 to D_3**

These lines are four 1-bit Discrete Input/Output Common pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register. It is also addressed directly by the operand of input/output instruction.

Refer to INPUT/OUTPUT for additional information.

• **D_4 to D_9**

These lines are six 1-bit Discrete Output pins. The 1-bit latches are attached to these pins. Each pin is addressed by the Y register.

Refer to INPUT/OUTPUT for additional information.

■ **ROM**

• **ROM Address Space**

ROM is used as program and pattern (constants) memory. The instruction used in the HMCS42 consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into the ROM.

The program area is even pages of pages 0 to 14. Therefore, the number of program words is 512 (64×8).

Address 0 to address 15 (decimal) of page 26 and page 30 are the pattern area. Each area is equivalent to 16 words.

In the pattern area, no program can be stored. The area is only used to store patterns (constants) that are referred in programs. In the program area, also patterns can be stored.

The ROM address space is shown in Figure 2.

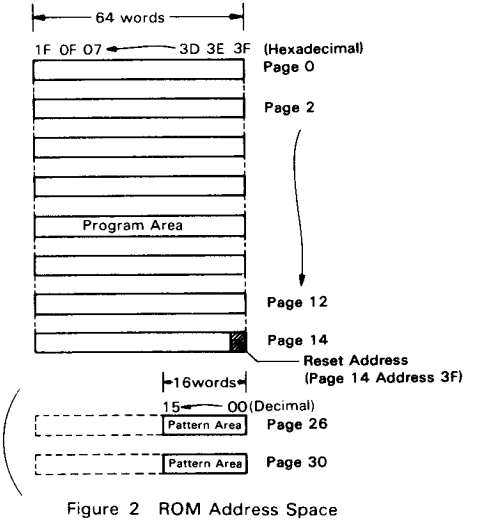

Figure 2 ROM Address Space

- **Program Counter (PC)**

The program counter is used for addressing the program area. It consists of the page part and the address part as shown in Figure 3.

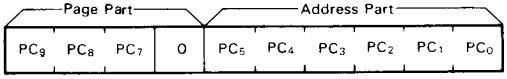

Figure 3 Configuration of Program Counter

Once a certain value is loaded into a page part, it is unchanged until other value is loaded by the program. Any even number among 0 to 14 can be set in the page part.

The address part consists of a random sequential counter and this counter counts up for each instruction cycle. All instructions except the pattern instruction are executed in one cycle. While the pattern instruction is executed in two cycles. The sequence indicated in decimal and hexadecimal is shown in Table 1. This sequence forms a loop and has neither the starting nor ending points. It generates no overflow carry. Therefore, instructions on a same page are executed in order unless the contents of the page part is unchanged.

Table 1 Sequence of the PC Address Part

Decimal	Hexadecimal	Decimal	Hexadecimal	Decimal	Hexadecimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

- **Designation of ROM Address and ROM Code**

The page part of the ROM address is represented by decimal and the address part is divided into 2 parts (2 bits and 4 bits) and represented by hexadecimal.

One word (10 bits) is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10}) and represented by hexadecimal.

The examples are shown in Figure 4.

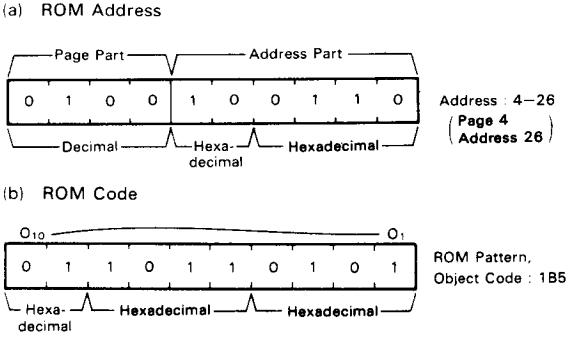

Figure 4 Designation of ROM Address and ROM Code

■ PATTERN GENERATION

The pattern (constants) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

• Reference

ROM addressing for the pattern reference is performed by modifying the program counter with the accumulator, the carry F/F and the operand p. Figure 5 shows how to modify the program counter. The address part is replaced with the accumulator and 0s, while the page part is logically ORed with 0s, C (F/F) and the lower bit of the operand p (p_0). The upper bit (p_1) of the operand is for referring to the pattern area.

Non-existing ROM area can not be referred.

The contents of the PC is only modified apparently and is not changed. Then the address is counted up after the execution of the pattern instruction and next instruction but one is executed. Therefore, the instruction just after the pattern instruction (P) should be NOP.

The pattern instruction is executed in 2 cycles.

• Generation

The bit pattern of referred ROM address is generated by the following two ways.

(i) The pattern is loaded into Accumulator.

(ii)The pattern is loaded into the data I/O registers R2 and R3.

The command bits (O_9, O_{10}) in the pattern determine which way is taken.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and mode (ii) are simultaneously performed when both O_9 and O_{10} are "1".

The correspondence of each bit of the pattern is shown in Figure 6.

CAUTION

In the program execution, the pattern can not be distinguished from the instruction. When the program is running at the address written as a pattern, the instruction corresponding to the pattern bit is executed. Take care not to execute a pattern as an instruction.

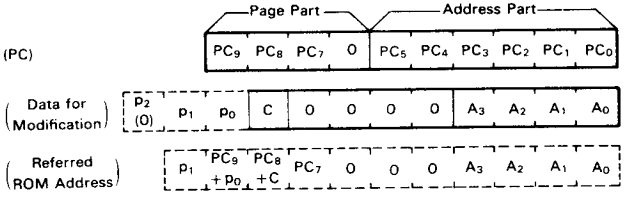

Figure 5 ROM Addressing for Pattern Generation

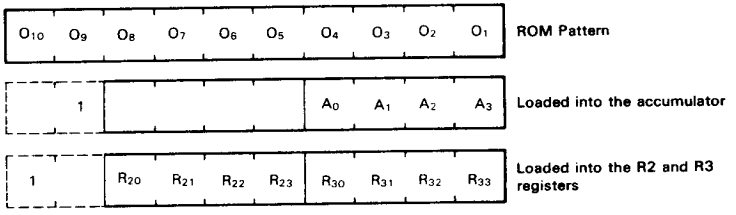

Figure 6 Correspondence of Each Bit of Pattern

Table 2 Examples of how to use Pattern Instruction

Family	Before Execution					Referred ROM Address	Pattern	After Execution				Remark
	PC Value	p	C	B	A			B	A	R2	R3	
HMCS42	0-3F	1	0	/	0	8-00	131	/	8	–	–	
	2-3F	3	1	/	8	30-08	231	/	–	C	8	
	14-00	2	0/1	/	9	30-09	331	/	8	C	8	
	10-01	2	0	/	5	26-05	331	/	8	C	8	
	8-00	2	1	/	5	28-05						not allowable

* "–" means that the value does not change after execution of the instruction.

** "0/1" means that either "0" or "1" may be selected.

*** The value of the PC and the ROM address are divided into the page and the address parts. The page part is represented by decimal and the address part by hexadecimal.

■ BRANCH

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to an optional address out of the sequence, there are four ways.

They are explained in the following paragraphs.

• BR

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM output (operand a, O_6 to O_1) are transferred to the lower 6 bits of the program counter. This instruction is a conditional instruction and executed only when the Status is "1". If it is "0", the instruction is skipped and it becomes "1". The operation is shown in Figure 7.

• LPU

By LPU instruction, a jump between pages is performed.

The lower 4 bits of ROM output are transferred to the page part of the program counter with delay by one-cycle time. Therefore, the cycle just after the issuing of this instruction is on the same page and the page jump is performed at the next cycle.

This instruction is conditional, and is executed only when the Status is "1". But the Status is unchanged (remains "0") even if it is skipped.

LPU instruction is used in combination with BR instruction or CAL instruction as the macro instruction of BRL or CALL instruction.

The LPU operation is shown in Figure 8.

• BRL

By BRL instruction, the program branches to an address in any page.

This is a macro instruction composed of LPU and BR and divided into two steps as follows.

```
                    BRL   a – b → LPU  a
<Jump to address b on page a>     BR   b
```

BRL instruction is a conditional instruction because of its characteristics of LPU and BR instructions, and is executed only when the Status is "1". When the status is "0", this instruction is skipped and the Status becomes "1"

• TBR (Table Branch)

By TBR instruction, the program branches referring to the table.

The program counter is modified by Accumulator, the Carry F/F, and the operand p. Accumulator and 0s are assigned into the address part of the program counter. The 0s, Carry F/F, and the operand p_1, p_0 are logically ORed with the page part of the program counter.

TBR modifies the PC in the same way as the pattern instruction (P) does. The method for modification is shown in Figure 9.

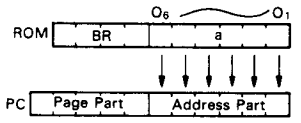

Figure 7 BR Operation

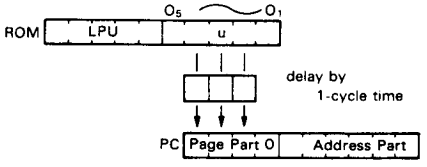

Figure 8 LPU Operation

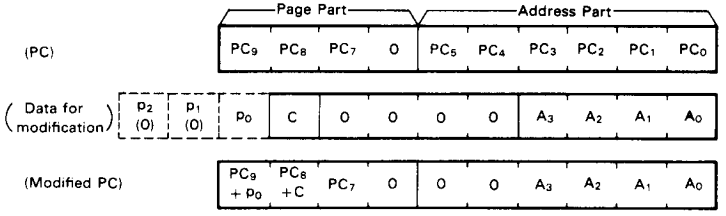

Figure 9 Modification of Program Counter by TBR Instruction

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

• CAL

By CAL instruction, subroutine jump to the Subroutine Space is performed.

The program counter is saved in the following order.

$$PC+1 \rightarrow ST1 \rightarrow ST2$$

The page part of PC is 0. The lower 6 bits of ROM output (operand a, O_6 to O_1) are transferred to the lower 6 bits of the program counter.

CAL instruction is a conditional instruction and executed only when the Status is "1". If it is "0", the instruction is skipped and it becomes "1".

The save condition of the program counter when CAL instruction is executed is shown in Figure 10.

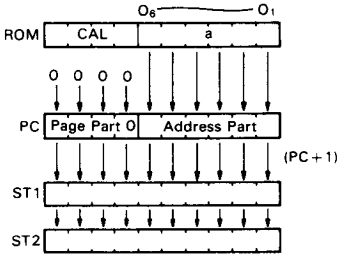

Figure 10 Save Condition of the Program Counter When CAL Instruction is Executed

- **CALL**

By CALL instruction, subroutine jump to an address in any page is performed.

This is a macro instruction of LPU and CAL. The subroutine jump to the page specified by LPU enables the subroutine jump to an optional address.

```
                              CALL  a – b → LPU  a
< Subroutine jump to address b on page a >  CAL  b
```

CALL instruction is conditional because of its characteristics of LPU and CAL instructions and is executed when the Status is "1". If the Status is "0", this instruction is skipped and the Status becomes "1".

■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 32 digits (128 bits) where one digit consists of 4 bits.

RAM is addressed with the matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits, 13 digits (MR0, MR4 to MR15), are called "Memory Register (MR)". The memory register can be exchanged with the accumulator by XAMR instruction.

The RAM address space is shown in Figure 11.

If an instruction consists of a simultaneous read/write operation of RAM (exchange between the contents of RAM and those of the register), the writing data doesn't affect the reading data because read operation precedes write operation.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset, or tested. The bit assignment is specified by the operand n of the instruction.

The bit test makes the Status "1" when the assigned bit is "1" and makes it "0" when the assigned bit is "0".

Correspondence between the RAM bit and the operand n is shown in Figure 12.

X \ Y		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	f \ d	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 ← digit No.
0	0																MR 0
4	4	MR 15	MR 14	MR 13	MR 12	MR 11	MR 10	MR 9	MR 8	MR 7	MR 6	MR 5	MR 4				

↑ file No

Figure 11 RAM Address Space

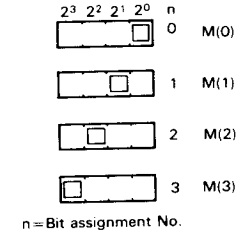

Figure 12 RAM Bit and Operand n

■ REGISTER

The HMCS42 has four registers and two latches available to the programmer. The latches are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

- **Status F/F (S)**

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1".

- **Accumulator (A; A Register) and Carry F/F (C)**

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F respectively. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

- **X Register (X)**

The result of ALU operation (1 bit) is loaded into this register. The X register has exchangeability for the SPX register. It addresses the RAM file and composed of 1-bit (0 or 4) register.

- **SPX Register (SPX)**

The SPX register is exchangeable with the X register.

The SPX register is used to stack the contents of the X register and expand the addressing system of RAM in combination with the X register. It is composed of 1-bit (0 or 4) register.

- **Y Register (Y)**

The result of ALU operation (4 bits) is loaded into this register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digits and 1-bit Discrete I/Os.

■ INPUT/OUTPUT

- **4-bit Data Input/Output Channel (R)**

The HMCS42 has one 4-bit Data Input Channel (R0) and two Data Output Channels (R2, R3).

The 4-bit register is attached to R2 and R3 channels.

Channel addressing is performed by the program. The input instruction inputs 4-bit data into the accumulator (A register) through R0 channel.

The data is transferred from the accumulator to the Data I/O Registers R2 and R3 via the bus lines. ROM bit patterns are loaded into the Data I/O Registers R2 and R3 by the pattern instruction.

The block diagram is shown in Figure 13. The I/O timing is shown in Figure 14.

- **1-bit Discrete Input/Output Pin (D)**

The HMCS42 has ten 1-bit Discrete Pins. The D_0 to D_3 are 1-bit Discrete I/O Common Pins and the D_4 to D_9 are 1-bit Discrete Output Pins.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and level ("0" or "1") of the addressed pin can be tested by an input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch output and the pin input. Therefore, the latch should be reset to "0" not to affect the pin input before execution of input instruction.

The D_0 to D_3 pins are also addressed directly by the operand n of input/output instruction and can be set or reset.

The block diagram is shown in Figure 15 and the I/O timing is in Figure 16.

- **I/O Configuration**

The I/O configuration of each pin can be specified among Open Drain and With Pull up MOS using a mask option as shown in Figure 17.

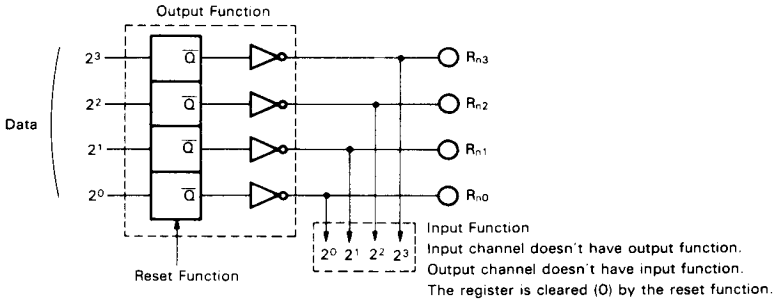

Figure 13 Data I/O Block Diagram

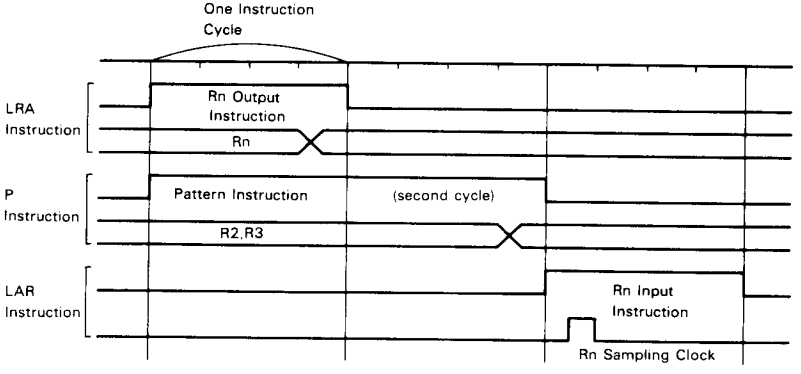

Figure 14 Timing Chart of Data I/O

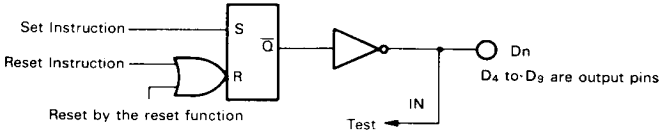

Figure 15 Discrete I/O Block Diagram

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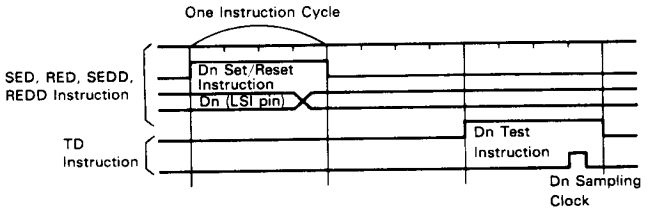


Figure 16 Timing Chart of Discrete I/O

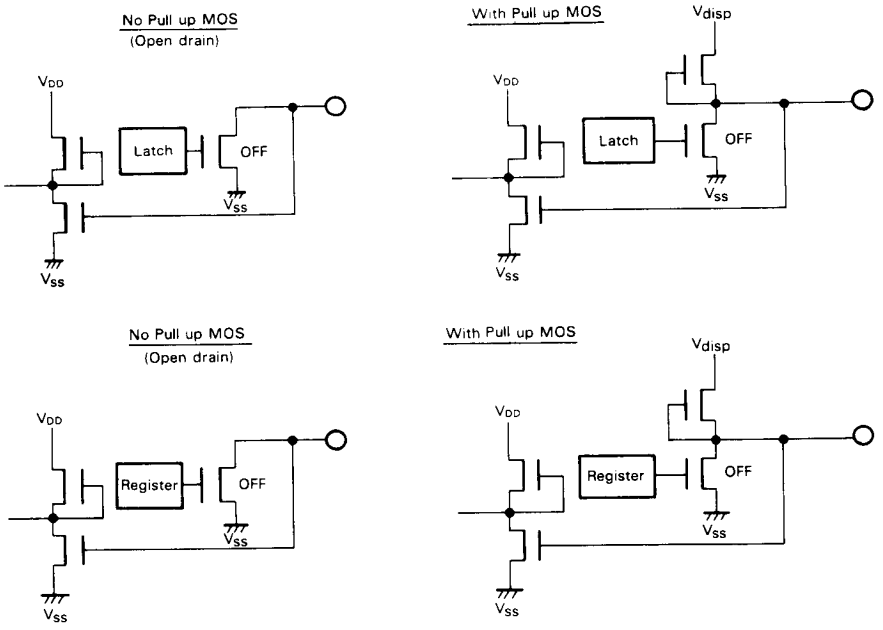


Figure 17 I/O Configuration

■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High") and the HMCS42 gets into operation by setting it to "0" ("Low"); Refer to Figure 18. Moreover, the HMCS42 has the automatic reset function (Built-in Reset). But this Built-in Reset restricts the rise condition of the power supply; Refer to Figure 19.

Internal conditions are specified as follows by the reset function.

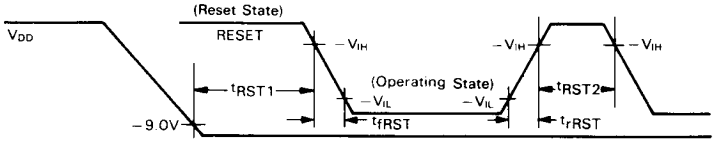
- Program Counter (PC) is set to address 3F on page 14 (14-3F).
- I/O latch and registers (D_0 to D_9, R2, R3) are set to "0".

Note that other blocks (Status, Register, RAM, etc.) are not cleared.

■ OSCILLATOR

The HMCS42 contains its own on-board oscillator and clock circuit (Built-in CPG) requiring only an external timing control element. Also an external oscillator can supply an externally generated clock as a frequency source.

User can select Built-in CPG (R_f C_f Oscillator) or External CPG by a mask option as shown in Figure 20.



· t_{RST1} includes the time required from the power ON until the operation gets into the constant state.
· t_{RST2} is applied when the operation is in the constant state.

Figure 18 RESET Timing

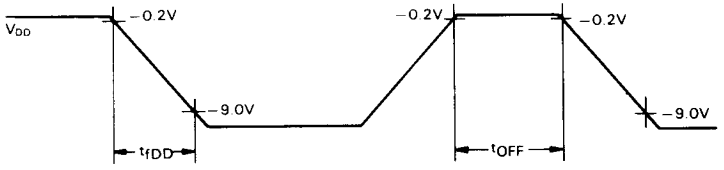
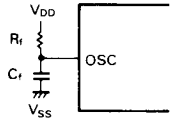


Figure 19 Power Supply Timing for Built-in Reset Circuit

(a) Internal Clock Operation Using Resistor R_f and Capacitor C_f (Built-in CPG ; R_f C_f Oscillator)



(b) External Clock Operation (External CPG)

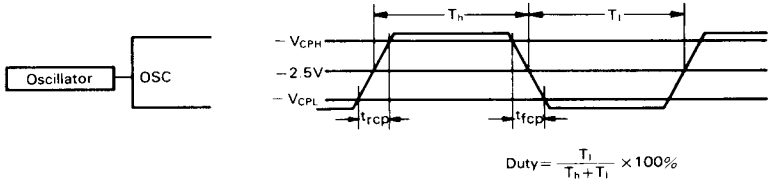


Figure 20 Clock Operation Mode

■ INSTRUCTION LIST

The instructions of the HMCS42 are listed according to their functions, as shown in Table 3.

Table 3 Instruction List

Group	Mnemonic	Function	Status
Register · Register Instruction	LAY	Y → A	
	LASPX	SPX → A	
	XAMR m	A ↔ MR (m)	
RAM Address Register Instruction	LXA	A → X	
	LYA	A → Y	
	LXI i	i → X	
	LYI i	i → Y	
	IY	Y+1 → Y	NZ
	DY	Y−1 → Y	NB
	AYY	Y+A → Y	C
	SYY	Y−A → Y	NB
	XSPX	X ↔ SPX	
RAM · Register Instruction	LAM (X)	M → A (X ↔ SPX)	
	XMA (X)	M ↔ A (X ↔ SPX)	
	LMAIY (X)	A → M, Y+1 → Y (X ↔ SPX)	NZ
	LMADY (X)	A → M, Y−1 → Y (X ↔ SPX)	NB
Immediate Transfer Instruction	LMIIY i	i → M, Y+1 → Y	NZ
	LAI i	i → A	
Arithmetic Instruction	AI i	A+i → A	C
	AMC	M+A+C (F/F) → A	C
	SMC	M−A−$\overline{C}$ (F/F) → A	NB
	AM	M+A → A	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\overline{A}$+1 → A	
	SEC	"1" → C (F/F)	
	REC	"0" → C (F/F)	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
Compare Instruction	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	ALEI i	A ≦ i	NB
	ALEM	A ≦ M	NB
RAM Bit Manipulation Instruction	SEM n	"1" → M (n)	
	REM n	"0" → M (n)	
	TM n	Test M (n)	M (n)

(to be continued)

Group	Mnemonic	Function	Status
ROM Address Instruction	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Input/Output Instruction	SED	"1" → D (Y)	
	RED	"0" → D (Y)	
	TD	Test D (Y)	D (Y)
	SEDD n	"1" → D (n)	
	REDD n	"0" → D (n)	
	LAR p	R (p) → A	
	LRA p	A → R (p)	
	P p	Pattern Generation	
	NOP	No Operation	

[NOTE] 1. (X) after a mnemonic code has two meanings as follows.

Mnemonic only		Instruction execution only
Mnemonic with X		After instruction execution, X ↔ SPX
[Example]	LAM	M → A
	LAMX	M → A, X ↔ SPX

2. Status column shows the factor which brings the Status F/F "1" under judgement instruction or instruction accompanying the judgement.
   - NZ ..... ALU Not Zero
   - C ..... ALU Overflow in Addition, that is, Carry
   - NB ..... ALU Overflow in Subtraction, that is, No Borrow
   - Except above ..... Contents of the status column affects the Status F/F directly.
3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F. Instructions which affect the Carry F/F are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except the pattern instruction (P) are executed in 1 cycle. The pattern instruction (P) is executed in 2 cycles.

HMCS42 Mask Option List

Date	
Customer	
Dept.	
Name	
ROM CODE ID	
LSI Type Name (entered by Hitachi)	

(1) I/O Option

Pin Name	I/O	I/O Option A	I/O Option B	Remarks	Pin Name	I/O	I/O Option A	I/O Option B	Remarks
D_0	I/O				R_{00}	I			
D_1	I/O				R_{01}	I			
D_2	I/O				R_{02}	I			
D_3	I/O				R_{03}	I			
D_4	O				R_{20}	O			
D_5	O				R_{21}	O			
D_6	O				R_{22}	O			
D_7	O				R_{23}	O			
D_8	O				R_{30}	O			
D_9	O				R_{31}	O			
RESET	I				R_{32}	O			
V_{disp}	Power Supply				R_{33}	O			

☆ Specify the I/O composition with a mark of "○" in the applicable composition column.
A: High Break-down Voltage B: With pull up MOS

(2) Package

Package
□ DP-28
□ DP-28S

☆ Mark "✓" in "□" for the selected package.

(3) CPG

CPG
□ External CPG
□ Built-in CPG (R_f C_f Oscillator)

☆ Mark "✓" in "□" for the selected CPG.