

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4012B

### gates

### Dual 4-input NAND gate

Product specification  
File under Integrated Circuits, IC04

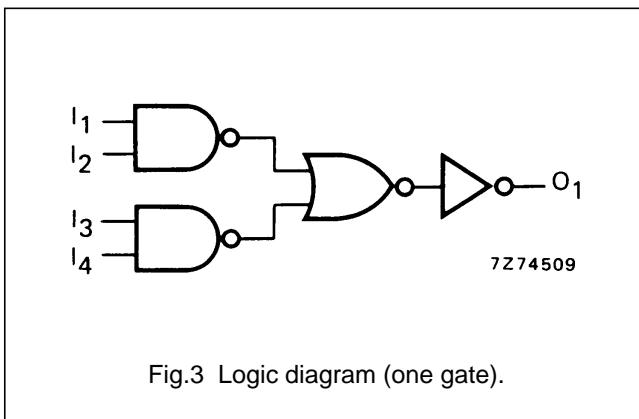
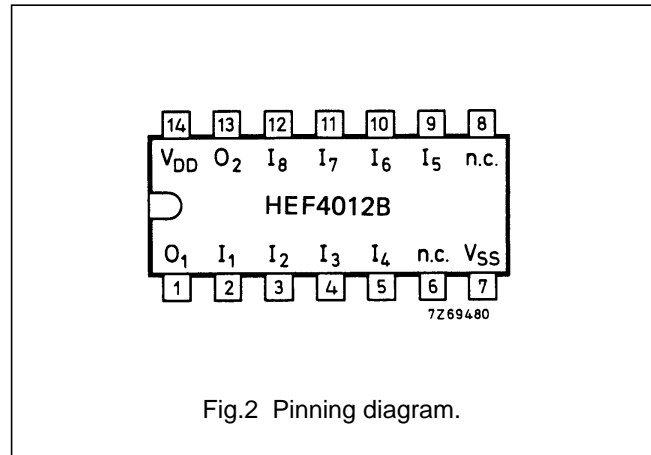
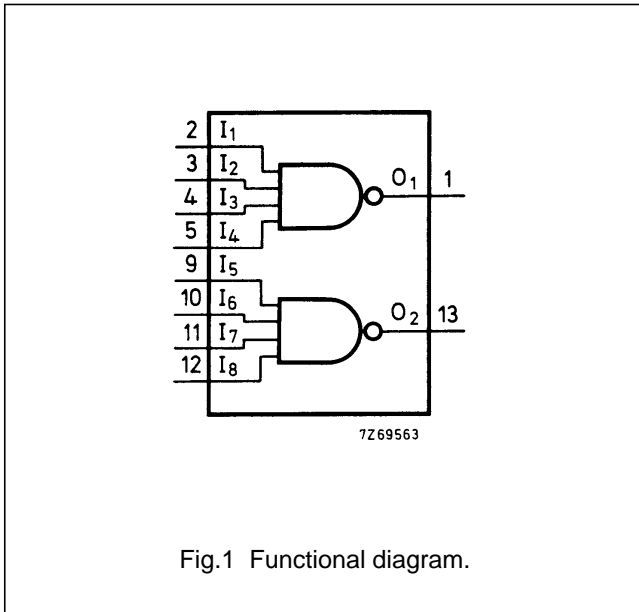
January 1995

# Dual 4-input NAND gate

# HEF4012B gates

### DESCRIPTION

The HEF4012B provides the positive dual 4-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4012BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4012BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4012BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America

### FAMILY DATA, I<sub>DD</sub> LIMITS category GATES

see Family Specifications

## Dual 4-input NAND gate

HEF4012B  
gates**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	TYP	MAX		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	70	135	ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		25	50	ns	$14\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		20	35	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{PLH}$	70	140	ns	$43\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15		25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{TLH}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$1100 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$4400 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$12\,900 f_i + \sum (f_o C_L) \times V_{DD}^2$	