Supertex inc.

High-Voltage Current-Mode PWM Controller

Ordering Information

$+V_{IN}$		Feedback Accuracy	Max Duty Cycle	Package Options			
Min	Max			14 Pin Plastic DIP	20 Pin Plastic PLCC	14 Pin Narrow Body SOIC	Die
10V	120V	< ± 1%	49%	HV9110P	HV9110PJ	HV9110NG	HV9110X
9.0V	80V	± 2%	49%	HV9112P	HV9112PJ	HV9112NG	HV9112X
10V	120V	< ± 1%	99%	HV9113P	HV9113PJ	HV9113NG	HV9113X

Standard temperature range for all parts is industrial (-40° to +85°C).

Features

- ❑ 10 to 120V input range
- ❑ Current-mode control
- ❑ High efficiency
- ❑ Up to 1.0MHz internal oscillator
- ❑ Internal start-up circuit
- ❑ Low internal noise

Applications

- ❑ DC/DC converters
- ❑ Distributed power systems
- ❑ ISDN equipment
- ❑ PBX systems
- ❑ Modems

General Description

The Supertex HV9110 through HV9113 are a series of BiCMOS/DMOS single-output, pulse width modulator ICs intended for use in high-speed high-efficiency switchmode power supplies. They provide all the functions necessary to implement a single-switch current-mode PWM, in any topology, with a minimum of external parts.

Because they utilize Supertex's proprietary BiCMOS/DMOS technology, they require less than one tenth of the operating power of conventional bipolar PWM ICs, and can operate at more than twice their switching frequency. Dynamic range for regulation is also increased, to approximately 8 times that of similar bipolar parts. They start directly from any DC input voltages between 10 and 120VDC, requiring no external power resistor. The output stage is push-pull CMOS and thus requires no clamping diodes for protection, even when significant lead length exists between the output and the external MOSFET. The clock frequency is set with a single external resistor.

Accessory functions are included to permit fast remote shutdown (latching or nonlatching) and undervoltage shutdown.

For similar ICs intended to operate directly from up to 450VDC input, please consult the data sheet for the HV9120/9123.

Absolute Maximum Ratings

$+V_{IN}$, Input Voltage	HV9110/9113	120V
	HV9112	80V
V_{DD}, Logic Voltage		15.5V
Logic Linear Input, FB and Sense Input Voltage		-0.3V to V_{DD}+0.3V
Storage Temperature		-65°C to 150°C
Power Dissipation, SOIC		750mW
Power Dissipation, Plastic DIP		1000mW
Power Dissipation PLCC		1400mW

For detailed circuit and application information, please refer to application notes AN-H13 and AN-H21 to AN-H24.

11/12/01

Electrical Characteristics

(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = 0V, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ,T_A = 25°C.)

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
Reference							
V_{REF}	Output Voltage	HV9110/13	3.92	4.00	4.08	V	R_L = 10MΩ
		HV9112	3.88	4.00	4.12		
		HV9110/13	3.82	4.00	4.16		R_L = 10MΩ, T_A = -55°C to 125°C
Z_{OUT}	Output Impedance[1]		15	30	45	KΩ	
I_{SHORT}	Short Circuit Current			125	250	µA	V_{REF} = $-V_{IN}$
ΔV_{REF}	Change in V_{REF} with Temperature[1]			0.25		mV/°C	T_A = -55°C to 125°C
Oscillator							
f_{MAX}	Oscillator Frequency		1.0	3.0		MHz	R_{OSC} = 0Ω
f_{OSC}	Initial Accuracy[2]		80	100	120	KHz	R_{OSC} = 330KΩ
			160	200	240		R_{OSC} = 150KΩ
	Voltage Stability				15	%	9.5V < V_{DD} <13.5V
	Temperature Coefficient[1]			170		ppm/°C	T_A = -55°C to 125°C
PWM							
D_{MAX}	Maximum Duty Cycle[1]	HV9110/12	49.0	49.4	49.6	%	
		HV9113	95	97	99		
D_{MIN}	Deadtime[1]	HV9113		225		nsec	
	Minimum Duty Cycle				0	%	
	Minimum Pulse Width Before Pulse Drops Out[1]			80	125	nsec	
Current Limit							
	Maximum Input Signal		1.0	1.2	1.4	V	V_{FB} = 0V
t_d	Delay to Output[1]			80	120	ns	V_{SENSE} = 1.5V, V_{COMP} ≤ 2.0V
Error Amplifier							
V_{FB}	Feedback Voltage	HV9110/13	3.96	4.00	4.04	V	V_{FB} Shorted to Comp
		HV9112	3.92	4.00	4.08		
I_{IN}	Input Bias Current			25	500	nA	V_{FB} = 4.0V
V_{OS}	Input Offset Voltage		nulled during trim				except HV9111
A_{VOL}	Open Loop Voltage Gain[1]		60	80		dB	
GB	Unity Gain Bandwidth[1]		1.0	1.3		MHz	
Z_{OUT}	Output Impedance[1]		see Fig. 1			Ω	
I_{SOURCE}	Output Source Current		-1.4	-2.0		mA	V_{FB} = 3.4V
I_{SINK}	Output Sink Current		0.12	0.15		mA	V_{FB} = 4.5V
PSRR	Power Supply Rejection[1]		see Fig. 2			dB	

Notes:

1. Guaranteed by design. Not subject to production test.
2. Stray capacitance on OSC In pin must be ≤5pF.

Electrical Characteristics (continued)

(Unless otherwise specified, V_{DD} = 10V, $+V_{IN}$ = 48V, Discharge = $-V_{IN}$ = 0V, R_{BIAS} = 390KΩ, R_{OSC} = 330KΩ,T_A = 25°C.)

Symbol	Parameters		Min	Typ	Max	Unit	Conditions
Pre-regulator/Startup							
$+V_{IN}$	Input Voltage	HV9110/13			120	V	I_{IN} < 10µA; V_{CC} > 9.4V
		HV9112			80		
$+I_{IN}$	Input Leakage Current				10	µA	V_{DD} > 9.4V
V_{TH}	V_{DD} Pre-regulator Turn-off Threshold Voltage		8.0	8.7	9.4	V	I_{PREREG} = 10µA
V_{LOCK}	Undervoltage Lockout		7.0	8.1	8.9	V	
Supply							
I_{DD}	Supply Current			0.75	1.0	mA	C_L < 75pF
I_Q	Quiescent Supply Current			0.55		mA	$\overline{\text{Shutdown}}$ = $-V_{IN}$
I_{BIAS}	Nominal Bias Current			20		µA	
V_{DD}	Operating Range		9.0		13.5	V	
Shutdown Logic							
t_{SD}	$\overline{\text{Shutdown}}$ Delay[1]			50	100	ns	C_L = 500pF, V_{SENSE} = $-V_{IN}$
t_{SW}	$\overline{\text{Shutdown}}$ Pulse Width[1]		50			ns	
t_{RW}	RESET Pulse Width[1]		50			ns	
t_{LW}	Latching Pulse Width[1]		25			ns	$\overline{\text{Shutdown}}$ and reset low
V_{IL}	Input Low Voltage				2.0	V	
V_{IH}	Input High Voltage		7.0			V	
I_{IH}	Input Current, Input Voltage High			1.0	5.0	µA	V_{IN} = V_{DD}
I_{IL}	Input Current, Input Voltage Low			-25	-35	µA	V_{IN} = 0V
Output							
V_{OH}	Output High Voltage	HV9110/13	V_{DD} -0.25			V	I_{OUT} = 10mA
		HV9112	V_{DD} -0.3				
		HV9110/13	V_{DD} -0.3				I_{OUT} = 10mA, T_A = -55°C to 125°C
V_{OL}	Output Low Voltage	All			0.2	V	I_{OUT} = -10mA
		HV9110/13			0.3		I_{OUT} = -10mA, T_A = -55°C to 125°C
R_{OUT}	Output Resistance	Pull Up		15	25	Ω	I_{OUT} = ±10mA
		Pull Down		8.0	20		
		Pull Up		20	30	Ω	I_{OUT} = ±10mA,
		Pull Down		10	30		T_A = -55°C to 125°C
t_R	Rise Time[1]			30	75	ns	C_L = 500pF
t_F	Fall Time[1]			20	75	ns	C_L = 500pF

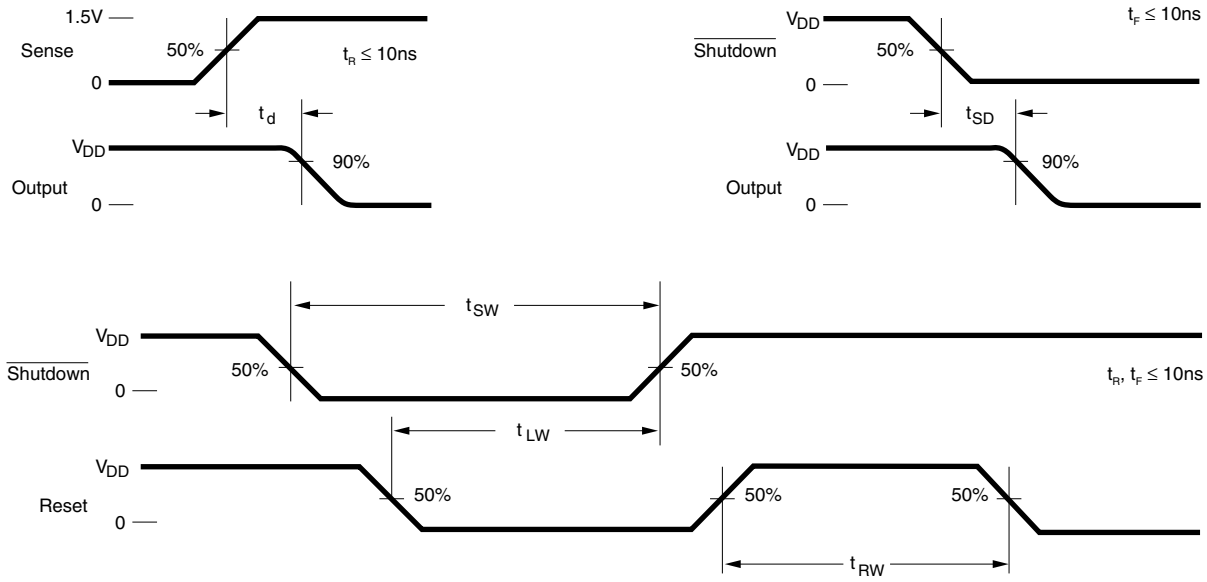
Note:

1. Guaranteed by design. Not subject to production test.

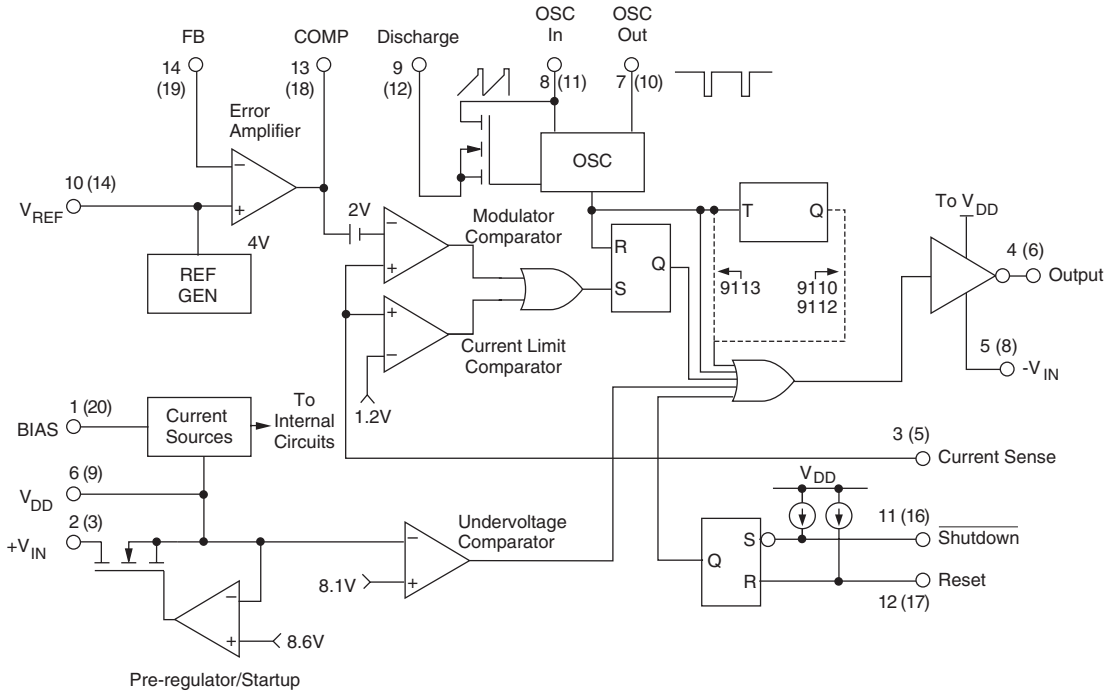
Truth Table

$\overline{\text{Shutdown}}$	Reset	Output
H	H	Normal Operation
H	H → L	Normal Operation, No Change
L	H	Off, Not Latched
L	L	Off, Latched
L → H	L	Off, Latched, No Change

Shutdown Timing Waveforms



Functional Block Diagram



Pin numbers in parentheses are for PLCC package

Typical Performance Curves

Fig. 1

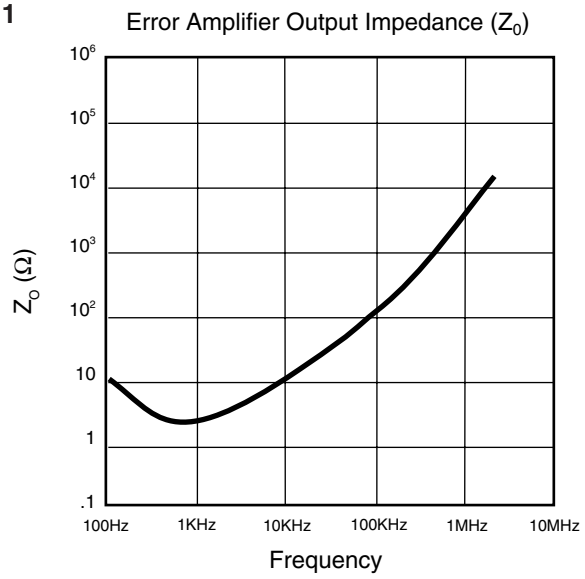


Fig. 2

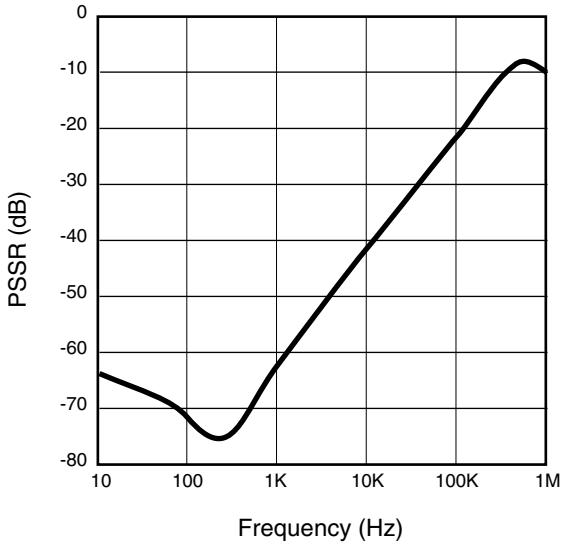


Fig. 3

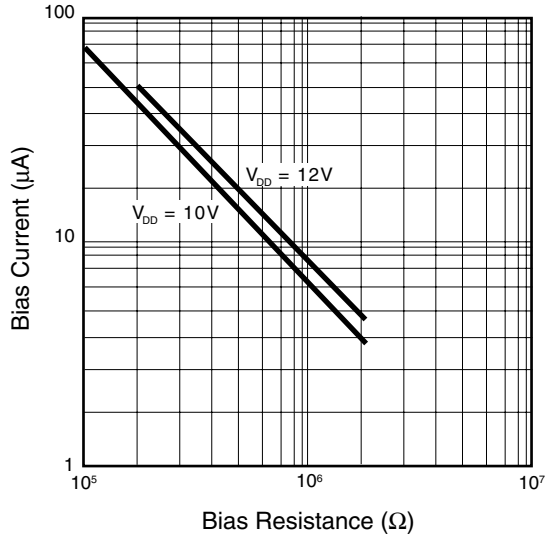


Fig. 4

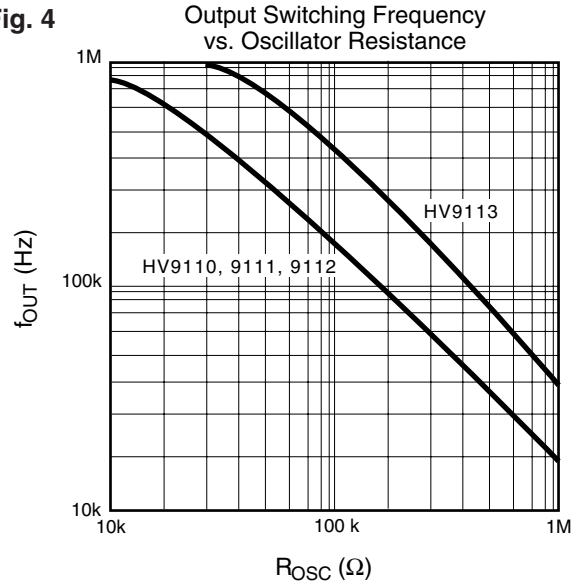


Fig. 5

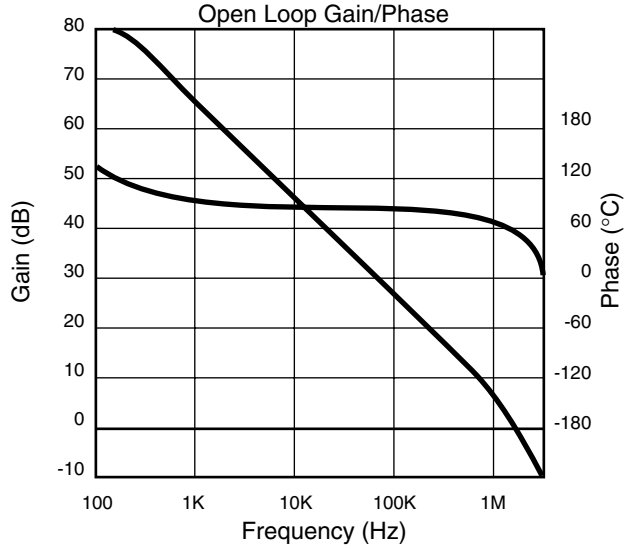
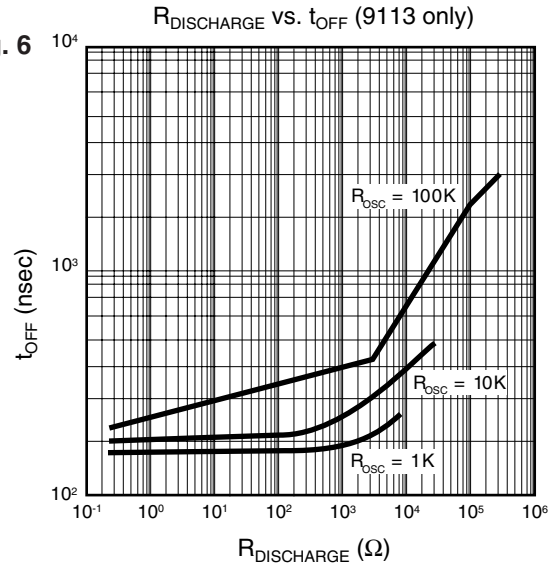
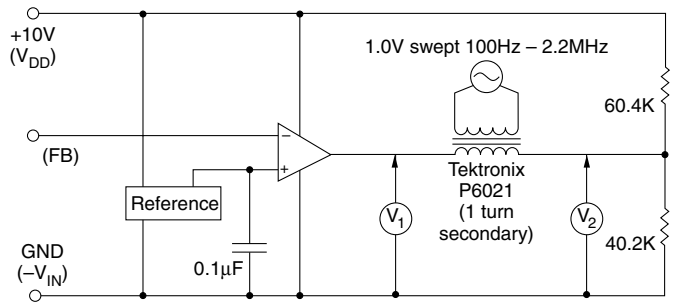


Fig. 6

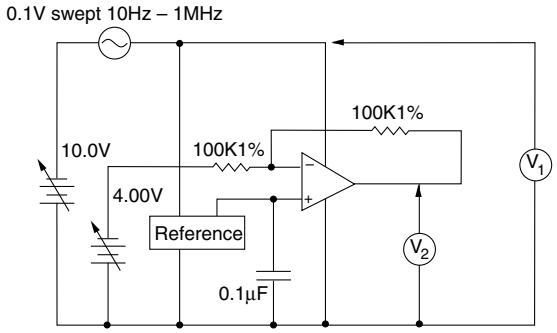


Test Circuits

Error Amp Z_{OUT}



PSRR



NOTE: Set Feedback Voltage so that
$V_{COMP} = V_{DIVIDE} \pm 1mV$ before connecting transformer

Detailed Description

Preregulator

The preregulator/startup circuit for the HV911X consists of a high-voltage n-channel depletion-mode DMOS transistor driven by an error amplifier to form a variable current path between the V_{IN} terminal and the V_{DD} terminal. Maximum current (about 20 mA) occurs when $V_{DD} = 0$, with current reducing as V_{DD} rises. This path shuts off altogether when V_{DD} rises to somewhere between 7.8 and 9.4V, so that if V_{DD} is held at 10 or 12V by an external source (generally the supply the chip is controlling). No current other than leakage is drawn through the high voltage transistor. This minimizes dissipation.

An external capacitor between V_{DD} and V_{SS} is generally required to store energy used by the chip in the time between shutoff of the high voltage path and the V_{DD} supply's output rising enough to take over powering the chip. This capacitor should have a value of 100X or more the *effective* gate capacitance of the MOSFET being driven, i.e.,

$C_{storage} \geq 100$ x (gate charge of FET at 10V ÷ 10V)

as well as very good high frequency characteristics. Stacked polyester or ceramic caps work well. Electrolytic capacitors are generally not suitable.

A common resistor divider string is used to monitor V_{DD} for both the undervoltage lockout circuit and the shutoff circuit of the high voltage FET. Setting the undervoltage sense point about 0.6V lower on the string than the FET shutoff point guarantees that the undervoltage lockout always releases before the FET shuts off.

Bias Circuit

An external bias resistor, connected between the bias pin and V_{SS} is required by the HV911X to set currents in a series of current mirrors used by the analog sections of the chip. Nominal external bias current requirement is 15 to 20µA, which can be set by a 390KΩ to 510KΩ resistor if a 10V V_{DD} is used, or a 510kΩ to 680KΩ resistor if V_{DD} will be 12V. A precision resistor is *not* required; ± 5% is fine.

Clock Oscillator

The clock oscillator of the HV911X consists of a ring of CMOS inverters, timing capacitors, a capacitor discharge FET, and, in the 50% maximum duty cycle versions, a frequency dividing flip-flop. A single external resistor between the OSC In and OSC Out pins is required to set oscillator frequency (see graph). For the 50% maximum duty cycle versions the Discharge pin is internally connected to GND. For the 99% duty cycle version, the discharge pin can either be connected to V_{SS} directly or connected to V_{SS} through a resistor used to set a deadtime.

One difference exists between the Supertex HV911X and competitive 911X's: On the Supertex part the oscillator is shut off when a shutoff command is received. This saves about 150µA of quiescent current, which aids in the construction of power supplies to meet CCITT specification I-430, and in other situations where an absolute minimum of quiescent power dissipation is required.

Reference

The Reference of the HV911X consists of a stable bandgap reference followed by a buffer amplifier which scales the voltage up to approximately 4.0V. The scaling resistors of the reference buffer amplifier are trimmed during manufacture so that the output of the error amplifier when connected in a gain of –1 configuration is as close to 4.000V as possible. This nulls out any input offset of the error amplifier. As a consequence, even though the observed reference voltage of a specific part may not be exactly 4.0V, the feedback voltage required for proper regulation will be.

A ≈50KΩ resistor is placed internally between the output of the reference buffer amplifier and the circuitry it feeds (reference output pin and non-inverting input to the error amplifier). This allows overriding the internal reference with a low-impedance voltage source ≤6.0V. Using an external reference reinstates the input offset voltage of the error amplifier, and its effect of the exact value of feedback voltage required.

Because the reference of the 911X is a high impedance node, and usually there will be significant electrical noise near it, a bypass capacitor between the reference pin and V_{SS} is strongly recommended. The reference buffer amplifier is intentionally compensated to be stable with a capacitive load of 0.01 to 0.1µF.

Detailed Description (continued)

Error Amplifier

The error amplifier in the HV911X is a true low-power differential input operational amplifier intended for around-the-amplifier compensation. It is of mixed CMOS-bipolar construction: A PMOS input stage is used so the common-mode range includes ground and the input impedance is very high. This is followed by bipolar gain stages which provide high gain without the electrical noise of all-MOS amplifiers. The amplifier is unity-gain stable.

Current Sense Comparators

The HV911X uses a true dual comparator system with independent comparators for modulation and current limiting. This allows the designer greater latitude in compensation design, as there are no clamps (except ESD protection) on the compensation pin. Like the error amplifier, the comparators are of low-noise BiCMOS construction.

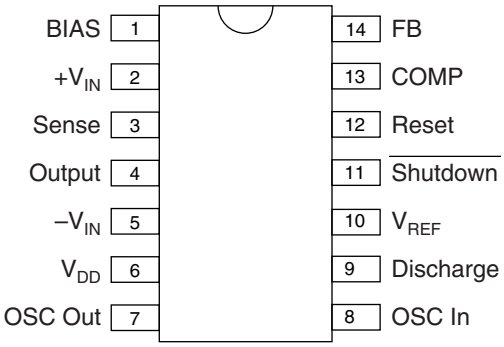
Remote Shutdown

The shutdown and reset pins of the 911X can be used to perform either latching or non-latching shutdown of a converter as required. These pins have internal current source pull-ups so they can be driven from open-drain logic. When not used they should be left open, or connected to V_{DD}.

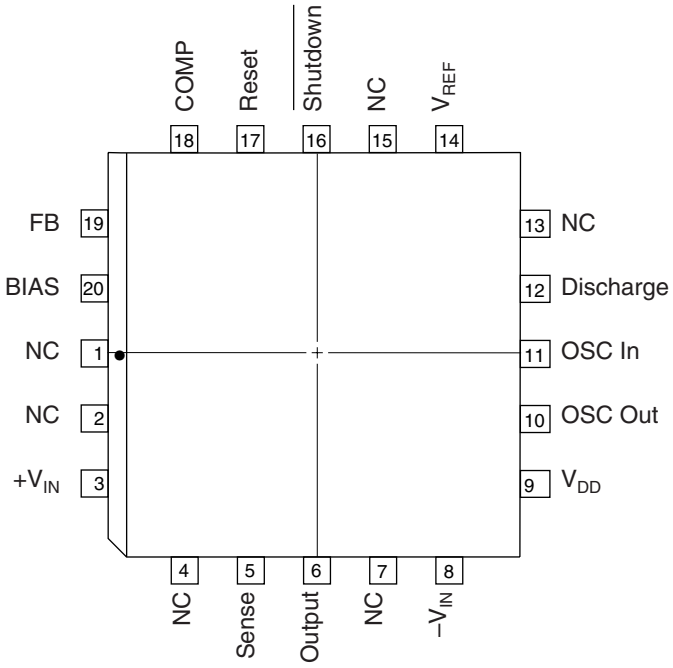
Output Buffer

The output buffer of the HV911X is of standard CMOS construction (P-channel pull-up, N-channel pull-down). Thus the body-drain diodes of the output stage can be used for spike clipping if necessary, and external Schottky diode clamping of the output is not required.

Pinout



14 Pin SOIC/DIP Package



20-pin PJ Package
top view

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