SIEMENS

256 K x 16-Bit Dynamic RAM
Low Power 256 K x 16-Bit Dynamic RAM with Self Refresh

HYB 514171BJ-60/-70/-80
HYB 514171BJL-60/-70/-80

Advanced Information

- 262 144 words by 16-bit organization
- 0 to 70 °C operating temperature
- Fast access and cycle time
  RAS access time:
  60 ns (-60 version)
  70 ns (-70 version)
  80 ns (-80 version)
  CAS access time:
  20 ns (-60, -70, -80 version)
  Cycle time:
  110 ns (-60 version)
  130 ns (-70 version)
  150 ns (-80 version)
- Fast page mode cycle time
  45 ns (-60 version)
  45 ns (-70 version)
  50 ns (-80 version)
- Single + 5 V (± 10 %) supply with a built-in VBB generator
- Low Power dissipation
  max. 1127,5 mW active (-60 version)
  max. 880 mW active (-70 version)
  max. 825 mW active (-80 version)
- Standby power dissipation
  11 mW standby (TLL)
  5.5 mW max. standby (CMOS)
  1.1 mW max. standby (CMOS) for Low Power Version
- Output unlatched at cycle and allows two-dimensional chip selection
- Read, write, read-modify write, CAS-before-RAS refresh, RAS-only refresh, hidden-refresh and fast page mode capability
- 2 CAS / 1WE Version
- Self Refresh (L-Version)
- All inputs and outputs TTL-compatible
- 512 refresh cycles / 16 ms
- 512 refresh cycles / 128 ms
  Low Power Version only
- Plastic Packages:
  P-SOJ-40-1 400mil width

The HYB 514171BJ/BJL is the new generation dynamic RAM organized as 262 144 words by 16-bit. The HYB 514171BJ/BJL utilizes CMOS silicon gate process as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514171BJ/BJL to be packed in a standard plastic 400mil wide P-SOJ-40/40 package. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include Self Refresh (L-Version), single + 5 V (± 10 %) power supply, direct interfacing with high performance logic device families such as Schottky TTL.

Ordering Information

Type	Ordering Code	Package	Description
HYB 514171BJ-60	Q67100-Q727	P-SOJ-40-1	60 ns 256 K x 16 DRAM
HYB 514171BJ-70	Q67100-Q728	P-SOJ-40-1	70 ns 256 K x 16 DRAM
HYB 514171BJ-80	Q67100-Q729	P-SOJ-40-1	80 ns 256 K x 16 DRAM

Truth Table

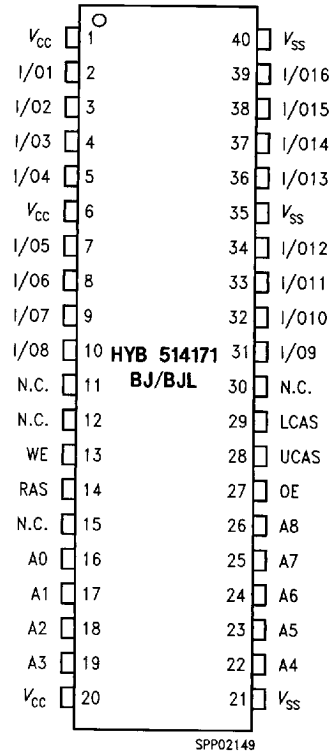
RAS	LCAS	UCAS	WE	OE	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	

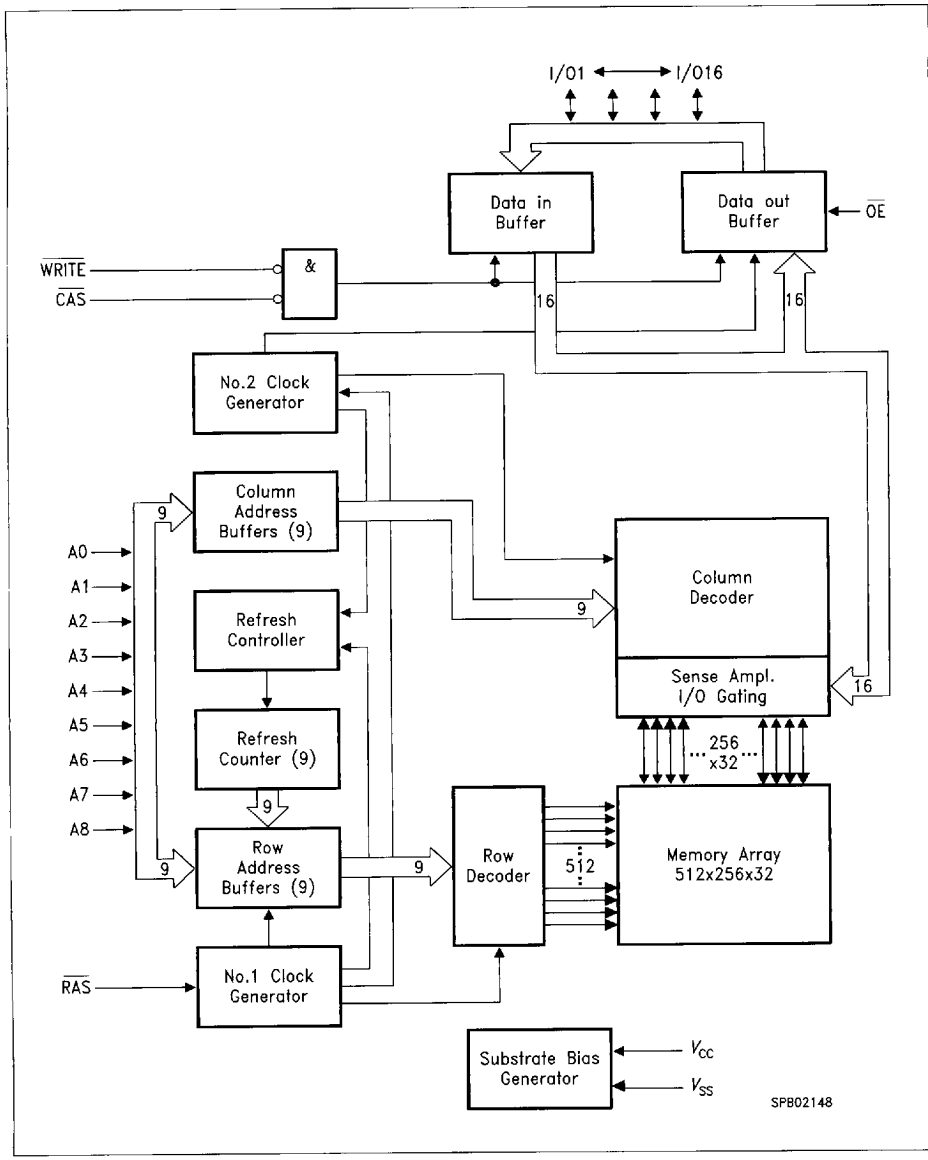
Pin Names

A0-A8	Address Inputs
RAS	Row Address Strobe
UCAS, LCAS	Column Address Strobe
WE	Read/Write Input
OE	Output Enable
IO1 – IO16	Data Input/Output
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Pin Configuration

P-SOJ-40-1





Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	1)
Input low voltage	V_{IL}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5.0 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input (0 V < V_{IN} < 7 V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current: -60 version -70 version -80 version	I_{CC1}		205 160 150	mA	2) 3)
Standby V_{CC} supply current (RAS = CAS = V_{IH})	I_{CC2}		2	mA	–
Average V_{CC} supply current during RAS-only refresh cycles: -60 version -70 version -80 version	I_{CC3}		205 160 150	mA	2)

Notes see page 157.

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode operation: -60 version -70 version -80 version	I_{CC4}		140 140 130	mA	2) 3)
Standby V_{CC} supply current (RAS = CAS = V_{CC} – 0.2 V)	I_{CC5}		1	mA	1)
Average V_{CC} supply current during CAS-before-RAS refresh mode: -60 version -70 version -80 version	I_{CC6}		205 160 150	mA	2)
Standby V_{CC} current (L-version) (RAS = CAS = V_{CC} – 0.2 V)	I_{CC5}		200	µA	
Self Refresh Current (L-version) (RAS, CAS = V_{IH}, A0 – A8 = V_{CC} – 0.2 V or 0.2 V)	I_{CC8}		300	µA	

Notes see page 157.

AC Characteristics [4]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	150	–	ns
Read-write cycle time	t_{RWC}	165	–	185	–	205	–	ns
Fast page mode cycle time	t_{PC}	45	–	45	–	50	–	ns
Fast page mode read/write cycle time	t_{PRWC}	100	–	100	–	105	–	ns
Access time from RAS [6) 11)]	t_{RAC}	–	60	–	70	–	80	ns
Access time from CAS [6) 11)]	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	–	40	ns
Access time from CAS precharge [6)]	t_{CPA}	–	40	–	40	–	45	ns
CAS to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay from CAS [7)]	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
RAS precharge time	t_{RP}	40	–	50	–	60	–	ns
RAS pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns
RAS pulse width in fast page mode	t_{RASP}	60	200000	70	200000	80	200000	ns
RAS hold time	t_{RSH}	20	–	20	–	20	–	ns
CAS hold time	t_{CSH}	60	–	70	–	80	–	ns
CAS pulse width	t_{CAS}	20	10000	20	10000	20	10000	ns
RAS to CAS delay time [11)]	t_{RCD}	20	40	20	50	20	60	ns
RAS to column address delay time [12)]	t_{RAD}	15	30	15	35	15	40	ns

Notes see page 157.

AC Characteristics (cont'd) [4]

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
CAS to RAS precharge time	t_{CRP}	5	–	5	–	10	–	ns
CAS precharge time	t_{CPN}	10	–	10	–	10	–	ns
CAS precharge time in fast page mode	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address to RAS lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time ref. to RAS [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	15	–	ns
Write command to RAS lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to CAS lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9]	t_{DH}	15	–	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	–	16	ms
Refresh period (L-version)	t_{REF}	–	128	–	128	–	128	ms

Notes see page 157.

AC Characteristics (cont'd) [4]

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Write command setup time [10]	t_{WCS}	0	–	0	–	0	–	ns
CAS to WRITE delay time [10]	t_{CWD}	50	–	50	–	50	–	ns
RAS to WRITE delay time [10]	t_{RWD}	90	–	100	–	110	–	ns
Column address to WRITE delay time [10]	t_{AWD}	60	–	65	–	70	–	ns
CAS setup time (CBR cycle)	t_{CSR}	5	–	5	–	5	–	ns
CAS hold time (CBR cycle)	t_{CHR}	15	–	15	–	15	–	ns
RAS to CAS precharge time	t_{RPC}	0	–	0	–	0	–	ns
CAS precharge time (CAS-before-RAS counter test cycle)	t_{CPT}	30	–	40	–	40	–	ns
Write to RAS precharge time (CBR cycle)	t_{WRP}	10	–	10	–	10	–	ns
Write to RAS hold time (CBR cycle)	t_{WRH}	10	–	10	–	10	–	ns
OE command hold time	t_{OEH}	20	–	20	–	20	–	ns
OE access time	t_{OEA}	–	20	–	20	–	20	ns
RAS hold time referenced to OE	t_{ROH}	10	–	10	–	10	–	ns
Output buffer turn-off delay from OE	t_{OEZ}	0	20	0	20	0	20	ns
Data to CAS low delay [14]	t_{DZC}	0	–	0	–	0	–	ns
Data to OE low delay [14]	t_{DZO}	0	–	0	–	0	–	ns
CAS high to data delay [15]	t_{CDD}	20	–	20	–	20	–	ns
OE high to data delay [15]	t_{ODD}	20	–	20	–	20	–	ns

Notes see page 157.

AC Characteristics (cont'd) [4]

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
CAS hold time after OE low	t_{OECH}	20	–	20	–	20	–	ns
RAS pulse width Self Refresh (L-Version)	t_{RASS}	100	–	100	–	100	–	µs
RAS precharge time Self Refresh (L-Version)	t_{RPS}	110	–	130	–	150	–	ns
CAS hold time Self Refresh (L-Version)	t_{CHS}	40	–	50	–	60	–	ns

Notes see page 157.

Capacitance
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	C_{I1}	–	6	pF
Input capacitance (RAS, UCAS, LCAS, WE, OE)	C_{I2}	–	7	pF
Output capacitance (IO1 to IO16)	C_{IO}	–	7	pF

Notes for pages 151 to 156:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC8} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading.

4) An initial pause of 200 µs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.

5) $V_{IH\ (min)}$ and $V_{IL\ (max)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) $t_{OFF\ (max)}$, $t_{OEZ\ (max)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the CAS leading edge in early write cycles and to the WRITE leading edge in read-write cycles.

10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS\ (min)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD\ (min)}$, $t_{CWD} > t_{CWD\ (min)}$ and $t_{AWD} > t_{AWD\ (min)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.

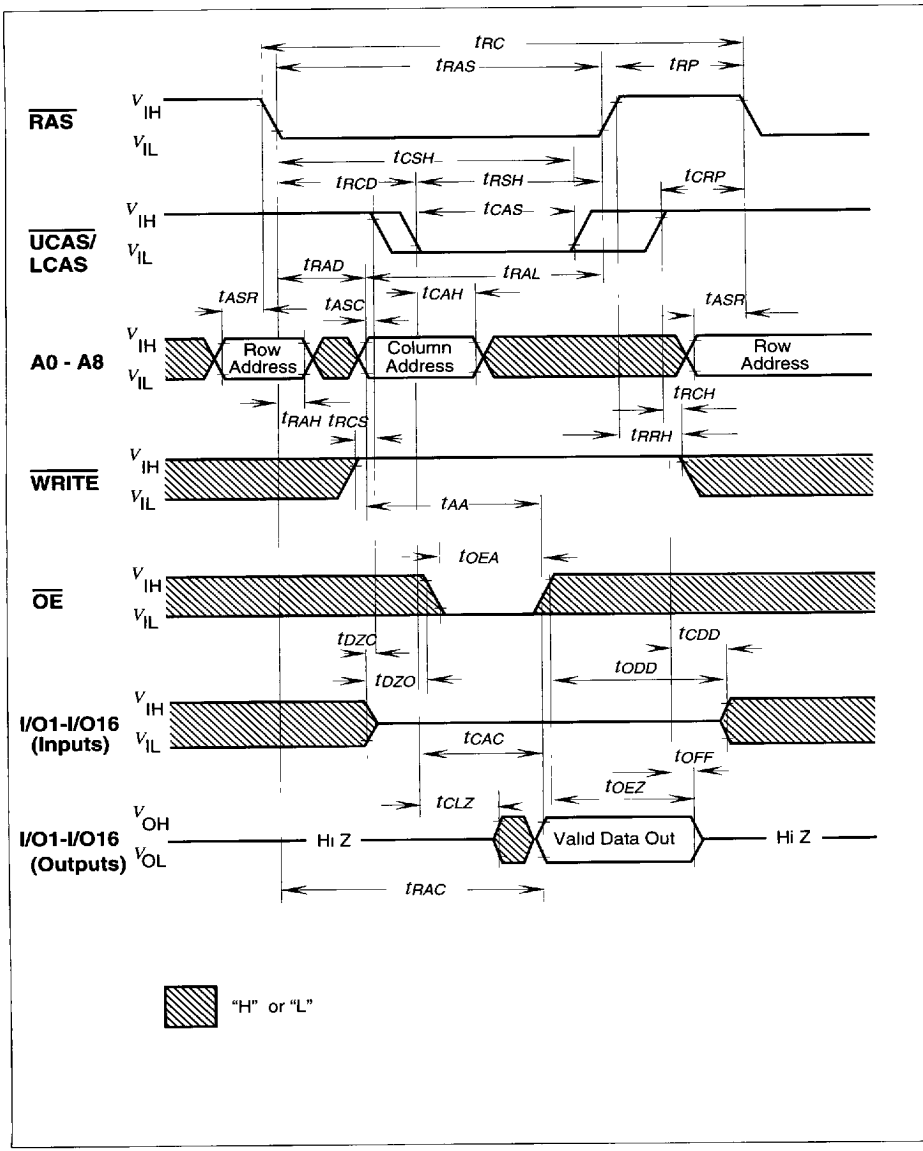
11) Operation within the $t_{RCD\ (max)}$ limit ensures that $t_{RAC\ (max)}$ can be met. $t_{RCD\ (max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD\ (max)}$ limit, then access time is controlled by t_{CAC}.

12) Operation within the $t_{RAD\ (max)}$ limit ensures that $t_{RAC\ (max)}$ can be met. $t_{RAD\ (max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD\ (max)}$ limit, then access time is controlled by t_{AA}.

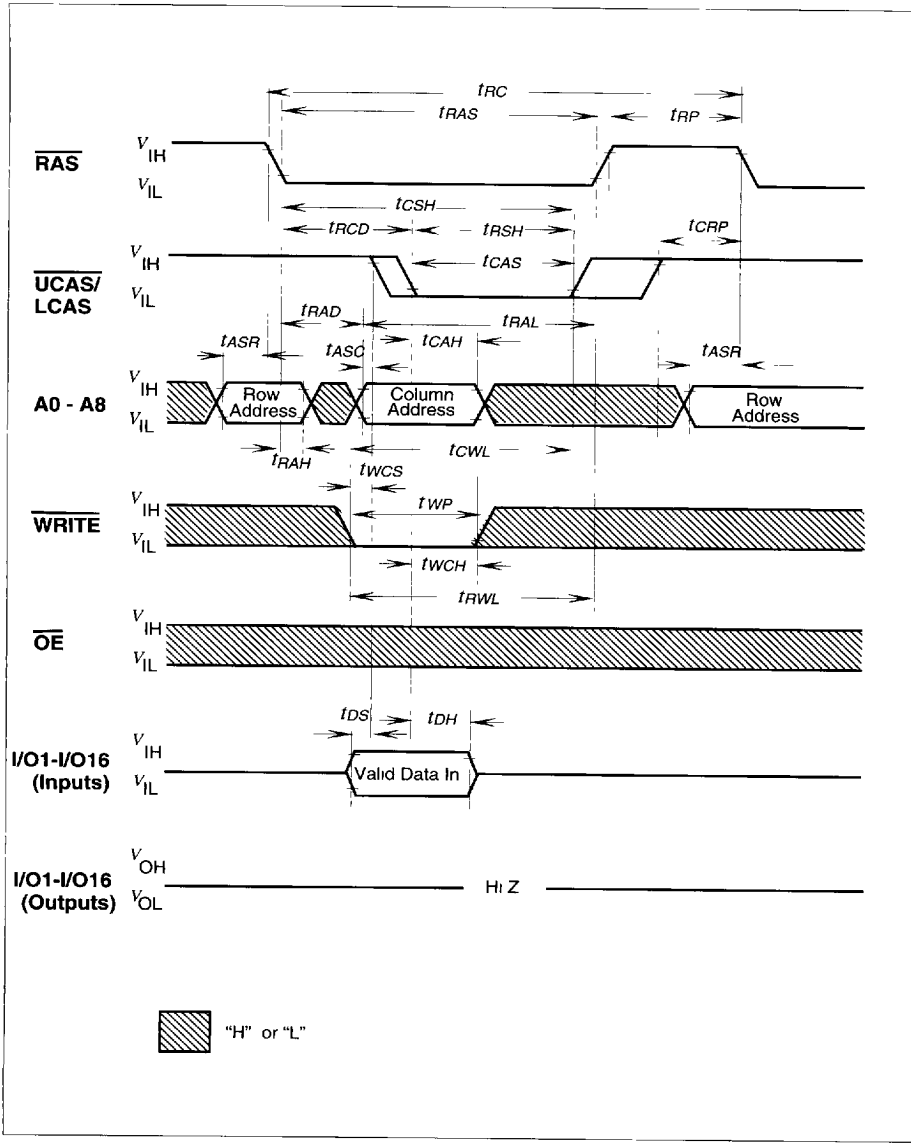
13) AC measurements assume $t_T = 5$ ns.

14) Either t_{DZC} or t_{DZO} must be satisfied.

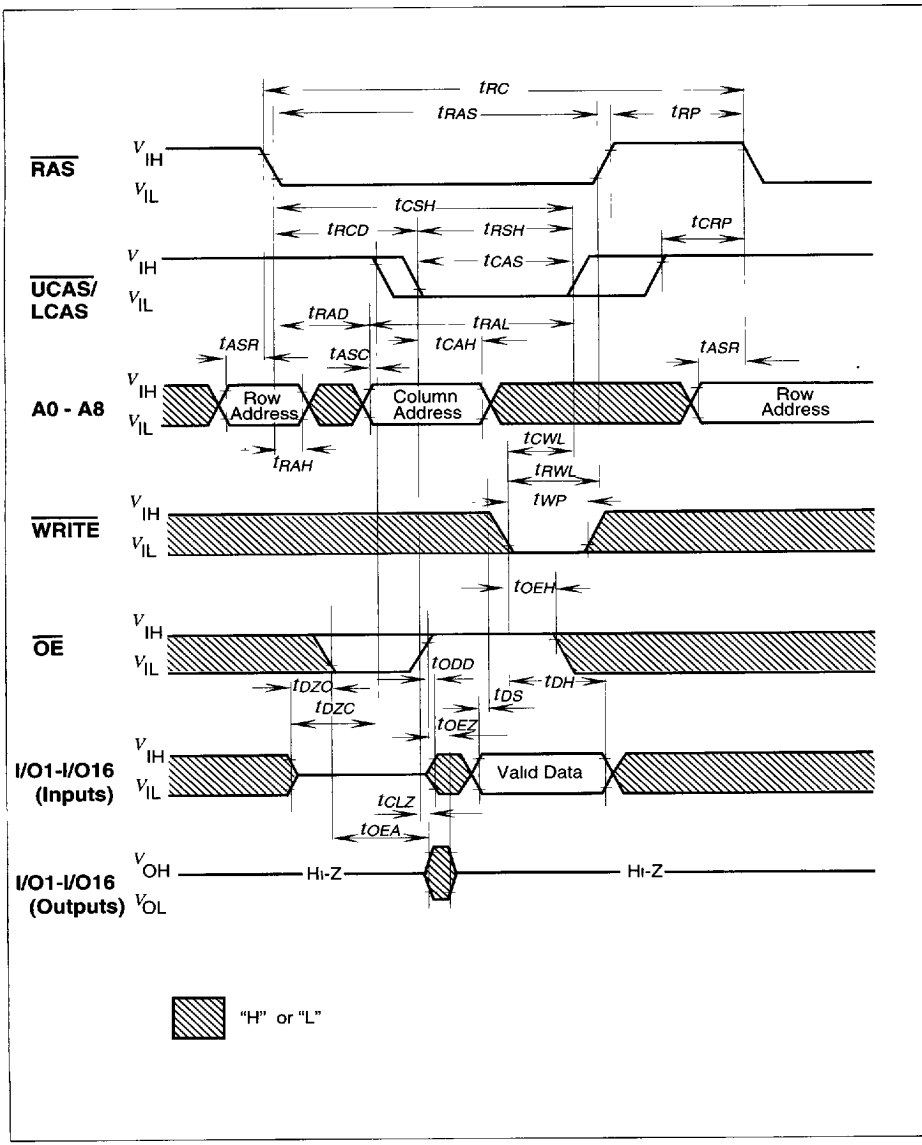
15) Either t_{CDD} or t_{ODD} must be satisfied.



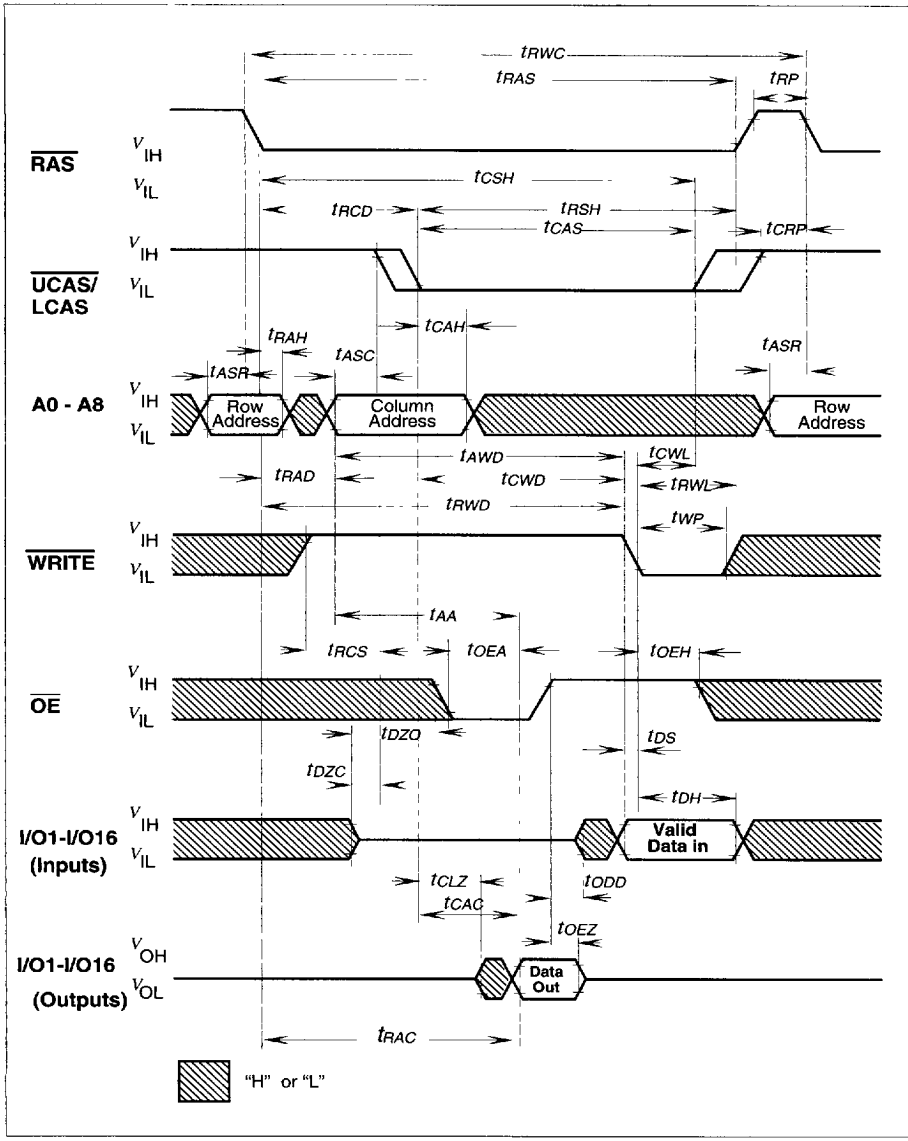
Read Cycle



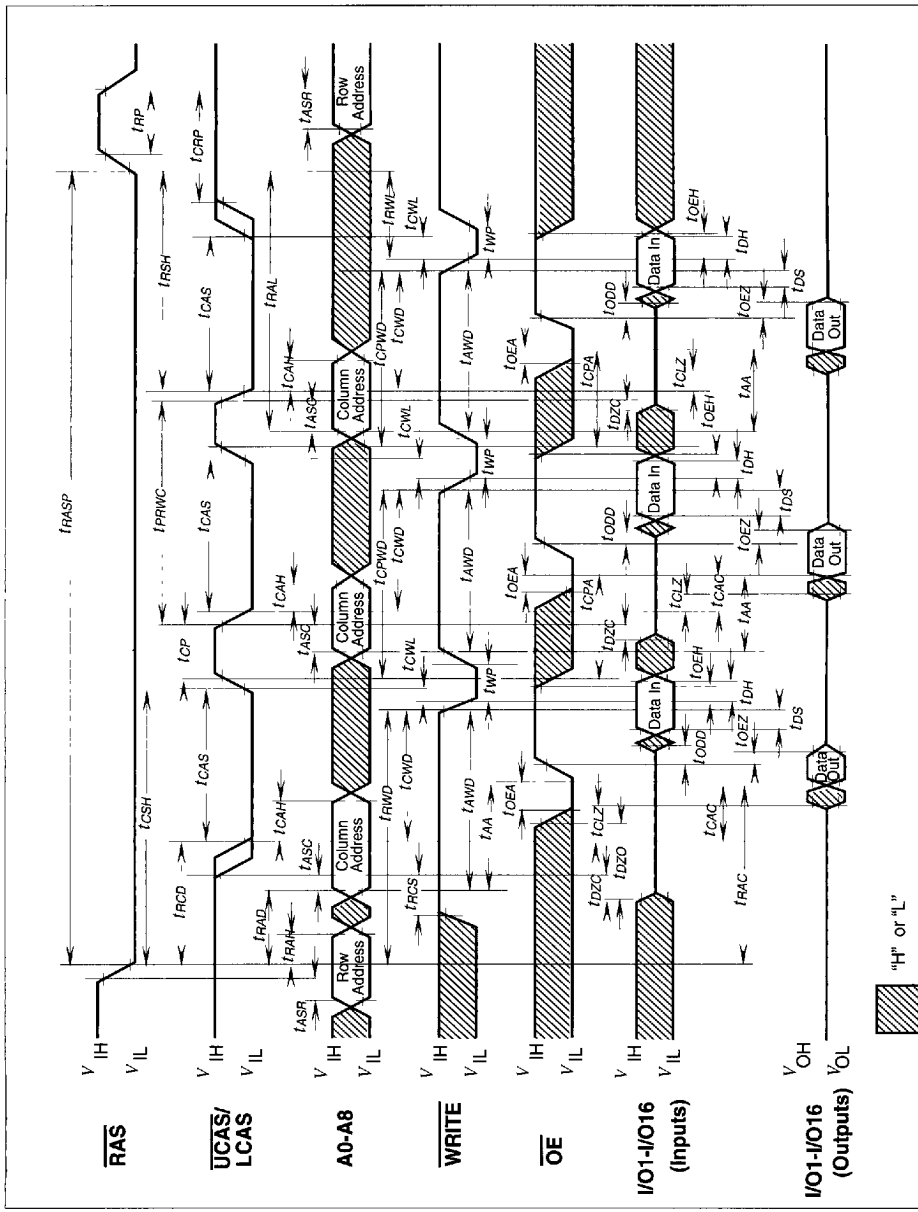
Write Cycle (Early Write)



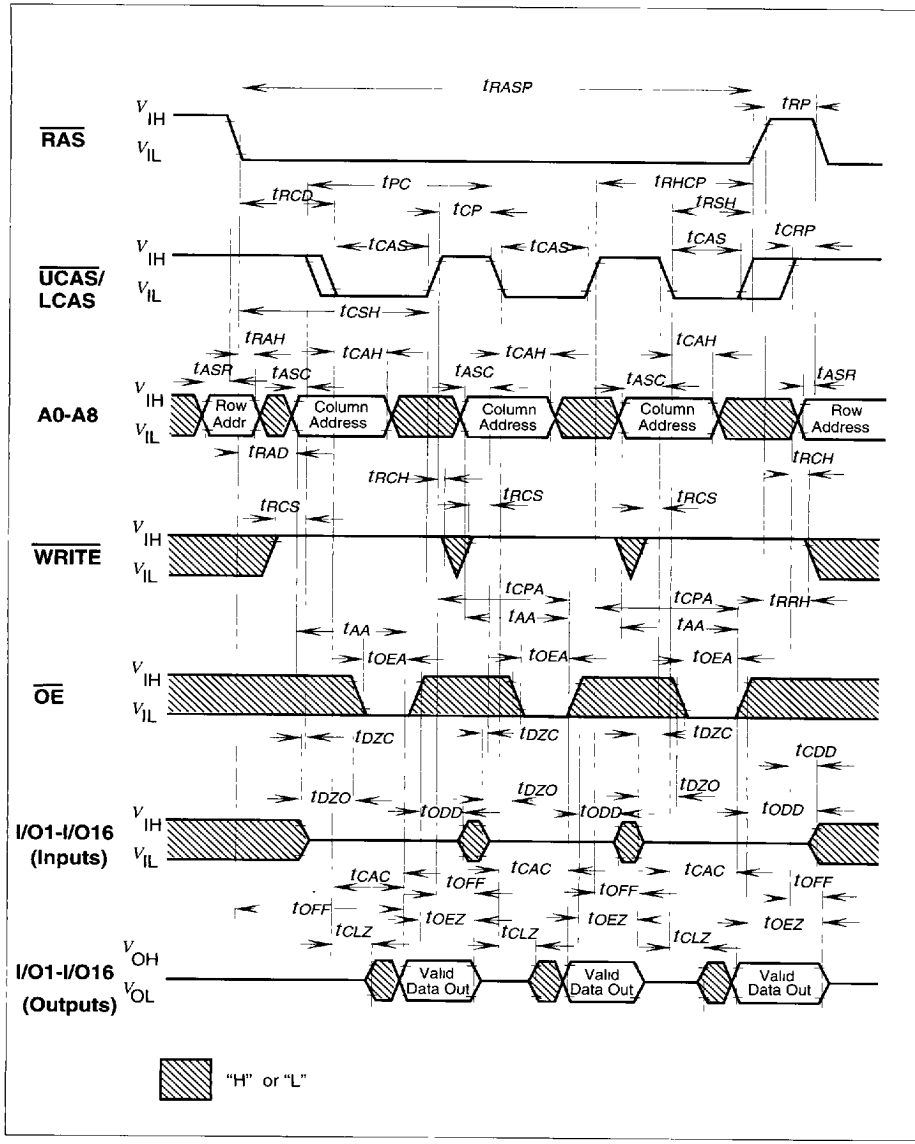
Write Cycle ($\overline{OE}$ Controlled Write)



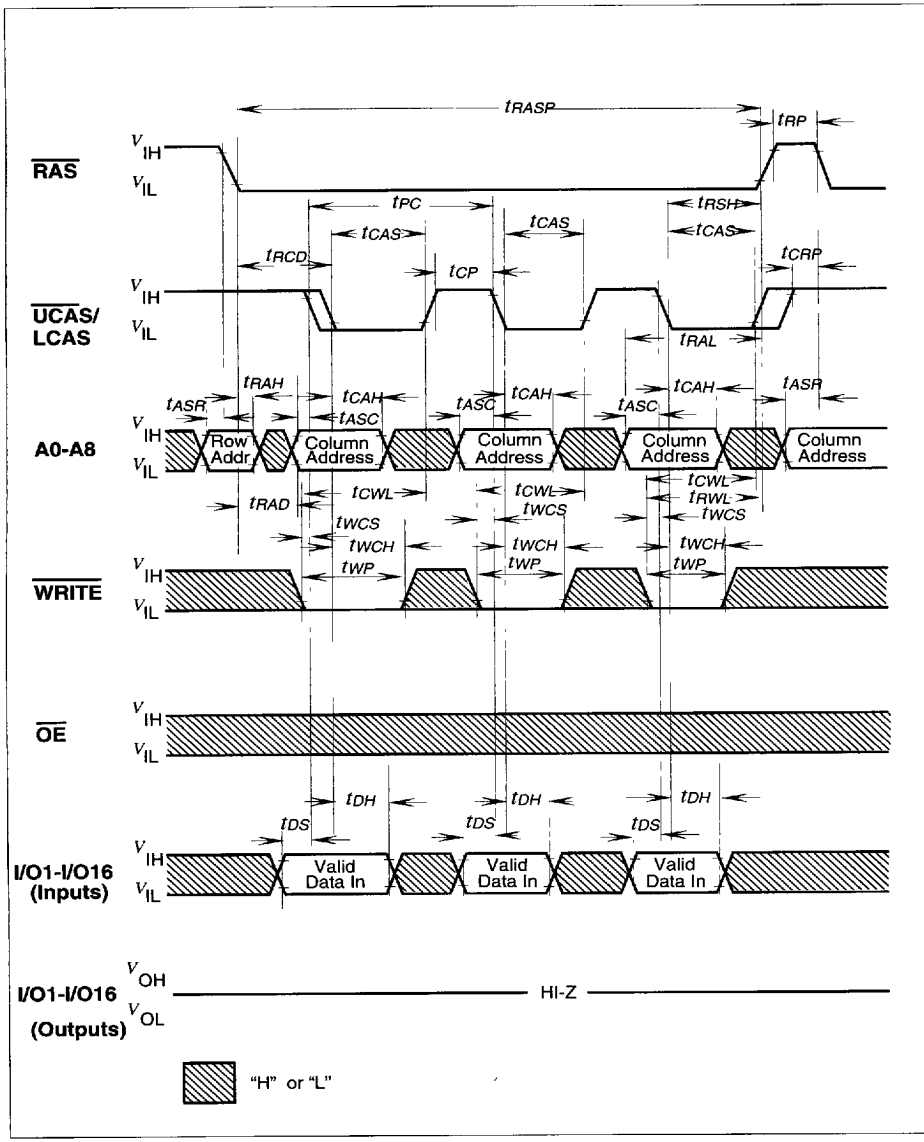
Read-Write (Read-Modify-Write) Cycle



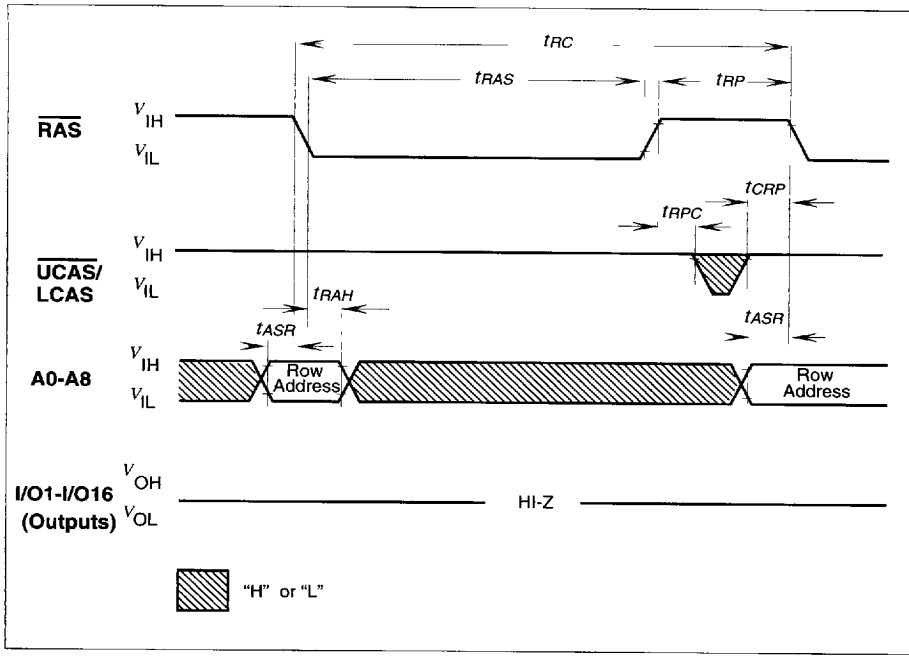
Fast Page Mode Read-Modify-Write Cycle



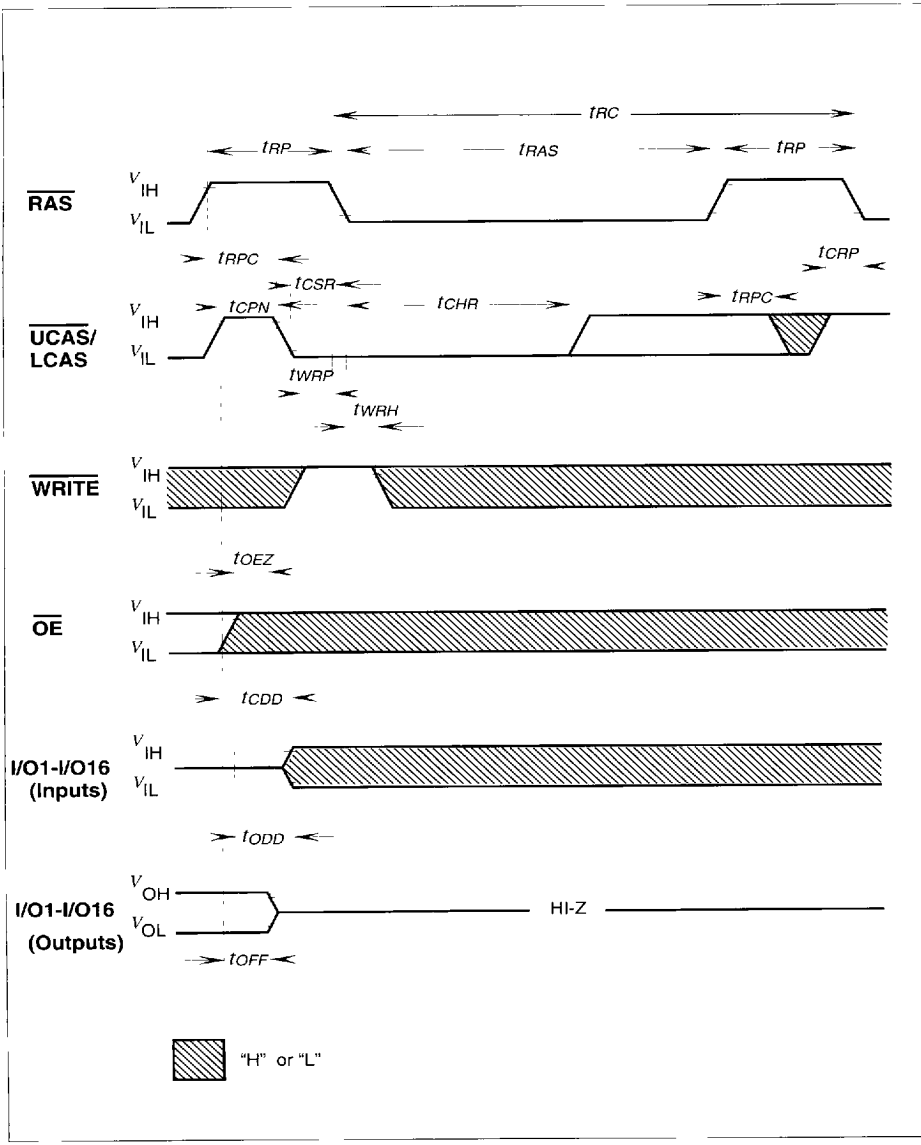
Fast Page Mode Read Cycle



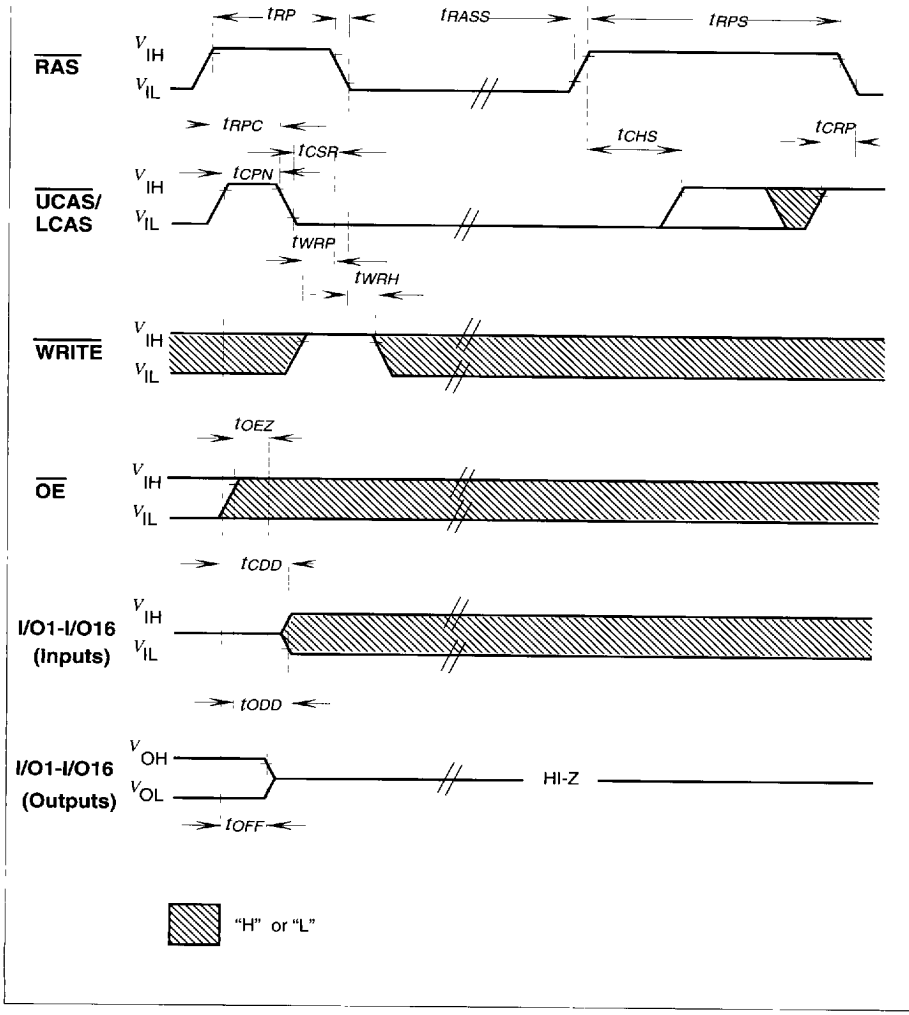
Fast Page Mode Early Write Cycle



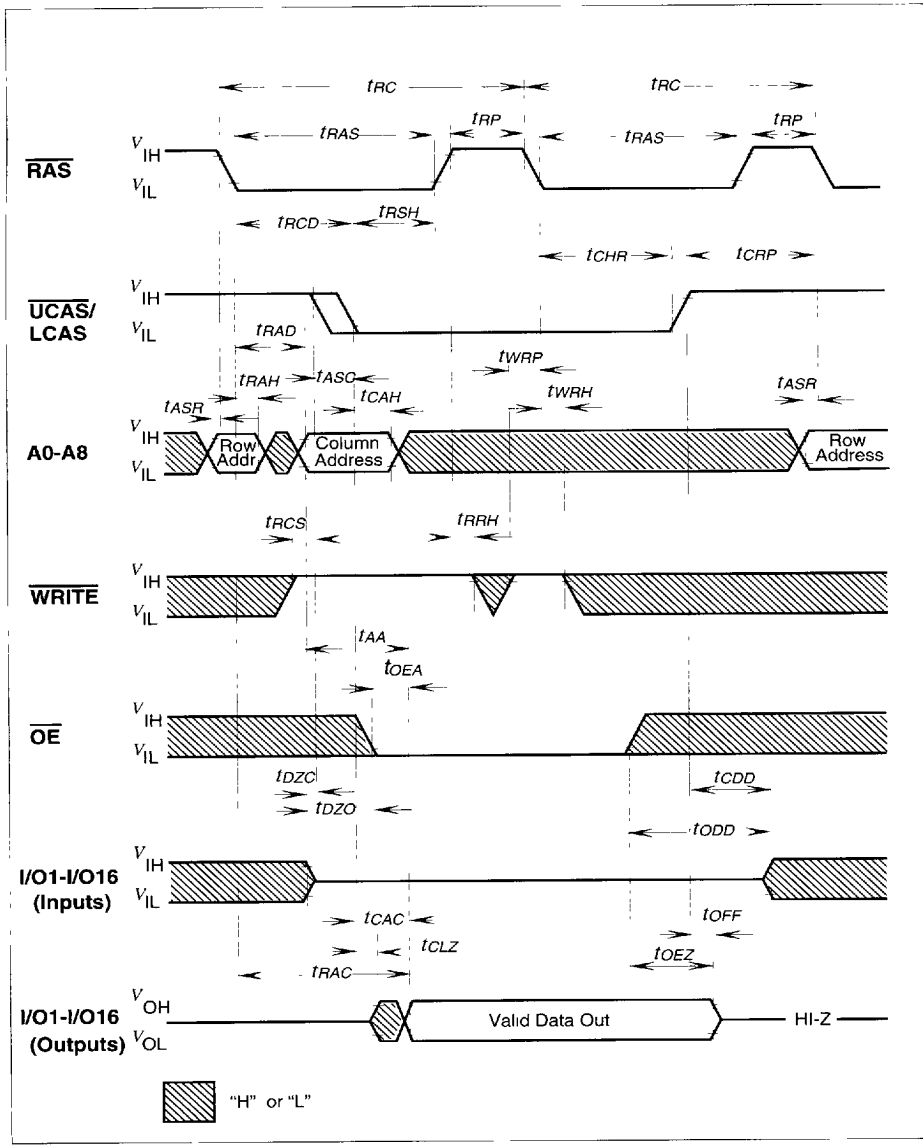
RAS-Only Refresh Cycle



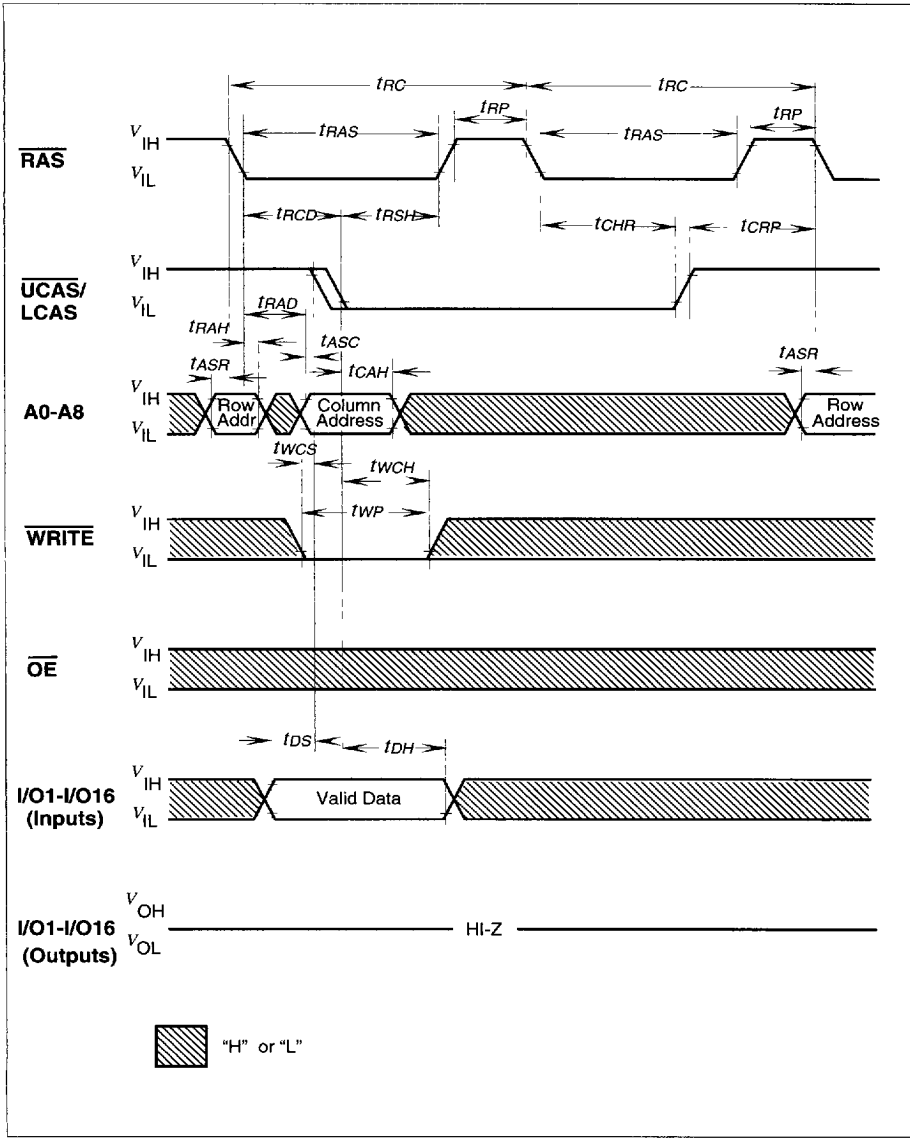
CAS-Before-RAS Refresh Cycle



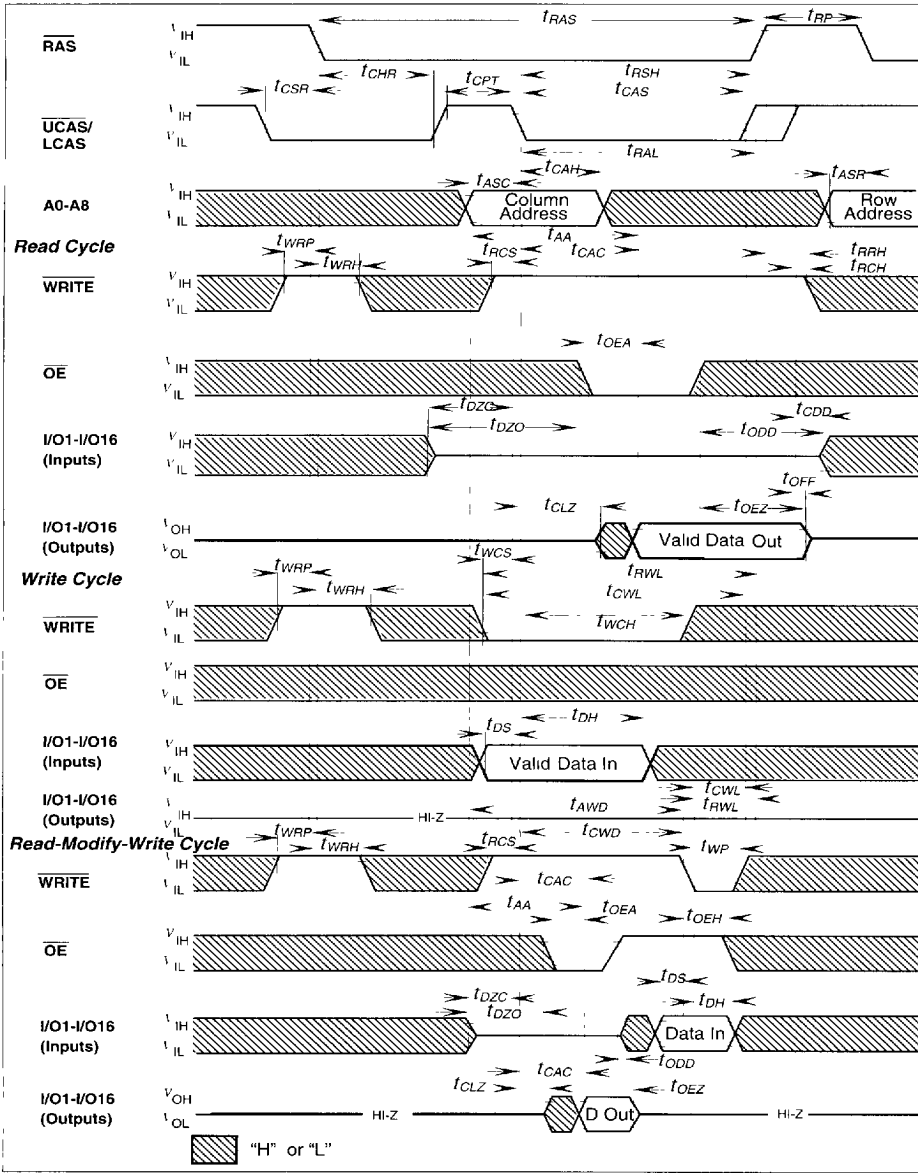
CAS before RAS Self Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Early Write)



CAS/-Before-RAS Refresh Counter Test Cycle