



# HIGH SPEED 2K X 16 DUAL-PORT SRAM

**IDT7133SA/LA  
IDT7143SA/LA**

## Features

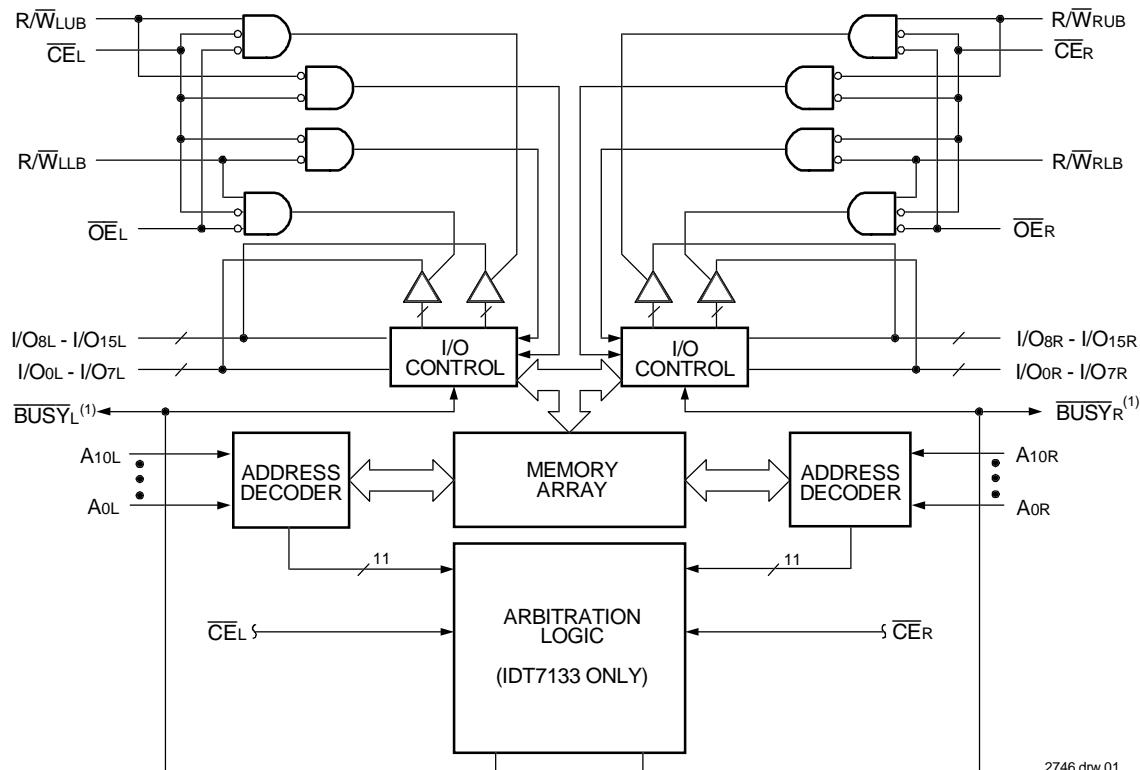
- ◆ High-speed access
  - Military: 25/35/45/55/70/90ns (max.)
  - Industrial: 25/35/55ns (max.)
  - Commercial: 20/25/35/45/55/70/90ns (max.)
- ◆ Low-power operation
  - IDT7133/43SA  
Active: 1150mW (typ.)  
Standby: 5mW (typ.)
  - IDT7133/43LA  
Active: 1050mW (typ.)  
Standby: 1mW (typ.)
- ◆ Versatile control for write: separate write control for lower and upper byte of each port
- ◆ MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- ◆ On-chip port arbitration logic (IDT7133 only)

- ◆  $\overline{\text{BUSY}}$  output flag on IDT7133;  $\overline{\text{BUSY}}$  input on IDT7143
- ◆ Fully asynchronous operation from either port
- ◆ Battery backup operation-2V data retention
- ◆ TTL-compatible; single 5V ( $\pm 10\%$ ) power supply
- ◆ Available in 68-pin ceramic PGA, Flatpack, PLCC and 100-pin TQFP
- ◆ Military product compliant to MIL-PRF-38535 QML
- ◆ Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available for selected speeds

## Description

The IDT7133/7143 are high-speed 2K x 16 Dual-Port Static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7143 "SLAVE" Dual-Port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit-or-wider

## Functional Block Diagram



### NOTE:

1. IDT7133 (MASTER):  $\overline{\text{BUSY}}$  is open drain output and requires pull-up resistor.  
IDT7143 (SLAVE):  $\overline{\text{BUSY}}$  is input.

**JUNE 2000**

memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

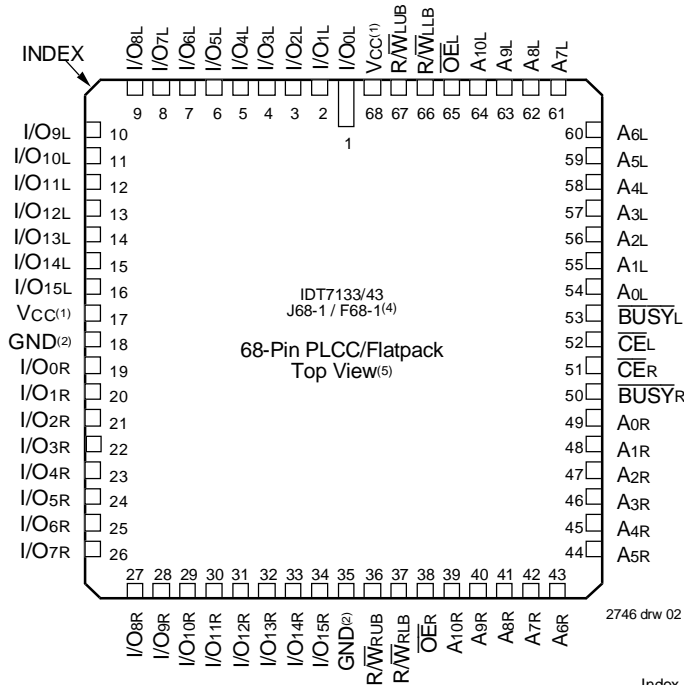
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by  $\overline{CE}$ , permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 1,150mW of power. Low-power (LA)

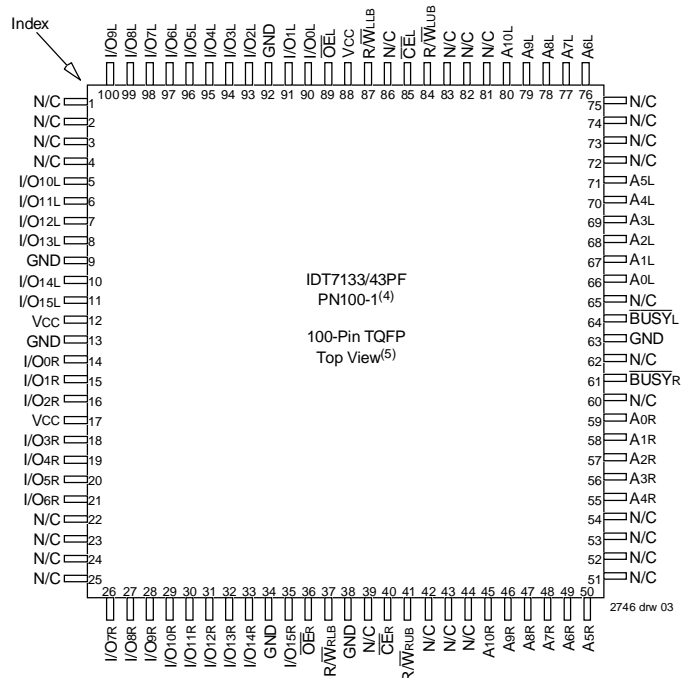
versions offer battery backup data retention capability, with each port typically consuming 200 $\mu$ W for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed in a 68-pin ceramic PGA, 68-pin flatpack, 68-pin PLCC and 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

**Pin Configurations (1,2,3)**



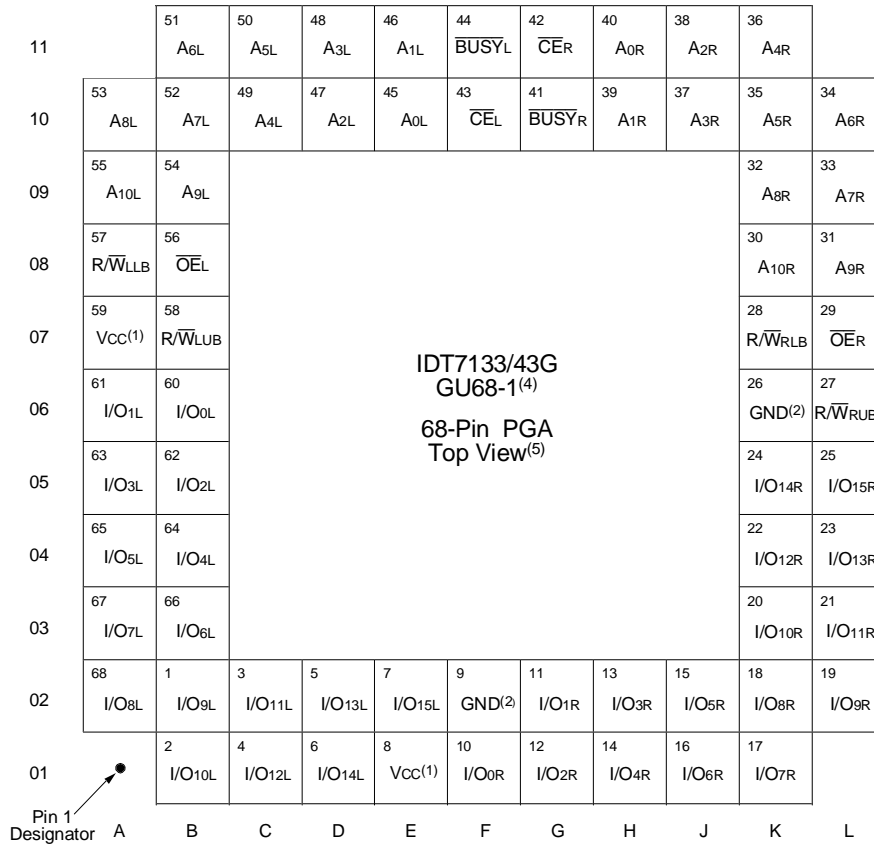
2746 drw 02



2746 drw 03

- NOTES:**
- Both Vcc pins must be connected to the power supply to ensure reliable operation.
  - Both GND pins must be connected to the ground supply to ensure reliable operation.
  - J68-Package body is approximately 0.95 in x 0.95 in x 0.17 in. F68-Package body is approximately 1.18 in x 1.18 in x 0.16 in. PN100-Package body is approximately 14mm x 14mm x 1.4mm.
  - This package code is used to reference the package diagram.
  - This text does not indicate orientation of the actual part-marking.

## Pin Configurations<sup>(1,2,3)</sup> (con't.)



### NOTES:

- Both Vcc pins must be connected to the power supply to ensure reliable operation.
- Both GND pins must be connected to the ground supply to ensure reliable operation.
- Package body is approximately 1.18 in x 1.18 in x 0.16 in.
- This package code is used to reference the package diagram.
- This text does not indicate orientation of the actual part-marking.

2746 drw 04

## Pin Names

Left Port	Right Port	Names
$\overline{\text{CE}}_L$	$\overline{\text{CE}}_R$	Chip Enable
$\overline{\text{R}}/\overline{\text{W}}_{LUB}$	$\overline{\text{R}}/\overline{\text{W}}_{RUB}$	Upper Byte Read/Write Enable
$\overline{\text{R}}/\overline{\text{W}}_{LLB}$	$\overline{\text{R}}/\overline{\text{W}}_{RLB}$	Lower Byte Read/Write Enable
$\overline{\text{OE}}_L$	$\overline{\text{OE}}_R$	Output Enable
A0L - A10L	A0R - A10R	Address
I/O0L - I/O15L	I/O0R - I/O15R	Data Input/Output
$\overline{\text{BUSY}}_L$	$\overline{\text{BUSY}}_R$	Busy Flag
Vcc		Power
GND		Ground

2746 tbl 01

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	-65 to +150	°C
P <sub>T</sub> <sup>(3)</sup>	Power Dissipation	2.0	2.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

2746 tbl 02

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>CC</sub> + 10%.

### Capacitance (T<sub>A</sub> = +25°C, f = 1.0mhz)

Symbol	Parameter <sup>(1)</sup>	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	11	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 3dV	11	pF

2746 tbl 03

**NOTES:**

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

### Maximum Operating Temperature and Supply Voltage<sup>(1,2)</sup>

Grade	Ambient Temperature	GND	V <sub>CC</sub>
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2746 tbl 04

**NOTES:**

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

### Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0 <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

2746 tbl 05

**NOTES:**

- V<sub>IL</sub> (min.) = -1.5V for pulse width less than 10ns.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 10%.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Either port, V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7133SA 7143SA		7133LA 7143LA		Unit
			Min.	Max.	Min.	Max.	
I <sub>L</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = 0V to V <sub>CC</sub>	—	10	—	5	μA
V <sub>OL</sub>	Output Low Voltage (I/O <sub>0</sub> -I/O <sub>15</sub> )	I <sub>OL</sub> = 4mA	—	0.4	—	0.4	V
V <sub>OL</sub>	Open Drain Output Low Voltage (BUSY)	I <sub>OL</sub> = 16mA	—	0.5	—	0.5	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA	2.4	—	2.4	—	V

2746 tbl 06

**NOTE:**

- At V<sub>CC</sub> ≤ 2.0V, input leakages are undefined.

### DC Electrical Characteristics Operating Temperature and Supply Voltage Range<sup>(2)</sup> (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version	7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l, Ind & Military		7133X35 7143X35 Com'l, Ind & Military		Unit
				Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	
I <sub>CC</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ , Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L S	250	310	250	300	240	295	mA
			L	230	280	230	270	210	250	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE} \text{ and } \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L S	—	—	250	330	240	325	mA
			L	—	—	230	300	220	295	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}^{(4)}$ $f = f_{MAX}^{(3)}$ Active Port Outputs Disabled	COM'L S	140	200	140	200	120	180	mA
			L	120	180	100	170	100	160	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE} \text{ and } \overline{CE}_R > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V, f = 0^{(4)}$	COM'L S	1.0	15	1.0	15	1.0	15	mA
			L	0.2	5	0.2	4	0.2	4	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A < 0.2V$ and $\overline{CE}^B > V_{CC} - 0.2V^{(5)}$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ Active Port Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L S	140	190	140	190	120	170	mA
			L	120	170	120	170	100	150	
MIL & IND	S	L	COM'L S	—	—	140	230	120	200	mA
			L	—	—	100	190	100	180	

2746 tbl 07a

Symbol	Parameter	Test Condition	Version	7133X45 7143X45 Com'l & Military		7133X55 7143X55 Com'l, Ind & Military		7133X70/90 7143X70/90 Com'l & Military		Unit
				Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	Typ. <sup>(1)</sup>	Max.	
I <sub>CC</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE} = V_{IL}$ , Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L S	230	290	230	285	230	280	mA
			L	210	250	210	250	210	250	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE} \text{ and } \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(3)}$	COM'L S	25	75	25	70	25	70	mA
			L	25	65	25	60	25	60	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}^{(4)}$ $f = f_{MAX}^{(3)}$ Active Port Outputs Disabled	COM'L S	120	190	120	180	120	180	mA
			L	100	170	100	160	100	160	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE} \text{ and } \overline{CE}_R > V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V, f = 0^{(4)}$	COM'L S	1.0	15	1.0	15	1.0	15	mA
			L	0.2	4	0.2	4	0.2	4	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A < 0.2V$ and $\overline{CE}^B > V_{CC} - 0.2V^{(5)}$ $V_{IN} > V_{CC} - 0.2V$ or $V_{IN} < 0.2V$ Active Port Outputs Disabled $f = f_{MAX}^{(3)}$	COM'L S	120	180	120	170	120	170	mA
			L	100	160	100	150	100	150	
MIL & IND	S	L	COM'L S	120	200	120	200	120	190	mA
			L	100	180	100	180	100	170	

2746 tbl 07b

**NOTES:**

- V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C for Typ., and are not production tested. I<sub>CCDC</sub> = 180mA (typ.)
- 'X' in part number indicates power rating (SA or LA)
- At f = f<sub>MAX</sub>, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ t<sub>rc</sub>, and using "AC Test Conditions" of input levels of GND to 3V.
- f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".

**Data Retention Characteristics**  
(LA Version Only)  $V_{Lc} = 0.2V$ ,  $V_{Hc} = V_{cc} - 0.2V$

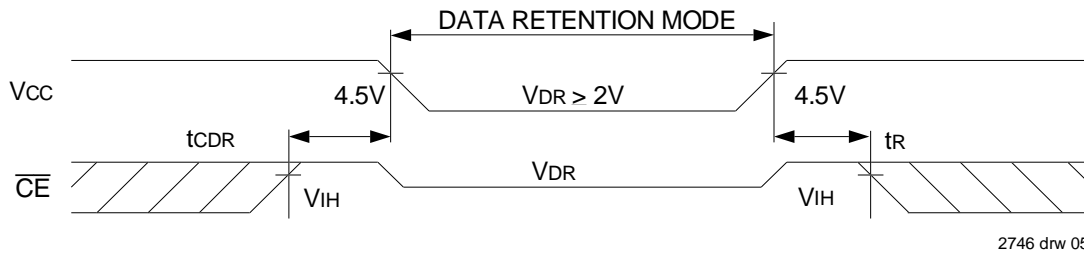
Symbol	Parameter	Test Condition	7133LA/7143LA			Unit
			Min.	Typ. <sup>(1)</sup>	Max.	
$V_{DR}$	$V_{cc}$ for Data Retention	$V_{cc} = 2V$	2.0	—	—	V
$I_{CCDR}$	Data Retention Current	$\overline{CE} \geq V_{Hc}$ $V_{IN} \geq V_{Hc}$ or $\leq V_{Lc}$	MIL. & IND. —	100	4000	$\mu A$
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time		0	—	—	V
$t_R^{(3)}$	Operation Recovery Time		$t_{RC}^{(2)}$	—	—	V

2746 tbl 08

**NOTES:**

- $V_{cc} = 2V$ ,  $T_A = +25^\circ C$ , and are not production tested.
- $t_{RC}$  = Read Cycle Time
- This parameter is guaranteed by device characterization but is not production tested.

**Data Retention Waveform**



2746 drw 05

**AC Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2 and 3

2746 tbl 09

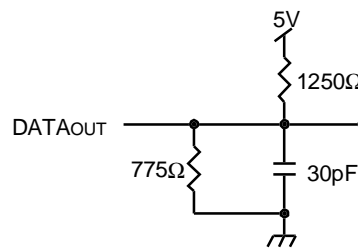


Figure 1. AC Output Test Load

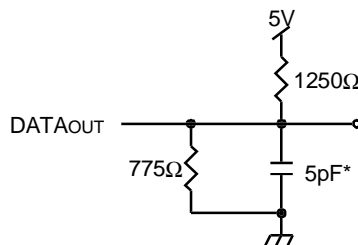


Figure 2. Output Load  
(for  $t_{Lz}$ ,  $t_{Hz}$ ,  $t_{Wz}$ ,  $t_{Oz}$ )  
\*Including scope and jig

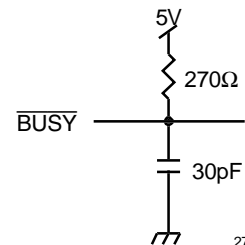


Figure 3.  $\overline{BUSY}$  Output Load  
(IDT7133 only)

2746 drw 06

### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(3)</sup>

Symbol	Parameter	7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l, Ind & Military		7133X35 7143X35 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	20	—	25	—	35	—	ns
t <sub>AA</sub>	Address Access Time	—	20	—	25	—	35	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	20	—	25	—	35	ns
t <sub>AOE</sub>	Output Enable Access Time	—	12	—	15	—	20	ns
t <sub>OH</sub>	Output Hold from Address Change	0	—	0	—	0	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1,2)</sup>	0	—	0	—	0	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	—	20	ns
t <sub>PU</sub>	Chip Enable to Power Up Time <sup>(2)</sup>	0	—	0	—	0	—	ns
t <sub>PD</sub>	Chip Disable to Power Down Time <sup>(2)</sup>	—	20	—	50	—	50	ns

2746 tbl 10a

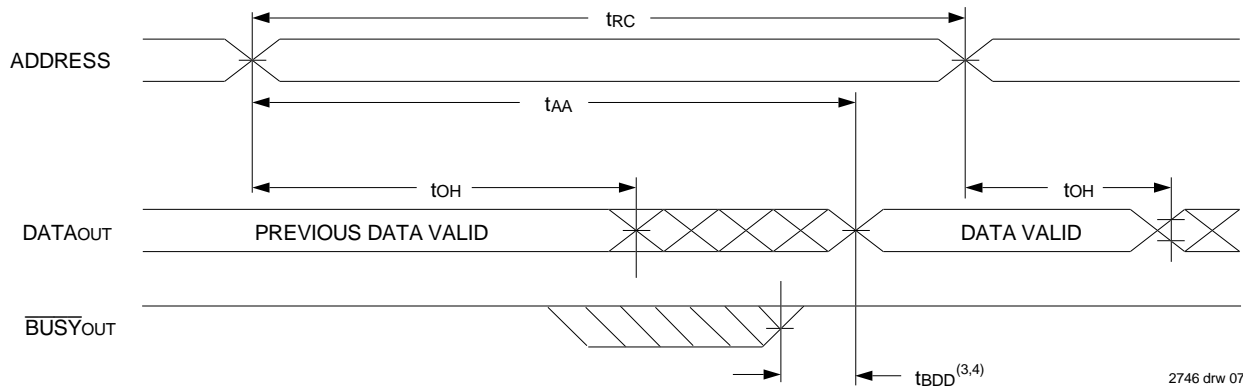
Symbol	Parameter	7133X45 7143X45 Com'l & Military		7133X55 7143X55 Com'l, Ind & Military		7133X70/90 7143X70/90 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	45	—	55	—	70/90	—	ns
t <sub>AA</sub>	Address Access Time	—	45	—	55	—	70/90	ns
t <sub>ACE</sub>	Chip Enable Access Time	—	45	—	55	—	70/90	ns
t <sub>AOE</sub>	Output Enable Access Time	—	25	—	30	—	40/40	ns
t <sub>OH</sub>	Output Hold from Address Change	0	—	0	—	0/0	—	ns
t <sub>LZ</sub>	Output Low-Z Time <sup>(1,2)</sup>	0	—	5	—	5/5	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,2)</sup>	—	20	—	20	—	25/25	ns
t <sub>PU</sub>	Chip Enable to Power Up Time <sup>(2)</sup>	0	—	0	—	0/0	—	ns
t <sub>PD</sub>	Chip Disable to Power Down Time <sup>(2)</sup>	—	50	—	50	—	50/50	ns

2746 tbl 10b

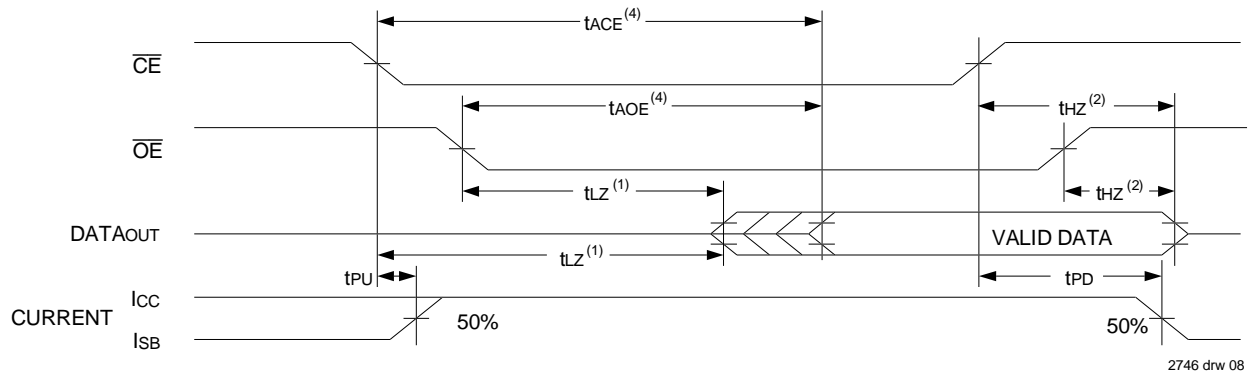
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (SA or LA).

**TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE<sup>(5)</sup>**



**TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE<sup>(5)</sup>**



**NOTES:**

1. Timing depends on which signal is asserted last,  $\overline{OE}$  or  $\overline{CE}$ .
2. Timing depends on which signal is deasserted first,  $\overline{OE}$  or  $\overline{CE}$ .
3.  $t_{BDD}$  delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations,  $\overline{BUSY}$  has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last,  $t_{AOE}$ ,  $t_{ACE}$ ,  $t_{AA}$ , or  $t_{BDD}$ .
5.  $R/W = V_{IH}$ , and the address is valid prior to or coincidental with  $\overline{CE}$  transition LOW.



## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(5)</sup>

Symbol	Parameter	7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l, Ind & Military		7133X35 7143X35 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>								
t <sub>WC</sub>	Write Cycle Time <sup>(3)</sup>	20	—	25	—	35	—	ns
t <sub>EW</sub>	Chip Enable to End-of-Write	15	—	20	—	25	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	15	—	20	—	25	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	15	—	20	—	25	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,2)</sup>	—	12	—	15	—	20	ns
t <sub>DH</sub>	Data Hold Time <sup>(4)</sup>	0	—	0	—	0	—	ns
t <sub>WZ</sub>	Write Enable to Output in High-Z <sup>(1,2)</sup>	—	12	—	15	—	20	ns
t <sub>OW</sub>	Output Active from End-of-Write <sup>(1,2,4)</sup>	0	—	0	—	0	—	ns

2746 tbl 11a

Symbol	Parameter	7133X45 7143X45 Com'l & Military		7133X55 7143X55 Com'l, Ind & Military		7133X70/90 7143X70/90 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>WRITE CYCLE</b>								
t <sub>WC</sub>	Write Cycle Time <sup>(3)</sup>	45	—	55	—	70/90	—	ns
t <sub>EW</sub>	Chip Enable to End-of-Write	30	—	40	—	50/50	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	30	—	40	—	50/50	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0/0	—	ns
t <sub>WP</sub>	Write Pulse Width	30	—	40	—	50/50	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0/0	—	ns
t <sub>DW</sub>	Data Valid to End-of-Write	20	—	25	—	30/30	—	ns
t <sub>HZ</sub>	Output High-Z Time <sup>(1,2)</sup>	—	20	—	20	—	25/25	ns
t <sub>DH</sub>	Data Hold Time <sup>(4)</sup>	5	—	5	—	5/5	—	ns
t <sub>WZ</sub>	Write Enable to Output in High-Z <sup>(1,2)</sup>	—	20	—	20	—	25/25	ns
t <sub>OW</sub>	Output Active from End-of-Write <sup>(1,2,4)</sup>	5	—	5	—	5/5	—	ns

2746 tbl 11b

### NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage from the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but not production tested.
3. For MASTER/SLAVE combination,  $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$ , since  $R\bar{W} = V_{IL}$  must occur after  $t_{BAA}$ .
4. The specification for  $t_{DH}$  must be met by the device supplying write data to the RAM under all operation conditions. Although  $t_{DH}$  and  $t_{OW}$  values will vary over voltage and temperature, the actual  $t_{DH}$  will always be smaller than the actual  $t_{OW}$ .
5. 'X' in part number indicates power rating (SA or LA).

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(6)</sup>

Symbol	Parameter	7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l, Ind & Military		7133X35 7143X35 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>BUS<math>\bar{Y}</math> TIMING (For MASTER 71V33)</b>								
tBAA	BUS $\bar{Y}$ Access Time from Address	—	20	—	20	—	30	ns
tBDA	BUS $\bar{Y}$ Disable Time from Address	—	20	—	20	—	30	ns
tBAC	BUS $\bar{Y}$ Access Time from Chip Enable	—	20	—	20	—	25	ns
tBDC	BUS $\bar{Y}$ Disable Time from Chip Enable	—	17	—	20	—	25	ns
tWDD	Write Pulse to Data Delay <sup>(1)</sup>	—	40	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay <sup>(1)</sup>	—	30	—	35	—	45	ns
tBDD	BUS $\bar{Y}$ Disable to Valid Data <sup>(2)</sup>	—	25	—	30	—	35	ns
tAPS	Arbitration Priority Set-up Time <sup>(3)</sup>	5	—	5	—	5	—	ns
tWH	Write Hold After BUS $\bar{Y}$ <sup>(6)</sup>	20	—	20	—	25	—	ns
<b>BUS<math>\bar{Y}</math> INPUT TIMING (For SLAVE 71V43)</b>								
tWB	BUS $\bar{Y}$ Input to Write <sup>(4)</sup>	0	—	0	—	0	—	ns
tWH	Write Hold After BUS $\bar{Y}$ <sup>(6)</sup>	20	—	20	—	25	—	ns
tWDD	Write Pulse to Data Delay <sup>(1)</sup>	—	40	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay <sup>(1)</sup>	—	30	—	35	—	45	ns

2746 tbl 12a

Symbol	Parameter	7133X45 7143X45 Com'l & Military		7133X55 7143X55 Com'l, Ind & Military		7133X70/90 7143X70/90 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>BUS<math>\bar{Y}</math> TIMING (For MASTER 71V33)</b>								
tBAA	BUS $\bar{Y}$ Access Time from Address	—	40	—	40	—	45/45	ns
tBDA	BUS $\bar{Y}$ Disable Time from Address	—	40	—	40	—	45/45	ns
tBAC	BUS $\bar{Y}$ Access Time from Chip Enable	—	30	—	35	—	35/35	ns
tBDC	BUS $\bar{Y}$ Disable Time from Chip Enable	—	25	—	30	—	30/30	ns
tWDD	Write Pulse to Data Delay <sup>(1)</sup>	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay <sup>(1)</sup>	—	55	—	55	—	70/70	ns
tBDD	BUS $\bar{Y}$ Disable to Valid Data <sup>(2)</sup>	—	40	—	40	—	40/40	ns
tAPS	Arbitration Priority Set-up Time <sup>(3)</sup>	5	—	5	—	5/5	—	ns
tWH	Write Hold After BUS $\bar{Y}$ <sup>(6)</sup>	30	—	30	—	30/30	—	ns
<b>BUS<math>\bar{Y}</math> INPUT TIMING (For SLAVE 71V43)</b>								
tWB	BUS $\bar{Y}$ Input to Write <sup>(4)</sup>	0	—	0	—	0/0	—	ns
tWH	Write Hold After BUS $\bar{Y}$ <sup>(6)</sup>	30	—	30	—	30/30	—	ns
tWDD	Write Pulse to Data Delay <sup>(1)</sup>	—	80	—	80	—	90/90	ns
tDDD	Write Data Valid to Read Data Delay <sup>(1)</sup>	—	55	—	55	—	70/70	ns

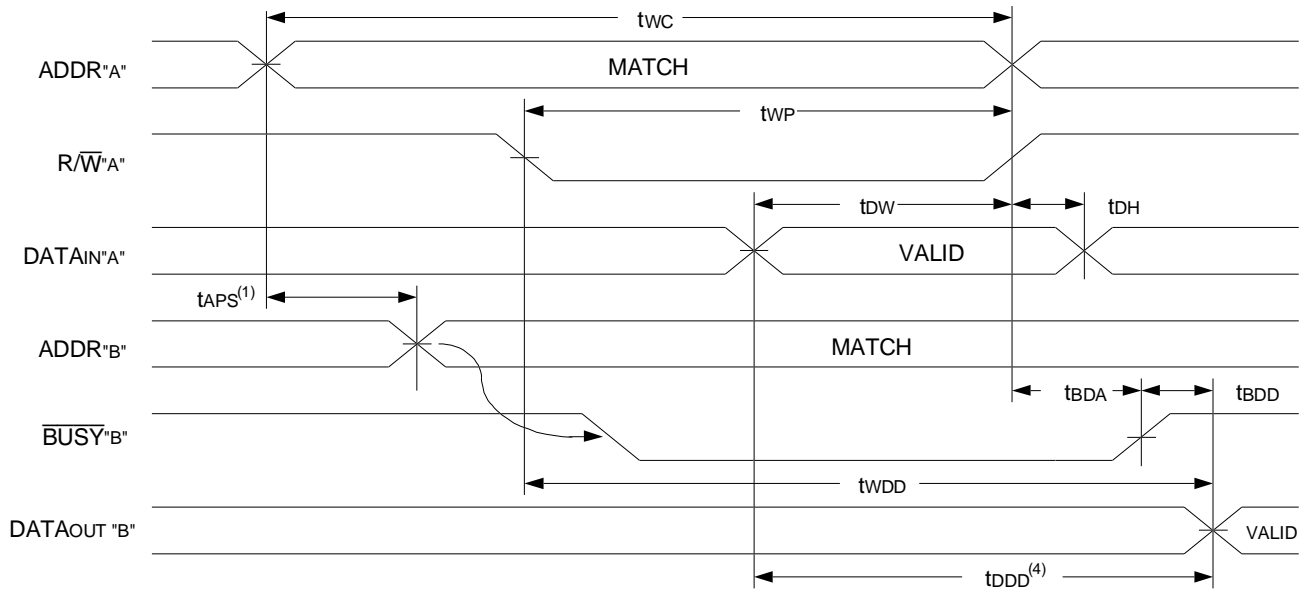
2746 tbl 12b

### NOTES:

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".
2. tDDD is calculated parameter and is greater of 0, tWDD - tWP (actual) or tDDD - tDW (actual).
3. To ensure that the earlier of the two ports wins.
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part number indicates power rating (SA or LA).



### Timing Waveform of Write with Port-to-Port Read and $\overline{\text{BUSY}}^{(1,2,3)}$

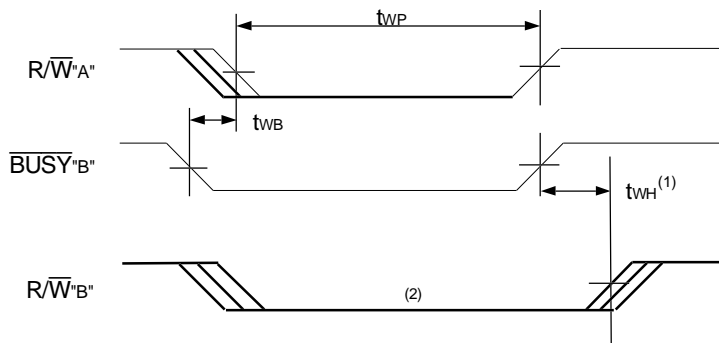


2746 drw 11

**NOTES:**

1. To ensure that the earlier of the two ports wins,  $t_{APS}$  is ignored for Slave (IDT7143).
2.  $\overline{\text{CE}}_L = \overline{\text{CE}}_R = V_{IL}$
3.  $\overline{\text{OE}} = V_{IL}$  for the reading port.
4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

### Timing Waveform of Write with $\overline{\text{BUSY}}^{(3)}$

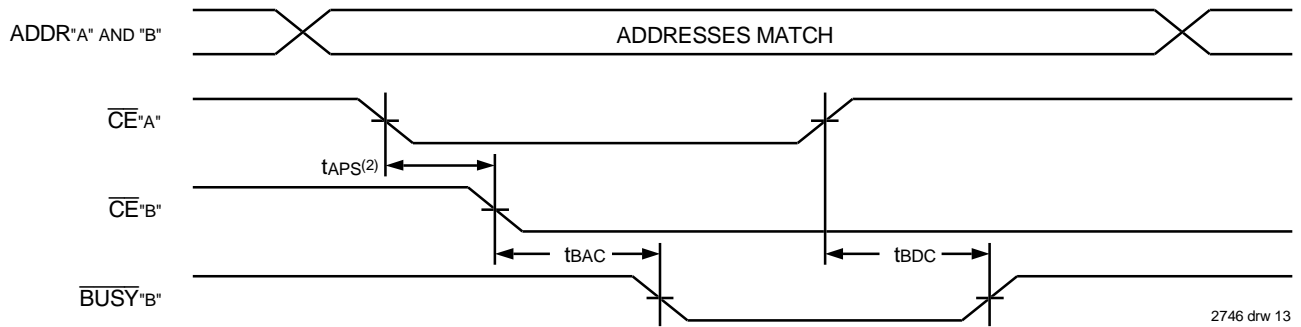


2746 drw 12

**NOTES:**

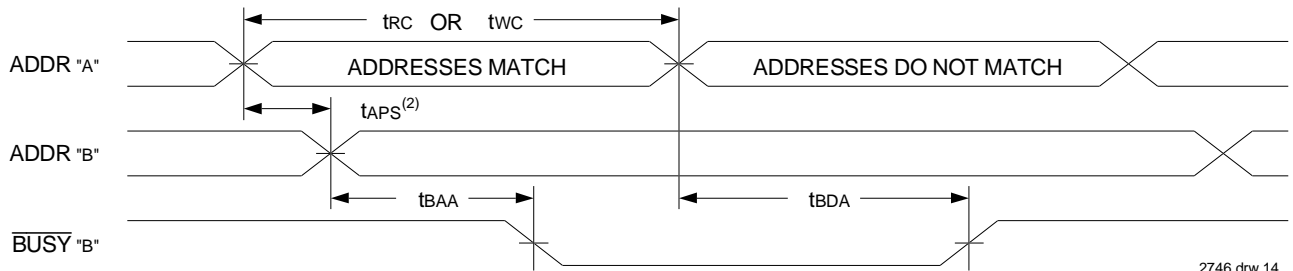
1.  $t_{WH}$  must be met for both  $\overline{\text{BUSY}}$  input (IDT7143, slave) and output (IDT7133, master).
2.  $\overline{\text{BUSY}}$  is asserted on port "B" blocking  $\overline{\text{R/W}}_B$ , until  $\overline{\text{BUSY}}_B$  goes HIGH.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

### Timing Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by $\overline{\text{CE}}$ Timing<sup>(1)</sup>



2746 drw 13

### Timing Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by Addresses<sup>(1)</sup>



2746 drw 14

**NOTES:**

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If  $t_{\text{APS}}$  is not satisfied, the  $\overline{\text{BUSY}}$  will be asserted on one side or the other, but there is no guarantee on which side  $\overline{\text{BUSY}}$  will be asserted (IDT7133 only).

## Functional Description

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7133/43 has an automatic power down feature controlled by  $\overline{CE}$ . The  $\overline{CE}$  controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ( $\overline{CE}$  HIGH). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Truth Table 1.

## Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The  $\overline{BUSY}$  pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a  $\overline{BUSY}$  indication, the write signal is gated internally to prevent the write from proceeding.

The use of  $\overline{BUSY}$  logic is not required or desirable for all applications. In some cases it may be useful to logically OR the  $\overline{BUSY}$  outputs together and use any  $\overline{BUSY}$  indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of  $\overline{BUSY}$  logic is not desirable, the  $\overline{BUSY}$  logic can be disabled by using the IDT7143 (SLAVE). In the IDT7143, the  $\overline{BUSY}$  pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the  $\overline{BUSY}$  pins HIGH. If desired, unintended write operations can be prevented to a port by tying the  $\overline{BUSY}$  pin for that port LOW. The  $\overline{BUSY}$  outputs on the IDT 7133 RAM are open drain and require pull-up resistors.

## Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7133/43 RAM array in width while using  $\overline{BUSY}$  logic, one master part is used to decide which side of the RAM array will receive a  $\overline{BUSY}$  indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the  $\overline{BUSY}$  signal as a write inhibit signal. Thus on the IDT7133 RAM the  $\overline{BUSY}$  pin is an output and on the IDT7143 RAM, the  $\overline{BUSY}$  pin is an input (see Figure 3).

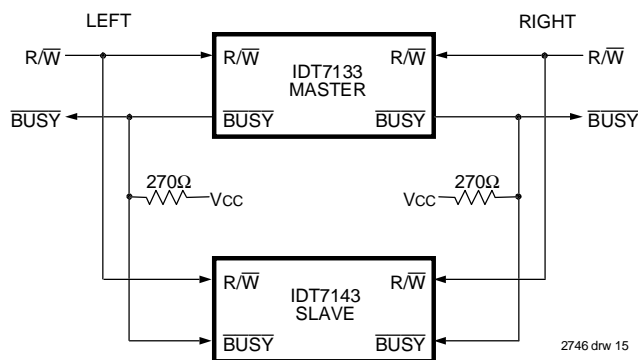


Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT7133 (MASTER) and the IDT7143 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its  $\overline{BUSY}_L$  while another activates its  $\overline{BUSY}_R$  signal. Both sides are now  $\overline{BUSY}$  and the CPUs will await indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has  $\overline{BUSY}$  inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the  $\overline{BUSY}$  input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past  $\overline{BUSY}$  to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to  $\overline{BUSY}$  from the MASTER.

### Truth Table I – Non-Contention Read/Write Control<sup>(4)</sup>

LEFT OR RIGHT PORT <sup>(1)</sup>						Function
R/ $\overline{W}$ LB	R/ $\overline{W}$ UB	$\overline{CE}$	$\overline{OE}$	I/O0-7	I/O8-15	
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, ISB2, ISB4
X	X	H	X	Z	Z	CE <sub>R</sub> = CE <sub>L</sub> = V <sub>H</sub> , Power Down Mode, ISB1 or ISB3
L	L	L	X	DATA <sub>IN</sub>	DATA <sub>IN</sub>	Data on Lower Byte and Upper Byte Written into Memory <sup>(2)</sup>
L	H	L	L	DATA <sub>IN</sub>	DATA <sub>OUT</sub>	Data on Lower Byte Written into Memory <sup>(2)</sup> , Data in Memory Output on Upper Byte <sup>(3)</sup>
H	L	L	L	DATA <sub>OUT</sub>	DATA <sub>IN</sub>	Data in Memory Output on Lower Byte <sup>(3)</sup> , Data on Upper Byte Written into Memory <sup>(2)</sup>
L	H	L	H	DATA <sub>IN</sub>	Z	Data on Lower Byte Written into Memory <sup>(2)</sup>
H	L	L	H	Z	DATA <sub>IN</sub>	Data on Upper Byte Written into Memory <sup>(2)</sup>
H	H	L	L	DATA <sub>OUT</sub>	DATA <sub>OUT</sub>	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

2746 tbl 13

**NOTES:**

1. A<sub>0L</sub> - A<sub>10L</sub> ≠ A<sub>0R</sub> - A<sub>10R</sub>
2. If  $\overline{BUSY}$  = LOW, data is not written.
3. If  $\overline{BUSY}$  = LOW, data may not be valid, see t<sub>WDD</sub> and t<sub>DDQ</sub> timing.
4. "H" = HIGH, "L" = LOW, "X" = Don't Care, "Z" = High-Impedance, "LB" = Lower Byte, "UB" = Upper Byte

### Truth Table II — Address $\overline{BUSY}$ Arbitration

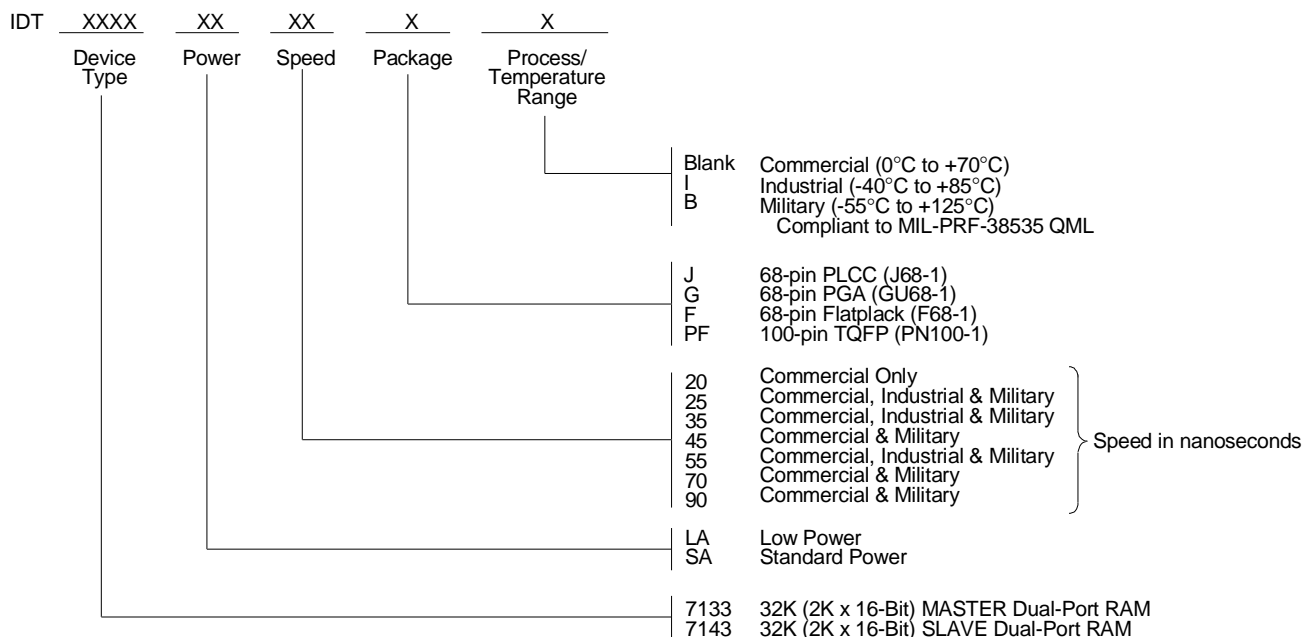
Inputs			Outputs		Function
$\overline{CE}_L$	$\overline{CE}_R$	A <sub>0L</sub> -A <sub>10L</sub> A <sub>0R</sub> -A <sub>10R</sub>	$\overline{BUSY}_L$ <sup>(1)</sup>	$\overline{BUSY}_R$ <sup>(1)</sup>	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit <sup>(3)</sup>

2746 tbl 14

**NOTES:**

1. Pins  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$  are both outputs on the IDT7133 (MASTER). Both are inputs on the IDT7143 (SLAVE). On Slaves the  $\overline{BUSY}$  input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t<sub>APS</sub> is not met, either  $\overline{BUSY}_L$  or  $\overline{BUSY}_R$  = V<sub>IL</sub> will result  $\overline{BUSY}_L$  and  $\overline{BUSY}_R$  outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when  $\overline{BUSY}_L$  outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when  $\overline{BUSY}_R$  outputs are driving LOW regardless of actual logic level on the pin.

## Ordering Information



2746 drw 16

## Datasheet Document History

- 12/18/98: Initiated datasheet document history  
Converted to new format  
Cosmetic and typographical corrections  
Added additional notes to pin configurations  
Page 2 corrected PN100 pinout
- 2/17/99: Corrected PF ordering code
- 3/9/99: Cosmetic and typographical corrections
- 6/9/99: Changed drawing format
- 10/1/99: Added Industrial Temperature Ranges and removed corresponding notes
- 11/10/99: Replaced IDT logo
- 4/1/00: Changed ±500mV to 0mV in notes  
Page 2 Fixed overbar in pinout
- 6/26/00: Page 4 Increased storage temperature parameters  
Clarified TA parameter  
Page 5 DC Electrical parameters—changed wording from "open" to "disabled"



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**  
800-345-7015 or 408-727-6116  
fax: 408-492-8674  
www.idt.com

**for Tech Support:**  
831-754-4613  
DualPortHelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.