

### Features

- Secondary side high speed SR controller
- DCM, CrCM and CCM flyback topologies
- 200V proprietary IC technology
- Max 500KHz switching frequency
- Anti-bounce logic and UVLO protection
- 7A peak turn off drive current
- Micropower start-up & ultra low quiescent current
- 10.7/14.5V gate drive clamp
- 50ns turn-off propagation delay
- Vcc range from 11.3V to 20V
- Direct sensing of MOSFET drain voltage
- Minimal component count
- Simple design
- Lead-free
- Compatible with 1W Standby, Energy Star, CECP, etc.

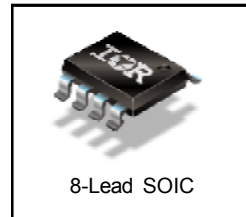
### Description

IR1167S is a smart secondary side driver IC designed to drive N-Channel power MOSFETs used as synchronous rectifiers in isolated Flyback converters.

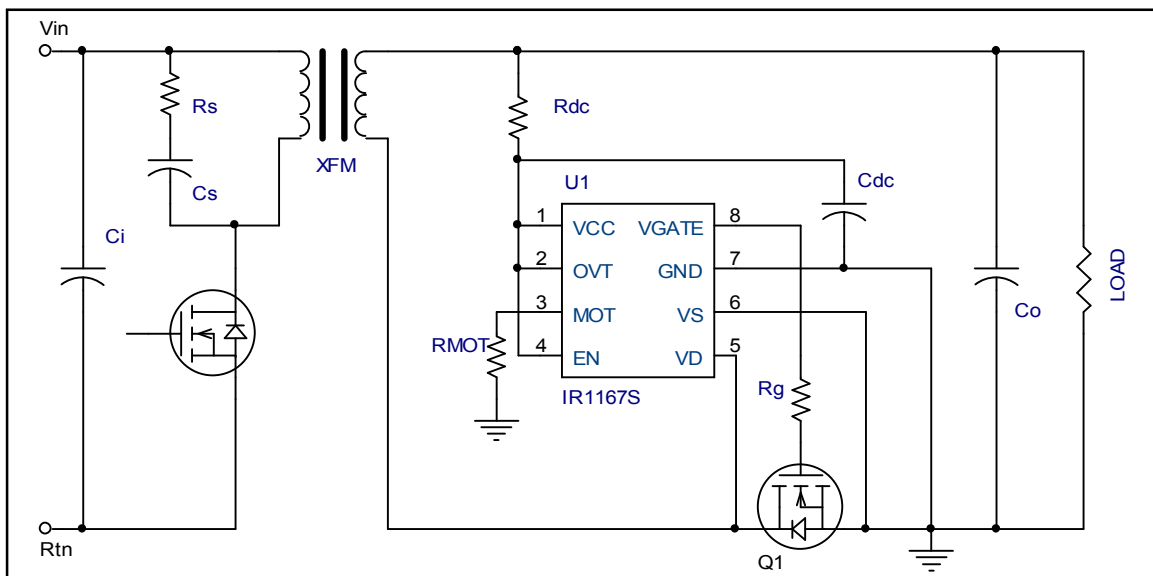
The IC can control one or more paralleled N-MOSFETs to emulate the behavior of Schottky diode rectifiers. The drain to source voltage is sensed differentially to determine the polarity of the current and turn the power switch on and off in proximity of the zero current transition.

Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in continuous, discontinuous and critical current mode operation and both fixed and variable frequency modes.

### Package



### IR1167 Application Diagram



## Absolute Maximum Ratings

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions are not implied. All voltages are absolute voltages referenced to GND. Thermal resistance and power dissipation are measured under board mounted and still air conditions.

Parameters	Symbol	Min.	Max.	Units	Remarks
Supply Voltage	V <sub>CC</sub>	-0.3	20	V	
Enable Voltage	V <sub>EN</sub>	-0.3	20	V	
Cont. Drain Sense Voltage	V <sub>D</sub>	-3	200	V	
Pulse Drain Sense Voltage	V <sub>D</sub>	-5	200	V	
Source Sense Voltage	V <sub>S</sub>	-3	20	V	
Gate Voltage	V <sub>GATE</sub>	-0.3	20	V	V <sub>CC</sub> =20V, Gate off
Operating Junction Temperature	T <sub>J</sub>	-40	150	°C	
Storage Temperature	T <sub>S</sub>	-55	150	°C	
Thermal Resistance	R <sub>θJA</sub>		128	°C/W	SOIC-8
Package Power Dissipation	P <sub>D</sub>		970	mW	SOIC-8, T <sub>AMB</sub> =25°C
ESD Protection	V <sub>ESD</sub>		2	kV	Human Body Model*
Switching Frequency	f <sub>sw</sub>		500	kHz	

\* Per EIA/JESD22-A114-B( discharging a 100pF capacitor through a 1.5kΩ series resistor).

## Electrical Characteristics

The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range  $T_J$  from  $-25^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Typical values represent the median values, which are related to  $25^{\circ}\text{C}$ . If not otherwise stated, a supply voltage of  $V_{CC} = 15\text{V}$  is assumed for test condition.

### Supply Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Supply Voltage Operating Range	$V_{CC}$	12		18	V	GBD
$V_{CC}$ Turn On Threshold	$V_{CC\text{ON}}$	9.8	10.5	11.3	V	
$V_{CC}$ Turn Off Threshold (Under Voltage Lock Out)	$V_{CC\text{UVLO}}$	8.4	9	9.7	V	
$V_{CC}$ Turn On/Off Hysteresis	$V_{CC\text{HYST}}$	1.4	1.55	1.7	V	
Operating Current	$I_{CC}$		8.5	10	mA	IR1167A $C_{\text{LOAD}}=1\text{nF}$ , $f_{\text{SW}} = 400\text{kHz}$
			50	65		
			10.3	12		IR1167B $C_{\text{LOAD}}=1\text{nF}$ , $f_{\text{SW}} = 400\text{kHz}$
			66	80		
Quiescent Current	$I_{\text{QCC}}$		1.8	2.2	mA	
Start-up Current	$I_{\text{CCSTART}}$		100	200	$\mu\text{A}$	$V_{\text{CC}}=V_{\text{CCON}} - 0.1\text{V}$
Sleep Current	$I_{\text{SLEEP}}$		150	200	$\mu\text{A}$	$V_{\text{EN}}=0\text{V}$ , $V_{\text{CC}} = 15\text{V}$
Enable Voltage High	$V_{\text{ENHI}}$	2.15	2.75	3.2	V	
Enable Voltage Low	$V_{\text{ENLO}}$	1.2	1.6	2	V	
Enable Pull-up Resistance	$R_{\text{EN}}$		1.5		$\text{M}\Omega$	GBD

### Comparator Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Turn-off Threshold	$V_{\text{TH1}}$	-7	-3.5	0	mV	$\text{OVT} = 0\text{V}$ , $V_{\text{S}}=0\text{V}$
		-15	-10.5	-7		OVT floating, $V_{\text{S}}=0\text{V}$
		-23	-19	-15		$\text{OVT} = V_{\text{CC}}$ , $V_{\text{S}}=0\text{V}$
Turn-on Threshold	$V_{\text{TH2}}$	-150		-50	mV	
Hysteresis	$V_{\text{HYST}}$		55		mV	
Input Bias Current	$I_{\text{BIAS1}}$		1	7.5	$\mu\text{A}$	$V_{\text{D}} = -50\text{mV}$
Input Bias Current	$I_{\text{BIAS2}}$		30	100	$\mu\text{A}$	$V_{\text{D}} = 200\text{V}$
Comparator Input Offset	$V_{\text{OFFSET}}$			2	mV	GBD
Input CM Voltage Range	$V_{\text{CM}}$	-0.15		2	V	

### One-Shot Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Blanking pulse duration	$t_{\text{BLANK}}$	9	15	25	$\mu\text{s}$	
Reset Threshold	$V_{\text{TH3}}$		2.5		V	$V_{\text{CC}}=10\text{V}$ - GBD
			5.4		V	$V_{\text{CC}}=20\text{V}$ - GBD
Hysteresis	$V_{\text{HYST3}}$		40		mV	$V_{\text{CC}}=10\text{V}$ - GBD

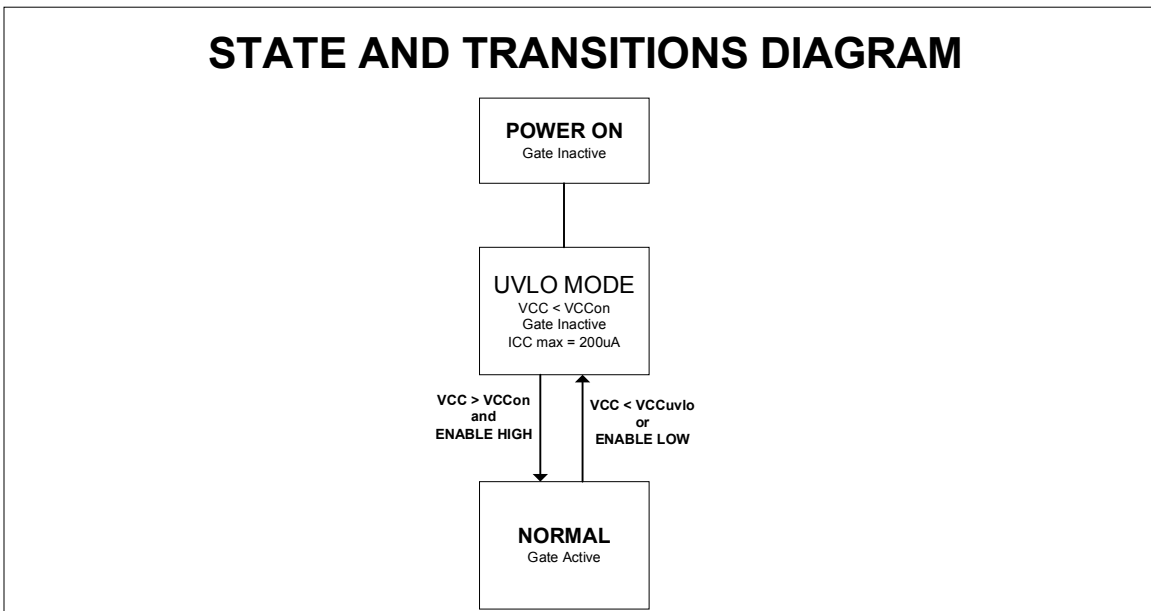
## Minimum On Time Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Minimum on time	$T_{ONmin}$	190	240	290	ns	$R_{MOT} = 5k\Omega, V_{CC} = 12V$
		2.4	3	3.6	$\mu s$	$R_{MOT} = 75k\Omega, V_{CC} = 12V$

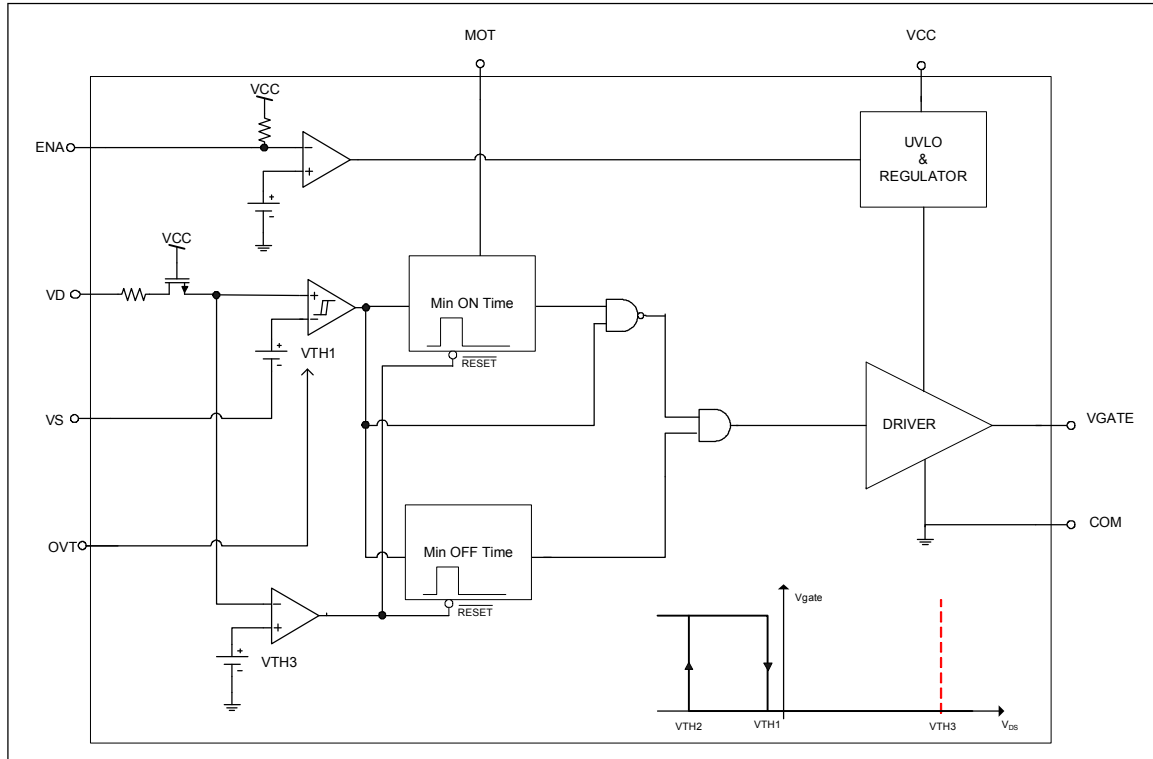
## Gate Driver Section

Parameters	Symbol	Min.	Typ.	Max.	Units	Remarks
Gate Low Voltage	$V_{GLO}$		0.3	0.5	V	$I_{GATE} = 200mA$
Gate High Voltage	$V_{GTH}$	9	10.7	12.5	V	IR1167A - $V_{CC} = 12V-18V$ (internally clamped)
Gate High Voltage	$V_{GTH}$	12	14.5	16.5	V	IR1167B - $V_{CC} = 12V-18V$ (internally clamped)
Rise Time	$t_{r1}$		18		ns	$C_{LOAD} = 1nF, V_{CC} = 12V$
	$t_{r2}$		125		ns	$C_{LOAD} = 10nF, V_{CC} = 12V$
Fall Time	$t_{f1}$		10		ns	$C_{LOAD} = 1nF, V_{CC} = 12V$
	$t_{f2}$		30		ns	$C_{LOAD} = 10nF, V_{CC} = 12V$
Turn on Propagation Delay	$t_{don}$		60	80	ns	$V_{DS}$ to $V_{GATE}$ -100mV overdrive
Turn off Propagation Delay	$t_{doff}$		40	65	ns	$V_{DS}$ to $V_{GATE}$ -100mV overdrive
Pull up Resistance	$r_{up}$		4		$\Omega$	$I_{GATE} = 1A - GBD$
Pull down Resistance	$r_{down}$		0.7		$\Omega$	$I_{GATE} = -200mA$
Output Peak Current (source)	$I_{O source}$		2		A	$C_{LOAD} = 10nF - GBD$
Output Peak Current (sink)	$I_{O sink}$		7		A	$C_{LOAD} = 10nF - GBD$

\*\* Guaranteed by Design



## Block Diagram



## Lead Assignments & Definitions

Lead Assignment	Pin#	Symbol	Description
	1	VCC	Supply Voltage
	2	OVT	Offset Voltage Trimming
	3	MOT	Minimum On Time
	4	EN	Enable
	5	VD	FET Drain Sensing
	6	VS	FET Source Sensing
	7	GND	Ground
	8	GATE	Gate Drive Output

## Detailed Pin Description

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### **GND: Ground**

This is ground potential pin of the integrated control circuit. The internal devices and gate driver are referenced to this point.

### **MOT: Minimum On Time**

The MOT programming pin controls the amount of minimum on time. Once  $V_{TH2}$  is crossed for the first time, the gate signal will become active and turn on the power FET. Spurious ringings and oscillations can trigger the input comparator off. The MOT blanks the input comparator keeping the FET on for a minimum time.

The MOT is programmed between 200ns and 3us (typ.) by using a resistor referenced to GND.

### **OVT: Offset Voltage Trimming**

The OVT pin will program the amount of input offset voltage for the turn-off threshold  $V_{TH1}$ .

The pin can be optionally tied to ground, to VCC or left floating, to select 3 ranges of input offset trimming. This programming feature allows for accommodating different RDSon MOSFETs.

### **GATE: Gate Drive Output**

This is the gate drive output of the IC. Drive voltage is internally limited and provides 2A peak source and 7A peak sink capability. Although this pin can be directly connected to the power MOSFET gate, the use of minimal gate resistor is recommended, especially when putting multiple FETs in parallel. Care must be taken in order to keep the gate loop as short and as small as possible in order to achieve optimal switching performance.

### **VS: Source Voltage Sense**

VS is the differential sense pin for the power MOSFET Source. This pin must not be connected directly to the power ground pin (7) but must be used to create a

kelvin contact as close as possible to the power MOSFET source pin.

### **VD: Drain Voltage Sense**

VD is the voltage sense pin for the power MOSFET Drain. This is a high voltage pin and particular care must be taken in properly routing the connection to the power MOSFET drain.

Additional filtering and or current limiting on this pin is not recommended as it would limit switching performance of the IC.

### **VCC: Power Supply**

This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.

To prevent noise problems, a bypass ceramic capacitor connected to Vcc and GND should be placed as close as possible to the IR1167S.

This pin is internally clamped.

### **EN: Enable**

This pin is used to activate the IC "sleep" mode by pulling the voltage level below 2.5V (typ). In sleep mode the IC will consume a minimum amount of current. However all switching functions will be disabled and the gate will be inactive.

## STATES OF OPERATION

### UVLO/Sleep Mode

The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage,  $V_{CC\ ON}$ . During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of  $I_{CC\ START}$ . The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of  $V_{CC} < V_{CC\ UVLO}$  occurs.

The sleep mode is initiated by pulling the EN pin below 2.5V (typ). In this mode the IC is essentially shut down and draws a very low quiescent supply current.

### Normal Mode

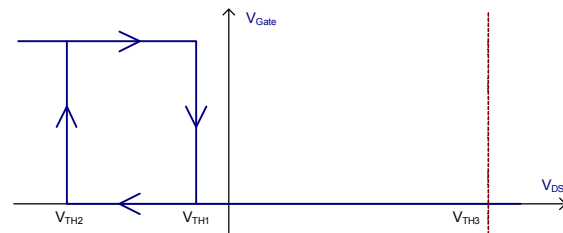
The IC enters in normal operating mode once the UVLO voltage has been exceeded. At this point the gate driver is operating and the IC will draw a maximum of  $I_{CC}$  from the supply voltage source.

## GENERAL DESCRIPTION

The IR1167 Smart Rectifier IC can emulate the operation of diode rectifier by properly driving a Synchronous Rectifier (SR) MOSFET.

The direction of the rectified current is sensed by the input comparator using the power MOSFET  $R_{DSon}$  as a shunt resistance and the GATE pin of the MOSFET is driven accordingly.

Internal blanking logic is used to prevent spurious transitions and guarantee operation in continuous (CCM), discontinuous (DCM) and critical (CrCM) conduction mode.



Input comparator thresholds

The modes of operation for a Flyback circuit differ mainly for the turn-off phase of the SR switch, while the turn-on phase of the secondary switch (which correspond to the turn off of the primary side switch) is identical.

### Turn-on phase

When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative  $V_{DS}$  voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold  $V_{TH2}$ .

At that point the IR1167 will drive the gate of MOSFET on which will in turn cause the conduction voltage  $V_{DS}$  to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off; hence, a Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.

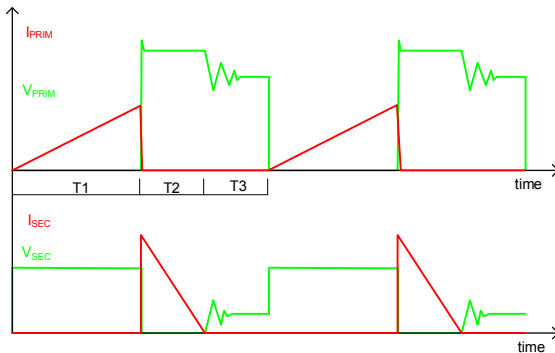
The programmed MOT will limit also the minimum duty

cycle of the SR MOSFET and, as a consequence, the max duty cycle of the primary side switch.

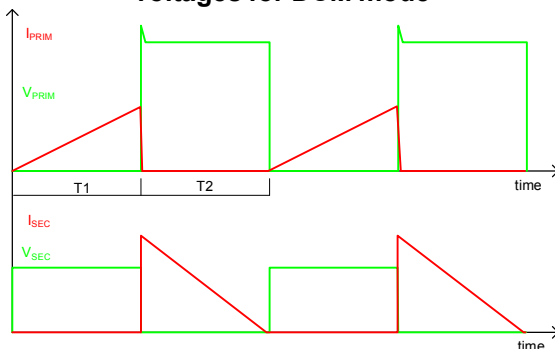
### DCM/CrCM Turn-off phase

Once the SR MOSFET has been turned on, it will remain on until the rectified current will decay to the level where  $V_{DS}$  will cross the turn-off threshold  $V_{TH1}$ . This will happen differently depending on the mode of operation.

In DCM the current will cross the threshold with a relatively low  $di/dt$ . Once the threshold is crossed, the current will start flowing again through the body diode,



Primary and secondary currents and voltages for DCM mode



Primary and secondary currents and voltages for CrCM mode

causing the  $V_{DS}$  voltage to jump negative. Depending on the amount of residual current,  $V_{DS}$  may trigger once again the turn on threshold: for this reason  $V_{TH2}$

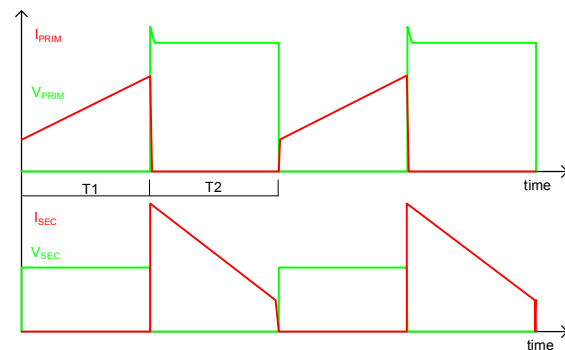
is blanked for a certain amount of time ( $T_{BLANK}$ ) after  $V_{TH1}$  has been triggered.

The blanking time is internally set. As soon as  $V_{DS}$  crosses the positive threshold  $V_{TH3}$  also the blanking time is terminated and the IC is ready for next conduction cycle.

### CCM Turn-off phase

In CCM mode the turn off transition is much steeper and  $di/dt$  involved is much higher. The turn on phase is identical to DCM or CrCM and therefore won't be repeated here.

During the SR FET conduction phase the current will decay linearly, and so will  $V_{DS}$  on the SR FET.



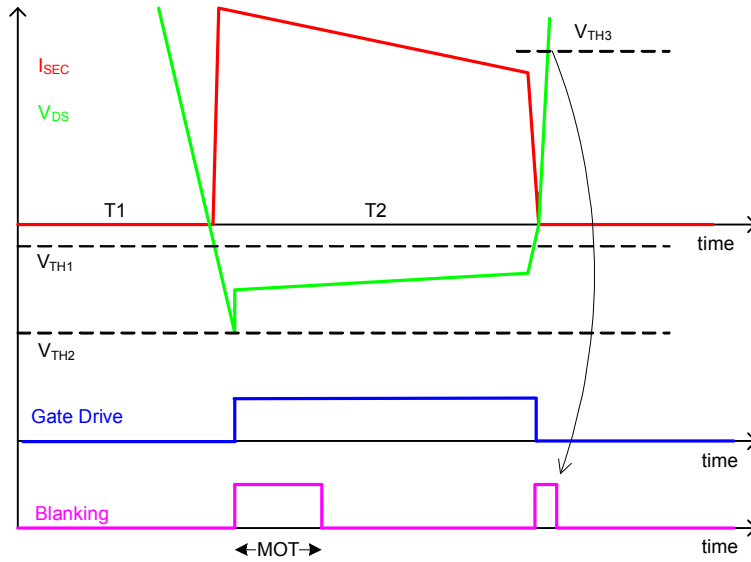
Primary and secondary currents and voltages for CCM mode

Once the primary switch will start to turn back on, the SR FET current will rapidly decrease crossing  $V_{TH1}$  and turning the gate off.

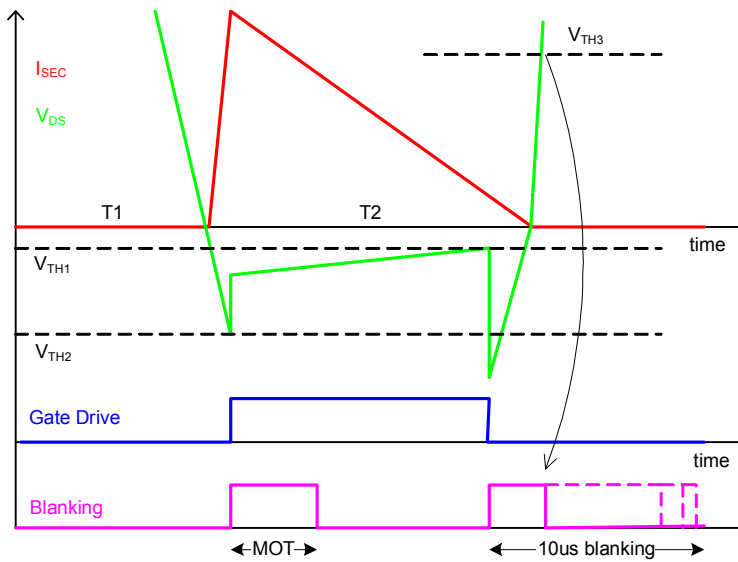
The turn off speed is critical to avoid cross conduction on the primary side and reduce switching losses.

also in this case a blanking period will be applied, but given the very fast nature of this transition, it will be reset as soon as  $V_{DS}$  crosses  $V_{TH3}$ .

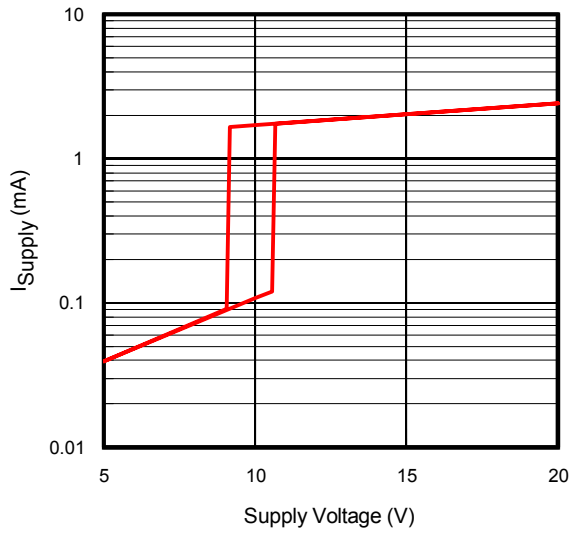




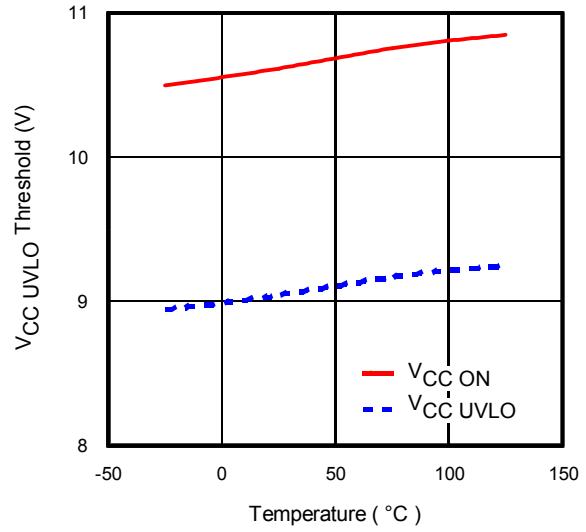
**Secondary side CCM operation**



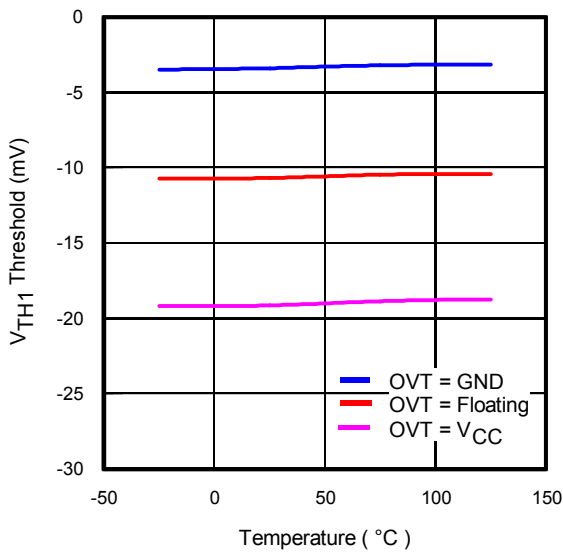
**Secondary side DCM/CrCM operation**



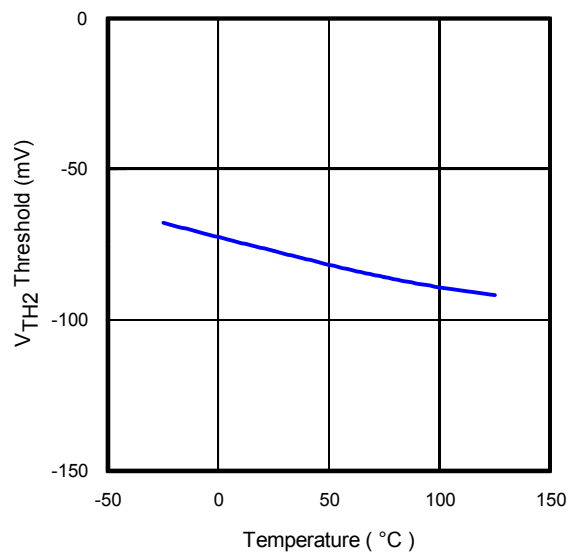
**Fig 1.** Supply Current vs. Supply Voltage



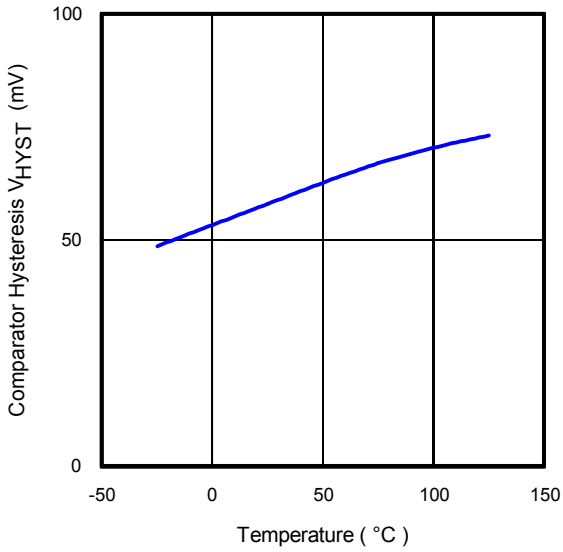
**Fig 2.** Under Voltage Lockout vs. Temp.



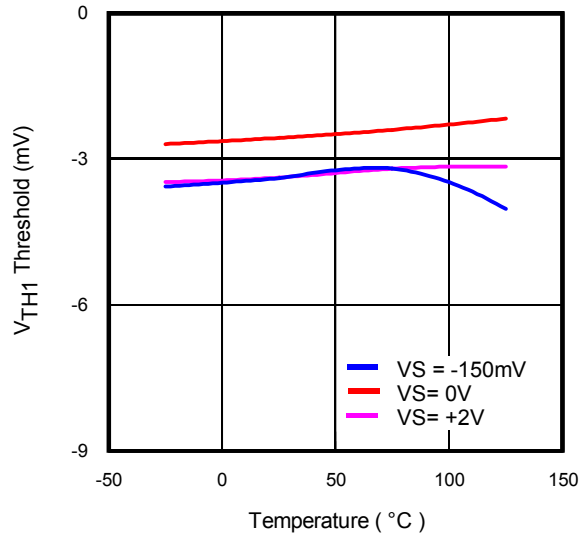
**Fig 3.** V<sub>TH1</sub> vs. Temp.



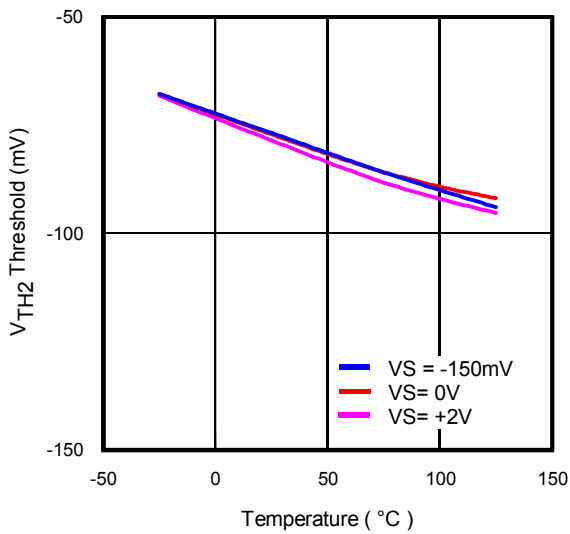
**Fig 4.** V<sub>TH2</sub> vs. Temp.



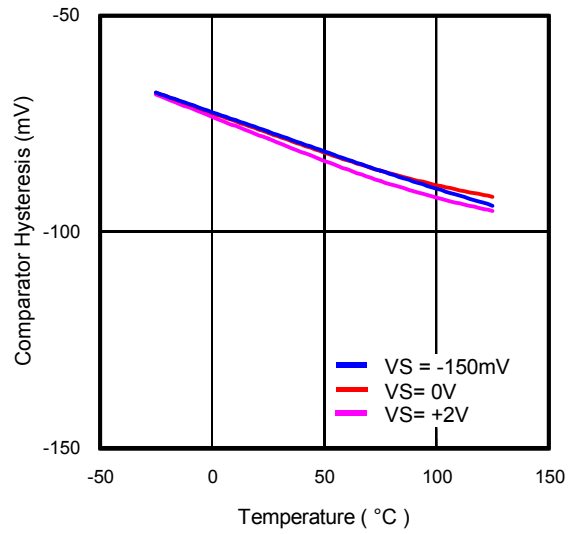
**Fig 5.** Comparator Hysteresis vs. Temp.



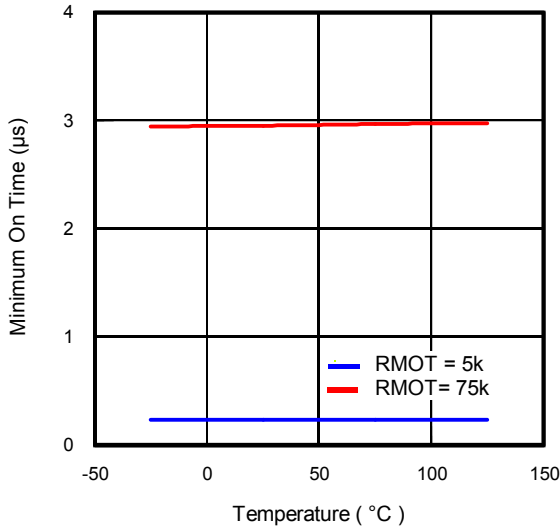
**Fig 6.**  $V_{TH1}$  vs. Temp. and Common Mode (OVT=GND)



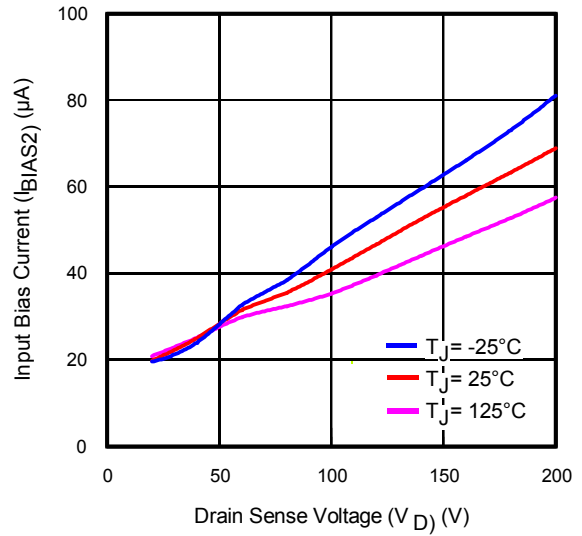
**Fig 7.**  $V_{TH2}$  vs. Temp. and Common Mode (OVT=GND)



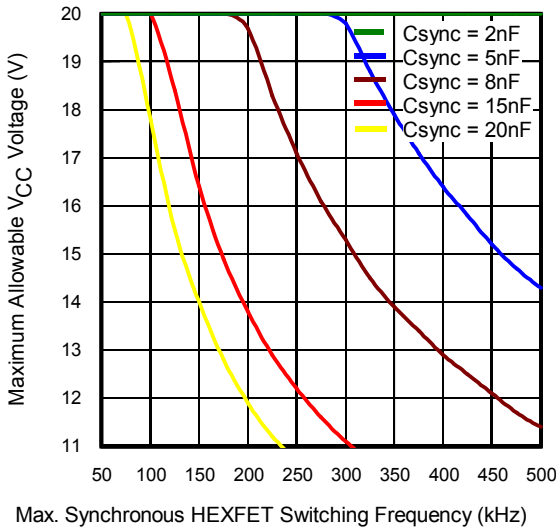
**Fig 8.** Comparator Hysteresis vs. Temp. and Common Mode (OVT=GND)



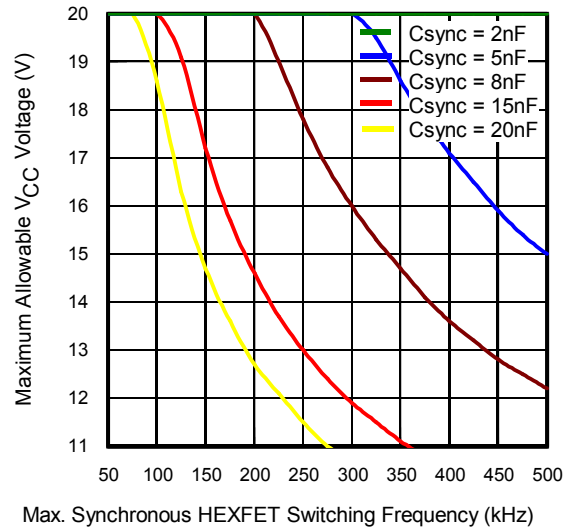
**Fig 9.** MOT vs. Temp.



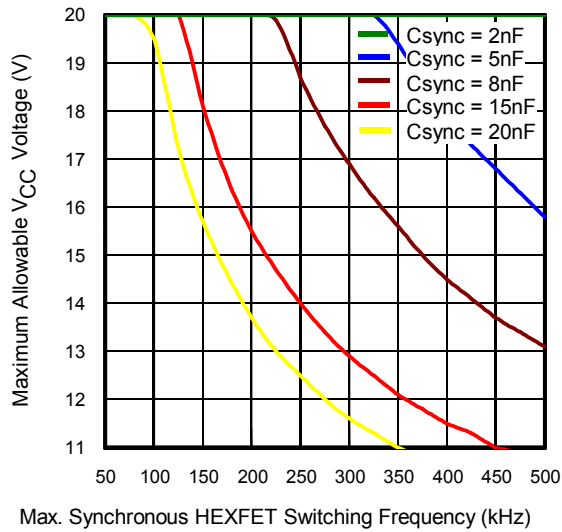
**Fig 10.** Input Bias Current vs. V<sub>D</sub>.



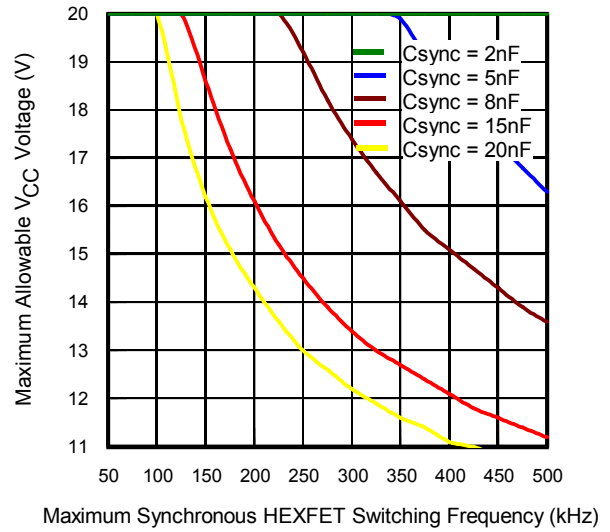
**Fig 11.** Max. V<sub>CC</sub> Voltage vs. Synchronous Rectifier Switching Freq, T<sub>J</sub>=125 C, T<sub>IC</sub> = 85 C, external R<sub>G</sub>=1Ω, 1Ω HEXFET Gate Resistance included



**Fig 12.** Max. V<sub>CC</sub> Voltage vs. Synchronous Rectifier Switching Freq, T<sub>J</sub>=125 C, T<sub>IC</sub> = 85 C, external R<sub>G</sub>=2Ω, 1Ω HEXFET Gate Resistance included

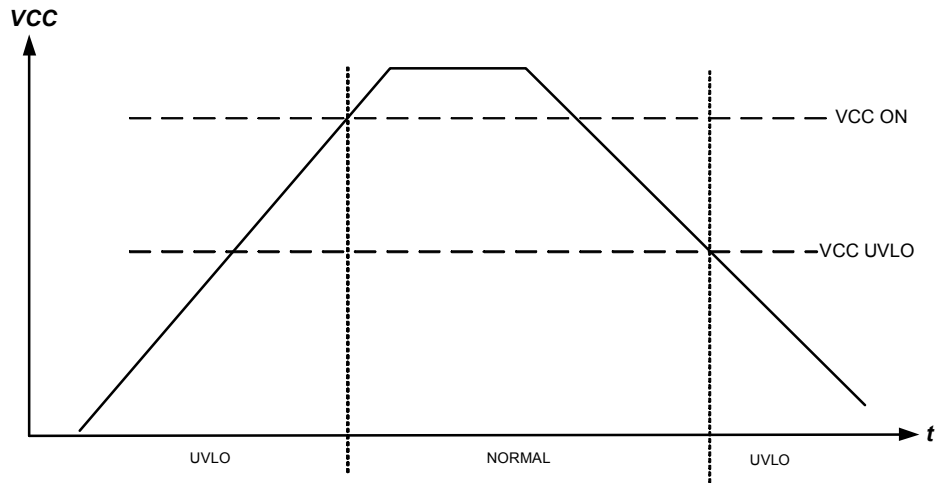


**Fig 13.** Max.  $V_{CC}$  Voltage vs. Synchronous Rectifier Switching Freq,  $T_J=125\text{ C}$ ,  $T_{IC} = 85\text{ C}$ , external  $R_G=4\Omega$ ,  $1\Omega$  HEXFET Gate Resistance included

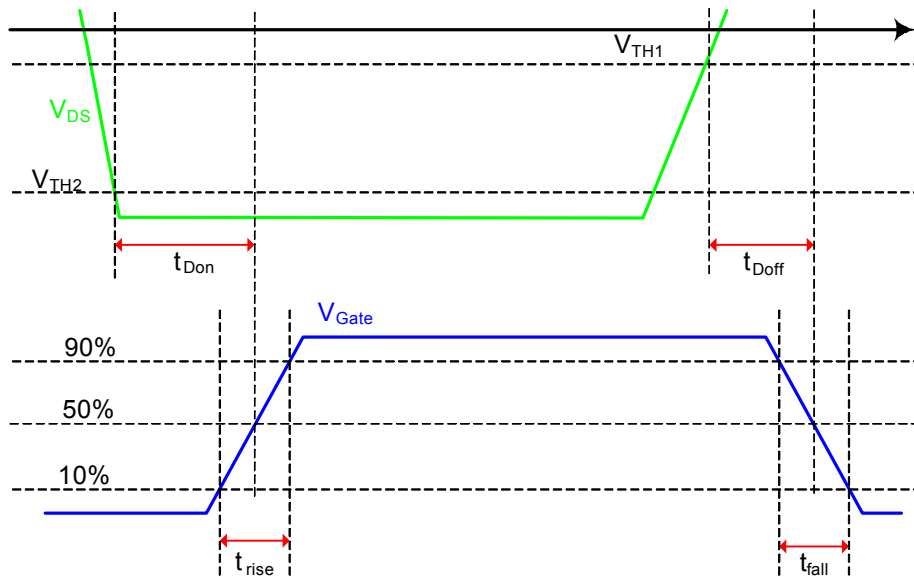


**Fig 14.** Max  $V_{CC}$  Voltage vs. Synchronous Rectifier Switching Freq,  $T_J=125\text{ C}$ ,  $T_{IC} = 85\text{ C}$ , external  $R_G=6\Omega$ ,  $1\Omega$  HEXFET Gate Resistance included

Figures 11-14 shows the maximum allowable  $V_{CC}$  voltage vs. maximum switching frequency for different loads which are calculated using the design methodology discussed in AN1087.

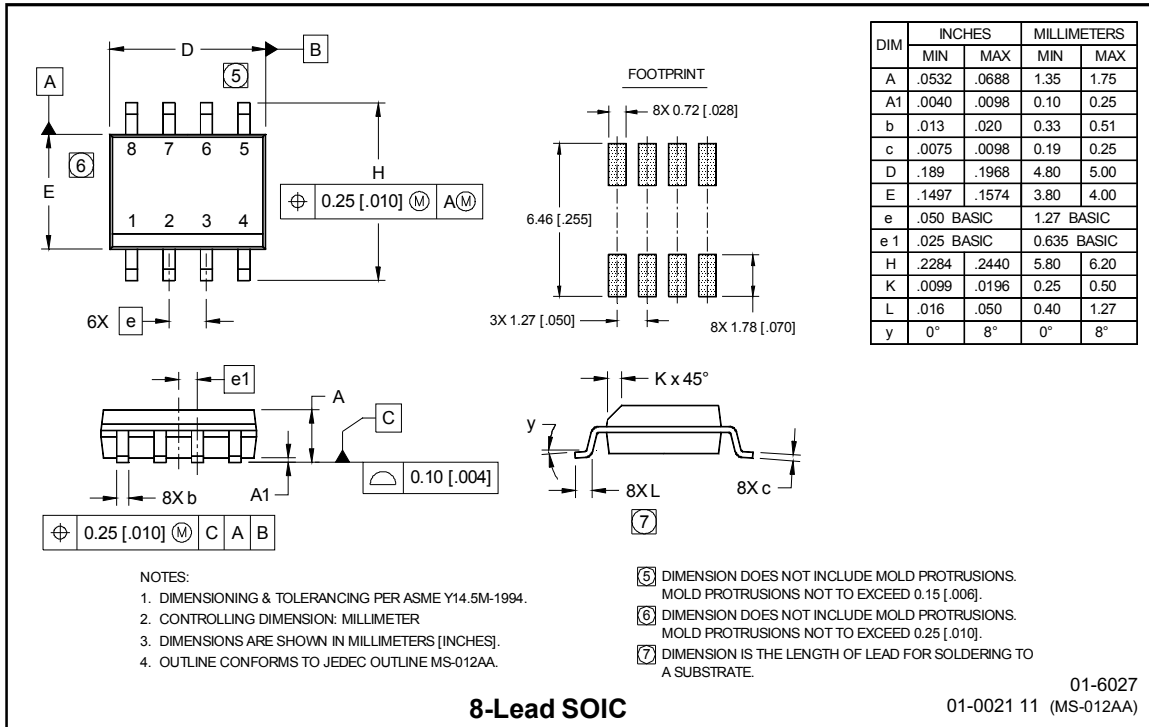


**Fig. 14 - V<sub>CC</sub> Under Voltage Lockout**

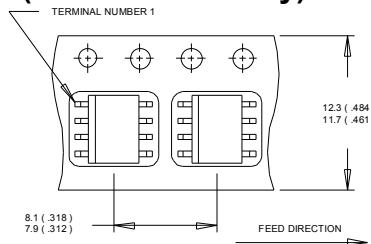


**Fig. 15 - Timing Diagrams**

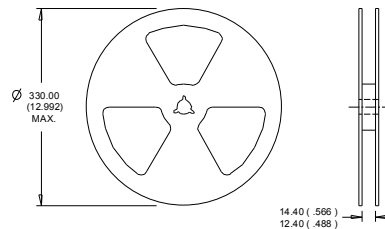
## Case outline



## Tape and Reel Information (SOIC 8-Lead only)

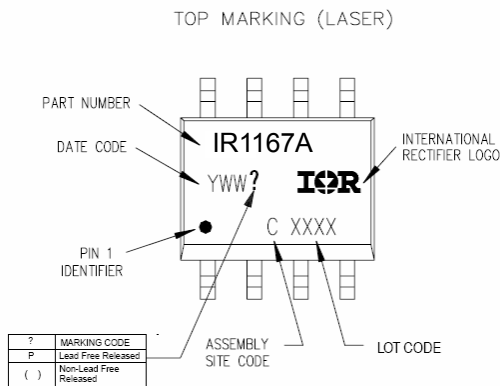


- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

## Part Marking Information



## Order Information

- 8-Lead SOIC IR1167ASPbF
- 8-Lead SOIC IR1167BSPbF
- 8-Lead SOIC Tape and Reel IR1167ASTRPbF
- 8-Lead SOIC Tape and Reel IR1167BSTRPbF

The SOIC-8 is MSL2 qualified  
 This product has been designed and qualified for the Industrial market.  
 Data and specifications subject to change without notice.  
 Qualification Standards can be found at [www.irf.com](http://www.irf.com)

International  
**IR** Rectifier

**WORLD HEADQUARTERS:** 233 Kansas Street, El Segundo, California 90245 Tel: (310) 252-7105  
*Data and specifications subject to change without notice. 1/2009*