

# IR2117

## SINGLE CHANNEL DRIVER

### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input

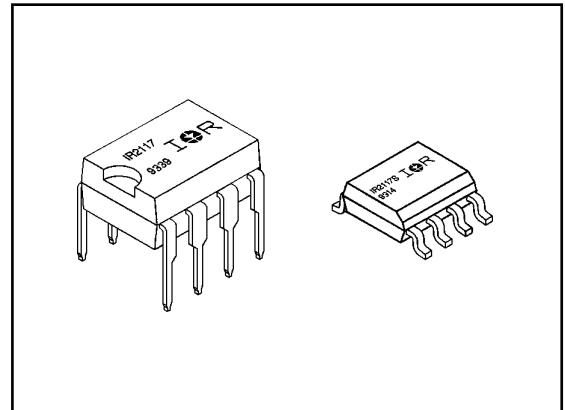
### Product Summary

$V_{\text{OFFSET}}$	600V max.
$I_{\text{O+/-}}$	200 mA / 420 mA
$V_{\text{OUT}}$	10 - 20V
$t_{\text{on/off (typ.)}}$	125 & 105 ns

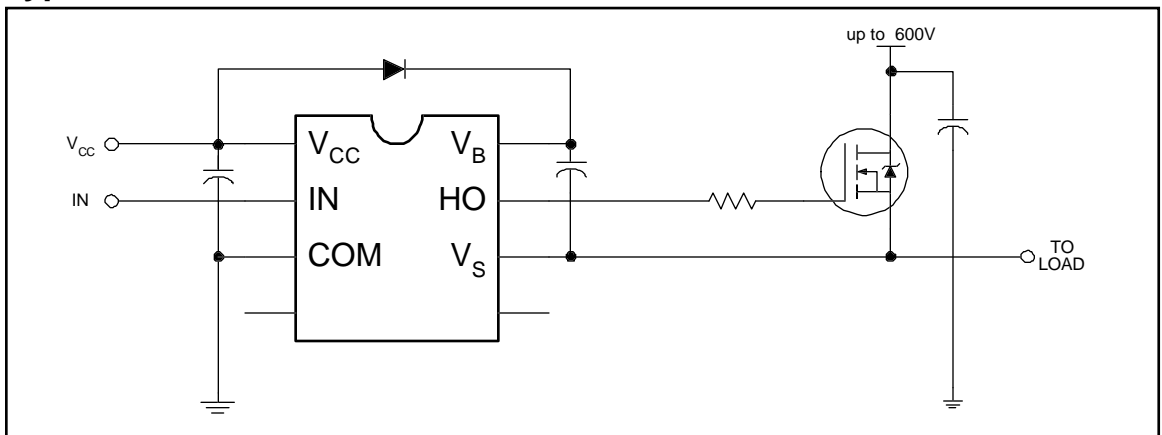
### Description

The IR2117 is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 600 volts.

### Packages



### Typical Connection



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 5 through 8.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Voltage	-0.3	625	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Logic Supply Voltage	-0.3	25	
V <sub>IN</sub>	Logic Input Voltage	-0.3	V <sub>CC</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50	V/ns
P <sub>D</sub>	Package Power Dissipation @ T <sub>A</sub> ≤ +25°C (8 Lead DIP)	—	1.0	W
	(8 Lead SOIC)	—	0.625	
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (8 Lead DIP)	—	125	°C/W
	(8 Lead SOIC)	—	200	
T <sub>J</sub>	Junction Temperature	—	150	°C
T <sub>S</sub>	Storage Temperature	-55	150	
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Value		Units
		Min.	Max.	
V <sub>B</sub>	High Side Floating Supply Absolute Voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High Side Floating Supply Offset Voltage	Note 1	600	
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Logic Supply Voltage	10	20	
V <sub>IN</sub>	Logic Input Voltage	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF and  $T_A$  = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

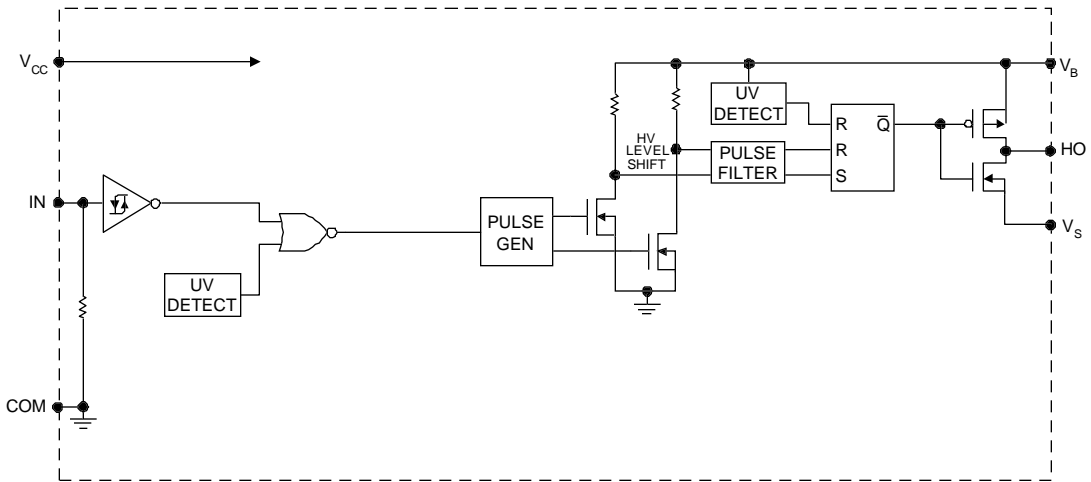
Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{on}$	Turn-On Propagation Delay	—	125	200	ns	$V_S = 0V$
$t_{off}$	Turn-Off Propagation Delay	—	105	180		$V_S = 600V$
$t_r$	Turn-On Rise Time	—	80	130		
$t_f$	Turn-Off Fall Time	—	40	65		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Value			Units	Test Conditions
		Min.	Typ.	Max.		
$V_{IH}$	Logic "1" Input Voltage	6.4	—	—	V	$V_{CC} = 10V$
		9.5	—	—		$V_{CC} = 15V$
		12.6	—	—		$V_{CC} = 20V$
$V_{IL}$	Logic "0" Input Voltage	—	—	3.8		$V_{CC} = 10V$
		—	—	6.0		$V_{CC} = 15V$
		—	—	8.3		$V_{CC} = 20V$
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
$V_{OL}$	Low Level Output Voltage, $V_O$	—	—	100		$I_O = 0A$
$I_{LK}$	Offset Supply Leakage Current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	—	50	240		$V_{IN} = 0V$ or $V_{CC}$
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	70	340		$V_{IN} = 0V$ or $V_{CC}$
$I_{IN+}$	Logic "1" Input Bias Current	—	20	40		$V_{IN} = V_{CC}$
$I_{IN-}$	Logic "0" Input Bias Current	—	—	1.0		$V_{IN} = 0V$
$V_{BSUV+}$	$V_{BS}$ Supply Undervoltage Positive Going Threshold	7.6	8.6	9.6	V	
$V_{BSUV-}$	$V_{BS}$ Supply Undervoltage Negative Going Threshold	7.2	8.2	9.2		
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold	7.6	8.6	9.6		
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	7.2	8.2	9.2		
$I_{O+}$	Output High Short Circuit Pulsed Current	200	250	—	mA	$V_O = 0V, V_{IN} = V_{CC}$ $PW \leq 10 \mu s$
$I_{O-}$	Output Low Short Circuit Pulsed Current	420	500	—		$V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu s$

## Functional Block Diagram



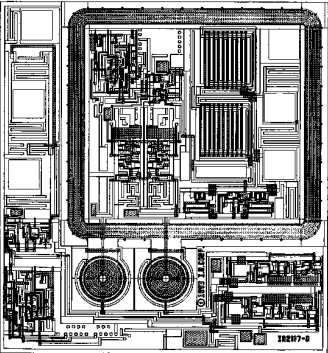
## Lead Definitions

Lead	
Symbol	Description
V <sub>CC</sub>	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO
COM	Logic ground
V <sub>B</sub>	High side floating supply
HO	High side gate drive output
V <sub>S</sub>	High side floating supply return

## Lead Assignments

<p>8 Lead DIP</p> <p><b>IR2117</b></p>	<p>S0-8</p> <p><b>IR2117S</b></p>
<b>Part Number</b>	

## Device Information

Process & Design Rule		HVDCMOS 4.0 $\mu\text{m}$
Transistor Count		114
Die Size		70 X 77 X 26 (mil)
Die Outline		
Thickness of Gate Oxide		800 $\text{\AA}$
Connections	Material	Poly Silicon
	First Layer	Width Spacing Thickness
Second Layer	Material	Al - Si (Si: 1.0% $\pm$ 0.1%)
	Width Spacing Thickness	6 $\mu\text{m}$ 9 $\mu\text{m}$ 20,000 $\text{\AA}$
	Contact Hole Dimension	8 $\mu\text{m}$ X 8 $\mu\text{m}$
Insulation Layer	Material	PSG (SiO <sub>2</sub> )
	Thickness	1.5 $\mu\text{m}$
Passivation	Material	PSG (SiO <sub>2</sub> )
	Thickness	1.5 $\mu\text{m}$
Method of Saw		Full Cut
Method of Die Bond		Ablebond 84 - 1
Wire Bond	Method	Thermo Sonic
	Material	Au (1.0 mil / 1.3 mil)
Leadframe	Material	Cu
	Die Area	Ag
	Lead Plating	Pb : Sn (37 : 63)
Package	Types	8 Lead PDIP / SO-8
	Materials	EME6300 / MP150 / MP190
Remarks:		

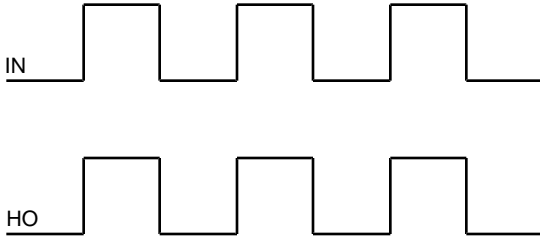


Figure 1. Input/Output Timing Diagram

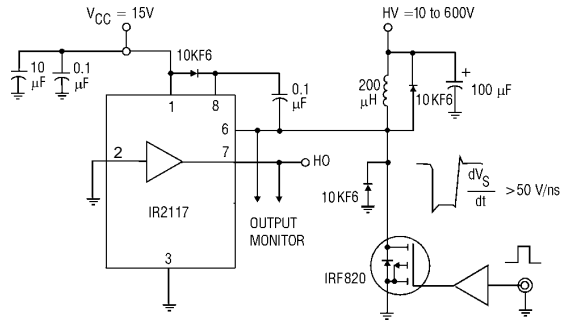


Figure 2. Floating Supply Voltage Transient Test Circuit

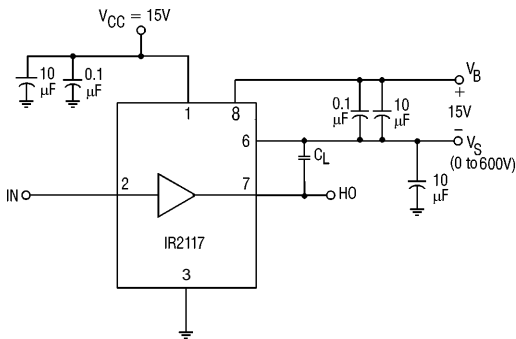


Figure 3. Switching Time Test Circuit

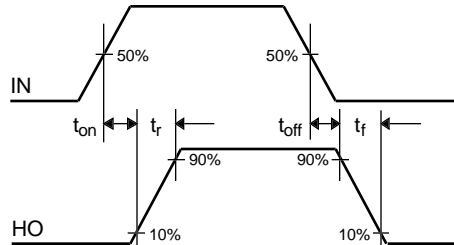
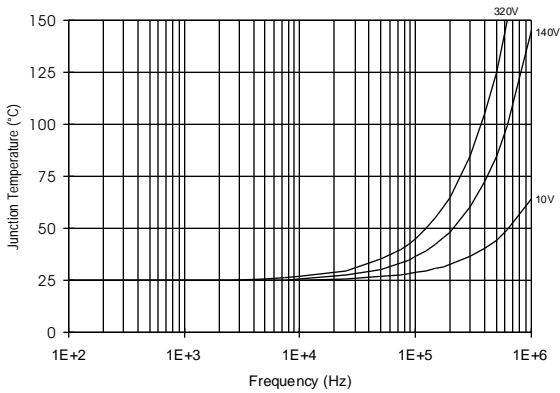
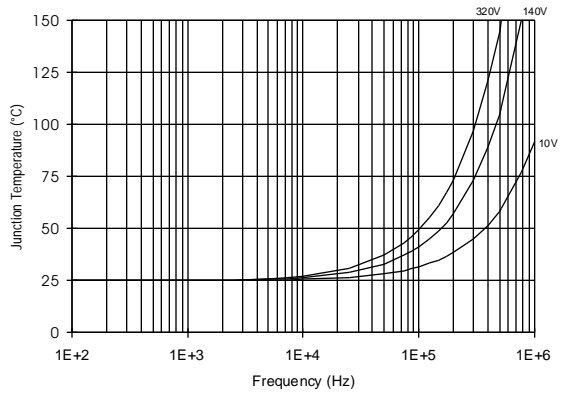


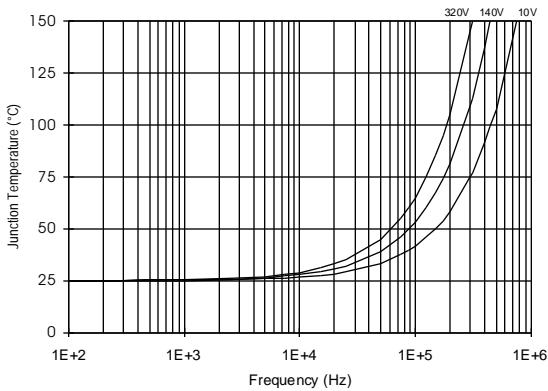
Figure 4. Switching Time Waveform Definition



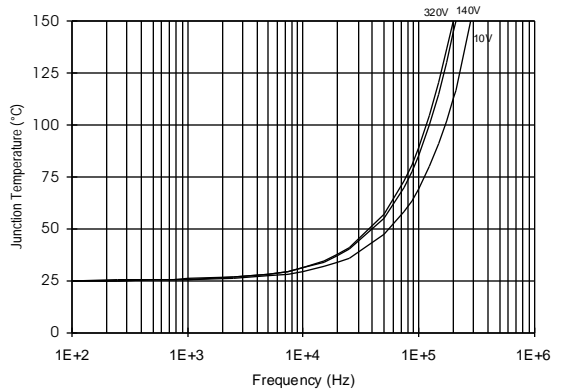
**Figure 5. IR2117 T<sub>J</sub> vs. Frequency (IRFBC20)**  
**R<sub>GATE</sub> = 33Ω, V<sub>CC</sub> = 15V**



**Figure 6. IR2117 T<sub>J</sub> vs. Frequency (IRFBC30)**  
**R<sub>GATE</sub> = 22Ω, V<sub>CC</sub> = 15V**



**Figure 7. IR2117 T<sub>J</sub> vs. Frequency (IRFBC40)**  
**R<sub>GATE</sub> = 15Ω, V<sub>CC</sub> = 15V**



**Figure 8. IR2117 T<sub>J</sub> vs. Frequency (IRFPE50)**  
**R<sub>GATE</sub> = 10Ω, V<sub>CC</sub> = 15V**

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