# IRU3037 / IRU3037A

## 8-PIN SYNCHRONOUS PWM CONTROLLER

## FEATURES

- Synchronous Controller in 8-Pin Package
- Operation from 4V to 25V Input
- Single 5V Supply Operation
- Internal 200KHz Oscillator (400KHz for IRU3037A)
- Soft-Start Function
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability

## APPLICATIONS

- DDR memory source sink Vtt application
- Low cost on-board DC to DC such as 5V to 3.3V, 2.5V or 1.8V
- Graphic Card
- Hard Disk Drive

## DESCRIPTION

The IRU3037 controller IC is designed to provide a low cost synchronous Buck regulator for on-board DC to DC converter applications. With the migration of today's ASIC products requiring low supply voltages such as 1.8V and lower, together with currents in excess of 3A, traditional linear regulators are simply too lossy to be used when input supply is 5V or even in some cases with 3.3V input supply. The IRU3037 together with dual N channel MOSFETs such as IRF7313, provide a low cost solution for such applications. This device features an internal 200KHz oscillator (400KHz for "A" version), under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

## TYPICAL APPLICATION

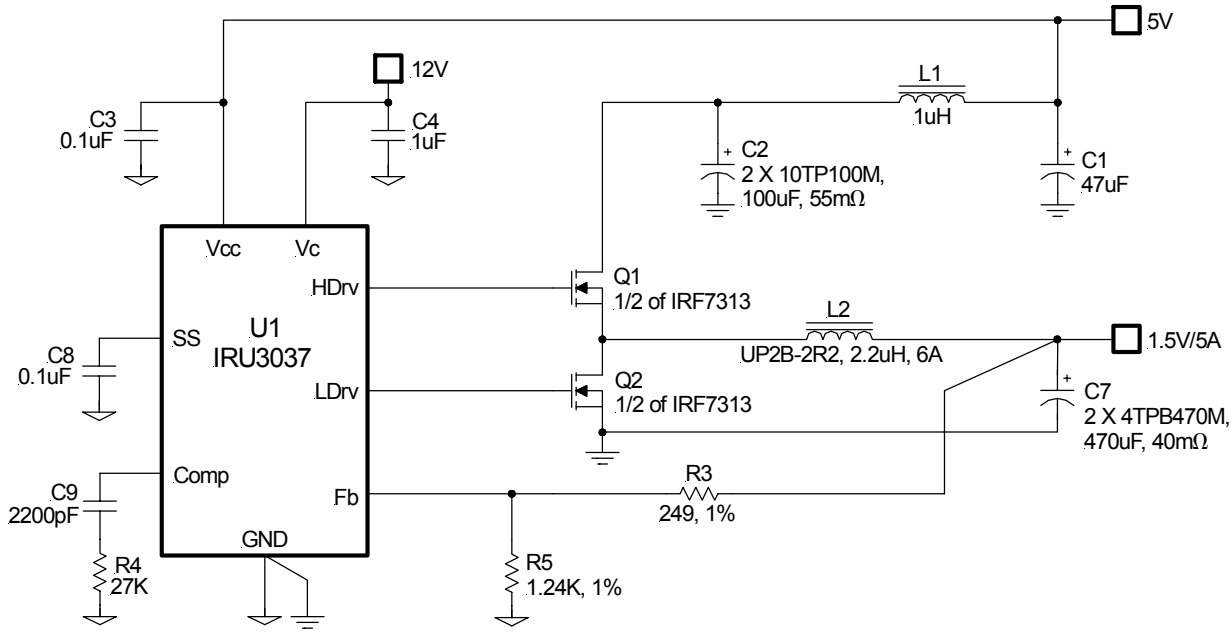



Figure 1 - Typical application of IRU3037 or IRU3037A.

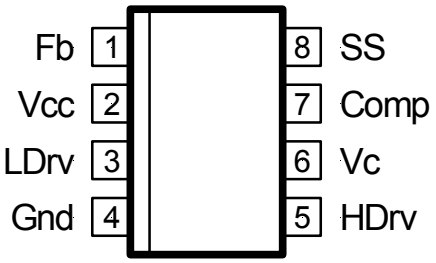
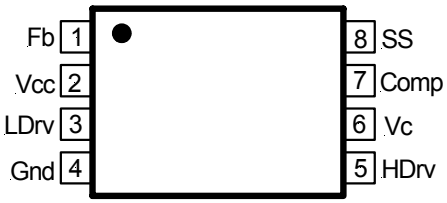
## PACKAGE ORDER INFORMATION

| $T_A$ (°C) | DEVICE | PACKAGE | FREQUENCY |
|---|---|---|---|
| 0 To 70 | IRU3037CS | 8-Pin Plastic SOIC | 200KHz |
| 0 To 70 | IRU3037CF | 8-Pin Plastic TSSOP | 200KHz |
| 0 To 70 | IRU3037ACS | 8-Pin Plastic SOIC | 400KHz |
| 0 To 70 | IRU3037ACF | 8-Pin Plastic TSSOP | 400KHz |

## ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage ..... 30V
Vc Supply Voltage ..... 30V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

## PACKAGE INFORMATION

| 8-PIN WIDE BODY PLASTIC SOIC (S) | 8-PIN WIDE BODY PLASTIC TSSOP (F) |
|---|---|
| TOP VIEW<br>  <br><br>$\theta_{JA}$=160°C/W | TOP VIEW<br>  <br><br>$\theta_{JA}$=124°C/W |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, Vc=12V and $T_A$=0 to 70°C. Typical values refer to $T_A$=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Reference Voltage** | | | | | | |
| Fb Voltage | $V_{FB}$ | IRU3037 | 1.225 | 1.250 | 1.275 | |
| | | IRU3037A | 0.784 | 0.800 | 0.816 | V |
| Fb Voltage Line Regulation | $L_{REG}$ | 5<Vcc<12 | | 0.2 | 0.35 | % |
| **UVLO** | | | | | | |
| UVLO Threshold - Vcc | UVLO Vcc | Supply Ramping Up | | 4.2 | | V |
| UVLO Hysteresis - Vcc | | | | 0.25 | | V |
| UVLO Threshold - Vc | UVLO Vc | Supply Ramping Up | | 3.3 | | V |
| UVLO Hysteresis - Vc | | | | 0.2 | | V |
| UVLO Threshold - Fb | UVLO Fb | Fb Ramping Down (IRU3037) | | 0.6 | | V |
| | | (IRU3037A) | | 0.4 | | |
| UVLO Hysteresis - Fb | | | | 0.1 | | V |
| **Supply Current** | | | | | | |
| Vcc Dynamic Supply Current | Dyn Icc | Freq=200KHz, $C_L$=1500pF | | 5 | | mA |
| Vc Dynamic Supply Current | Dyn Ic | Freq=200KHz, $C_L$=1500pF | | 7 | | mA |
| Vcc Static Supply Current | $I_{CCQ}$ | SS=0V | 1 | 3.3 | 6 | mA |
| Vc Static Supply Current | $I_{CQ}$ | SS=0V | 0.5 | 1 | 4.5 | mA |
| **Soft-Start Section** | | | | | | |
| Charge Current | SSIB | SS=0V | 10 | 20 | 35 | µA |

| PARAMETER | SYM | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Error Amp** | | | | | | |
| Fb Voltage Input Bias Current | $I_{FB1}$ | SS=3V, Fb=1V | | -0.1 | | µA |
| Fb Voltage Input Bias Current | $I_{FB2}$ | SS=0V, Fb=1V | | -64 | | µA |
| Transconductance | GM | | | 500 | | umho |
| **Oscillator** | | | | | | |
| Frequency | Freq | IRU3037 | 180 | 200 | 220 | KHz |
| | | IRU3037A | 360 | 400 | 440 | |
| **Output Drivers** | | | | | | |
| Rise Time | Tr | $C_L$=1500pF | | 50 | 100 | ns |
| Fall Time | Tf | $C_L$=1500pF | | 50 | 100 | ns |
| Dead Band Time | $T_{DB}$ | | 50 | 250 | | ns |
| Max Duty Cycle | Ton | Fb=1V, Freq=200KHz | 85 | 90 | | % |
| Min Duty Cycle | Toff | Fb=1.5V | 0 | | | % |

# PIN DESCRIPTIONS

| PIN# | PIN SYMBOL | PIN DESCRIPTION |
|---|---|---|
| 1 | Fb | This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier. |
| 2 | Vcc | This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability. |
| 3 | LDrv | Output driver for the synchronous power MOSFET. |
| 4 | Gnd | This pin serves as the ground pin and must be connected directly to the ground plane. A high frequency capacitor (0.1 to 1µF) must be connected from V5 and V12 pins to this pin for noise free operation. |
| 5 | HDrv | Output driver for the high side power MOSFET. |
| 6 | Vc | This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability. |
| 7 | Comp | Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation. |
| 8 | SS | This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. |

## BLOCK DIAGRAM

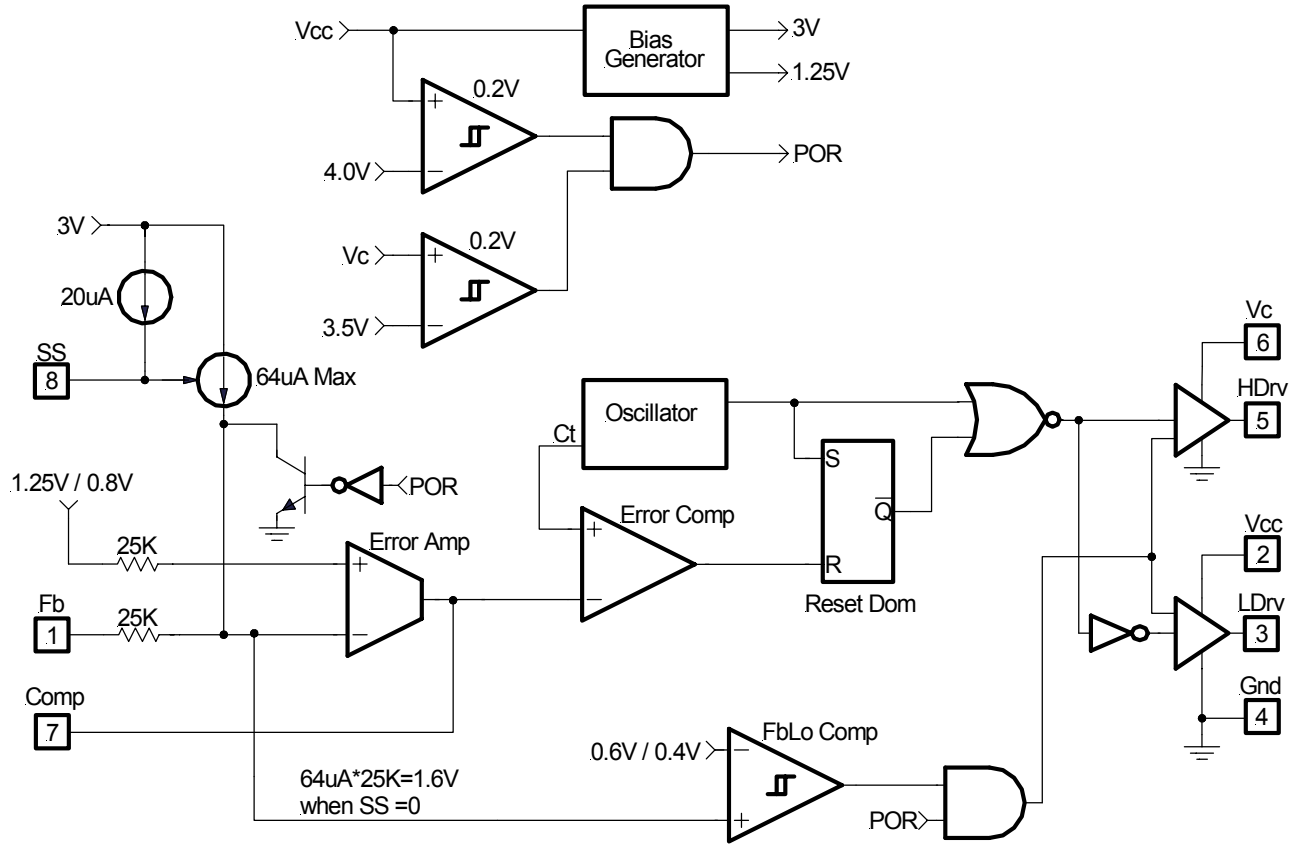



Figure 2 - Simplified block diagram of the IRU3037.

## THEORY OF OPERATION

**Introduction**

The IRU3037 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an error amplifier, an internal oscillator, a PWM comparator, 0.5A peak gate driver, soft-start and shutdown circuits (See the block diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the reference voltage.

This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor to set the oscillation frequency to 200 KHz (400 KHz for “A” version).

**Soft-Start**

The IRU3037 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.3V and 4.2V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A’s output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

**Short-Circuit Protection**

The outputs are protected against the short-circuit. The IRU3037 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The IRU3037 shuts down the PWM signals, when the output voltage drops below 0.6V (0.4V for IRU3037A).

**Under-Voltage Lockout**
The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc and Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

# APPLICATION INFORMATION

**Design Example:**
The following example is a demo-board application for IRU3037, the schematic is figure 8 on page 10.

$V_{IN}$ = 5V
$V_{OUT}$ = 3.3V
$I_{OUT}$ = 4A
$\Delta V_{OUT}$ = 100mV
$f_S$ = 200KHz

**Output Voltage Programming**
Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 1.25V (0.8V for IRU3037A). The divider is ratioed to provide 1.25V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_6}{R_5}\right) \qquad (1)$$

When an external resistor divider is connected to the output as shown in Figure 3.

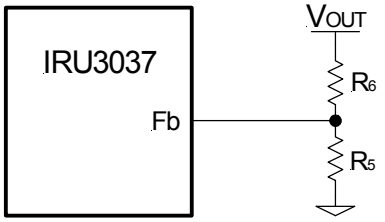



Figure 3 - Typical application of the IRU3037 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Choose $R_5$ = 1KΩ will result to:
$R_6$ = 1.64KΩ

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

**Soft-Start Programming**
The soft-start timing can be programmed by selecting the soft start capacitance value. The start up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad (2)$$

Where:
$C_{SS}$ is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

**Boost Supply Vc**
To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 8. The capacitor is charged up to twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications. In application, when a separate voltage source is available the boost circuit can be avoided as shown in figure 1.

**Input Capacitor Selection**
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power-up. The IRU3037 provides the soft-start function which controls and limits the current surge. The value of the input capacitor can be calculated by the following formula:

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V} \qquad (3)$$

Where:
$C_{IN}$ is the input capacitance (μF)
$I_{IN}$ is the input current (A)
Δt is the turn on time of the high-side switch (μs)
ΔV is the allowable peak to peak voltage ripple (V)

Assuming the following:

$\Delta V = 1\%(V_{IN})$, Efficiency($\eta$) = 90%

$$\Delta t = D \times \frac{1}{f_S} \quad \rightarrow \quad \Delta t = 3.3\mu s$$

$$I_{IN} = \frac{V_O \times I_O}{\eta \times V_{IN}} \quad \rightarrow \quad I_{IN} = 2.93A$$

By using equation (3), $C_{IN} = 193.3\mu F$
Choose two 100$\mu$F tantalum capacitors.

The Sanyo TPB series PosCap capacitor 100$\mu$F, 10V with 55m$\Omega$ ESR is a good choice.

**Output Capacitor Selection**

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \qquad (4)$$

Where:
$\Delta V_O$ = Output Voltage Ripple
$\Delta I_O$ = Output Current
$\Delta V_O$=100mV and $\Delta I_O$=4A, result to ESR=25m$\Omega$

The Sanyo TPC series, PosCap capacitor is a good choice. The 6TPC150M 150$\mu$F, 6.3V has an ESR 40m$\Omega$. Selecting two of these capacitors in parallel, results to an ESR of $\cong$ 20m$\Omega$ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

**Inductor Selection**

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor ($\Delta$i); the optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad (5)$$

Where:
$V_{IN}$ = Maximum Input Voltage
$V_{OUT}$ = Output Voltage
$\Delta$i = Inductor Ripple Current
$f_S$ = Switching Frequency
$\Delta t$ = Turn On Time
D = Duty Cycle

If $\Delta i = 20\%(I_O)$, then the output inductor will be:

$L = 7\mu H$

The Toko D124C series provides a range of inductors in different values, low profile suitable for large currents, 10$\mu$H, 4.2A is a good choice for this application. This will result to a ripple approximately 14% of output current.

**Power MOSFET Selection**

The IRU3037 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage ($V_{DSS}$), gate-source drive voltage ($V_{GS}$), maximum output current, On-resistance $R_{DS}$(on) and thermal management.

The MOSFET must have a maximum operating voltage ($V_{DSS}$) exceeding the maximum input voltage ($V_{IN}$).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low $V_{GS}$ to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND} \text{ (Upper Switch)} = I^2_{LOAD} \times R_{DS}(on) \times D \times \vartheta$$

$$P_{COND} \text{ (Lower Switch)} = I^2_{LOAD} \times R_{DS}(on) \times (1 - D) \times \vartheta$$

$\vartheta = R_{DS}$(on) Temperature Dependency

The $R_{DS}$(on) temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, IRF7301 is a good choice. The device provides low on-resistance in a compact SOIC 8-Pin package.

The IRF7301 has the following data:

$V_{DSS}$ = 20V
$I_D$ = 5.2A
$R_{DS}(on)$ = 0.05Ω

The total conduction losses will be:

$P_{CON}(Total) = P_{CON}(Upper\ Switch)\vartheta + P_{CON}(Lower\ Switch)\vartheta$

$P_{CON}(total) = I^2_{LOAD} \times R_{DS}(on) \times \vartheta$

$\vartheta$ = 1.5 according to the IRF7301 data sheet for 150°C junction temperature

$P_{CON}(total)$ = 1.2W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS}(off)}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad (7)$$

Where:
$V_{DS}$(off) = Drain to Source Voltage at off time
$t_r$ = Rise Time
$t_f$ = Fall Time
T = Switching Period
$I_{LOAD}$ = Load Current

The switching time waveform is shown in figure 4.

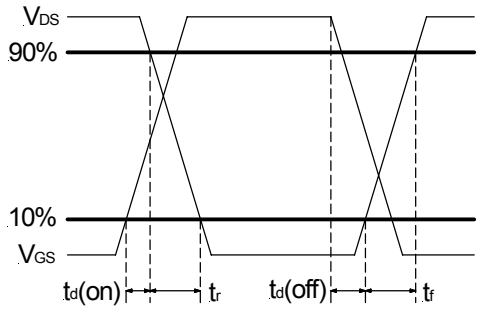



Figure 4 - Switching time waveforms.

From IRF7301 data sheet we obtain:

$t_r$ = 42ns
$t_f$ = 51ns

These values are taken under a certain condition test. For more detail please refer to the IRF7301 data sheet.

By using equation (7), we can calculate the switching losses.

$P_{SW}$ = 0.186W

**Feedback Compensation**

The IRU3037 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (See figure 5). The Resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2\pi\sqrt{Lo \times Co}} \qquad (8)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

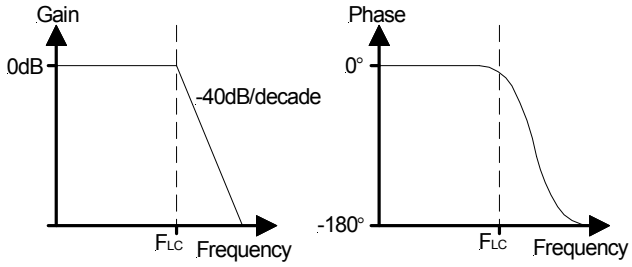



Figure 5 - Gain and phase of LC filter.

The IRU3037's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 6.

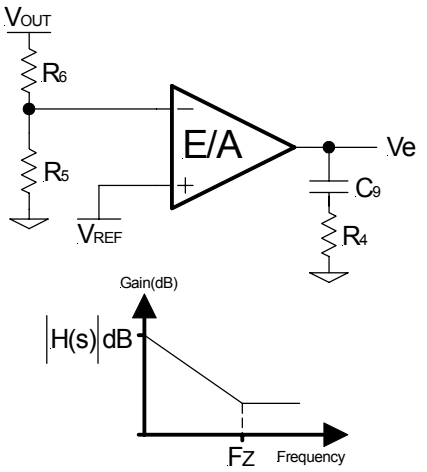



Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / $V_{OUT}$) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + SR_4C_9}{SC_9} \qquad (9)$$

The (s) indicates that the transformer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \qquad (10)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad (11)$$

The gain is determined by the voltage divider and E/A's transconductance.

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z \cong 75\%F_{LC} \qquad (12)$$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}}$$

For:
$L_O = 10\mu H$
$C_O = 300\mu F$
$F_Z = 2.17KHz$

Choosing $C_9$=2200pF and using equation (12) to calculate $R_4$, we get: $R_4$=33KΩ

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the LC filter expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad (13)$$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in figure 7.

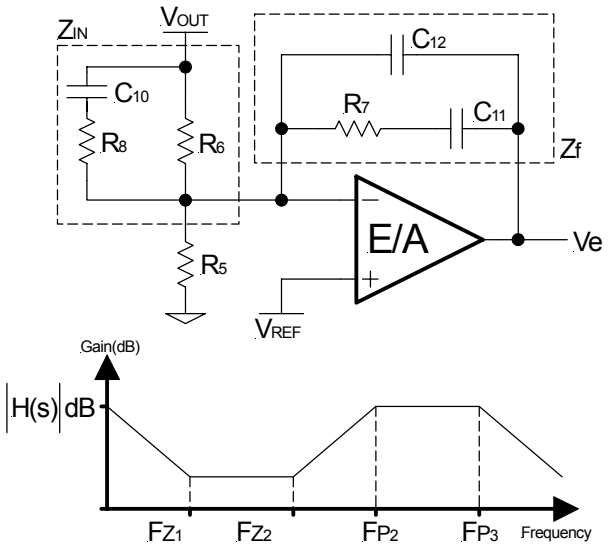



Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transformer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_mZ_f}{1 + g_mZ_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$g_mZ_f >> 1$ and $g_mZ_{IN} >> 1$

By replacing $Z_{IN}$ and $Z_f$ according to figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{SR_6(C_{12}+C_{11})} \times \frac{(1+SR_7C_{11}) \times [1+SC_{10}(R_6+R_8)]}{\left[1+SR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+SR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefor, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12} + C_{11}}\right)}$$

$$F_{P3} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)}$$

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules:

1) Set $R_6$ for desired crossover frequency.

2) Choose $R_5$ to set the output voltage. (See Equation 1)

3) Place first zero before LC's resonant frequency pole. ($F_{Z1} \cong 75\%\ F_{LC}$)

4) Place second zero around the resonant frequency. ($F_{Z2} = F_{LC}$)

5) Place second pole at ESR zero. ($F_{P2} = F_{ESR}$)

6) Place third pole at the half the switching frequency. ($F_{P3} = 1/2\ F_S$)

These design rules will give a crossover frequency approximately one-tenth of the switching frequency (~20KHz). The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

**Layout Consideration**

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

Figure 8 shows a suggested layout for the critical components, based on the schematic on page 10.

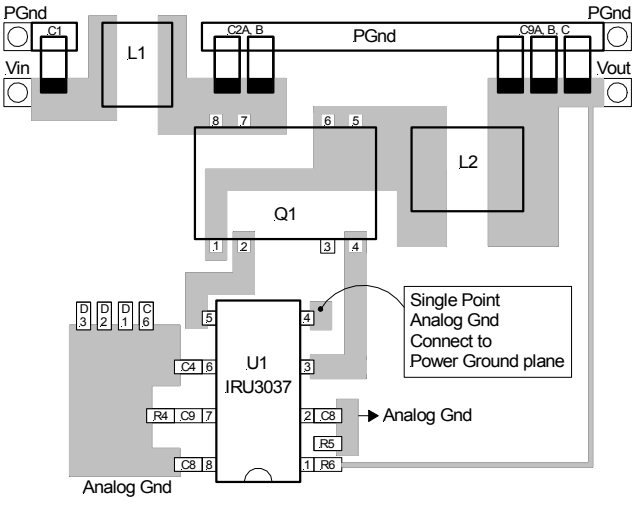
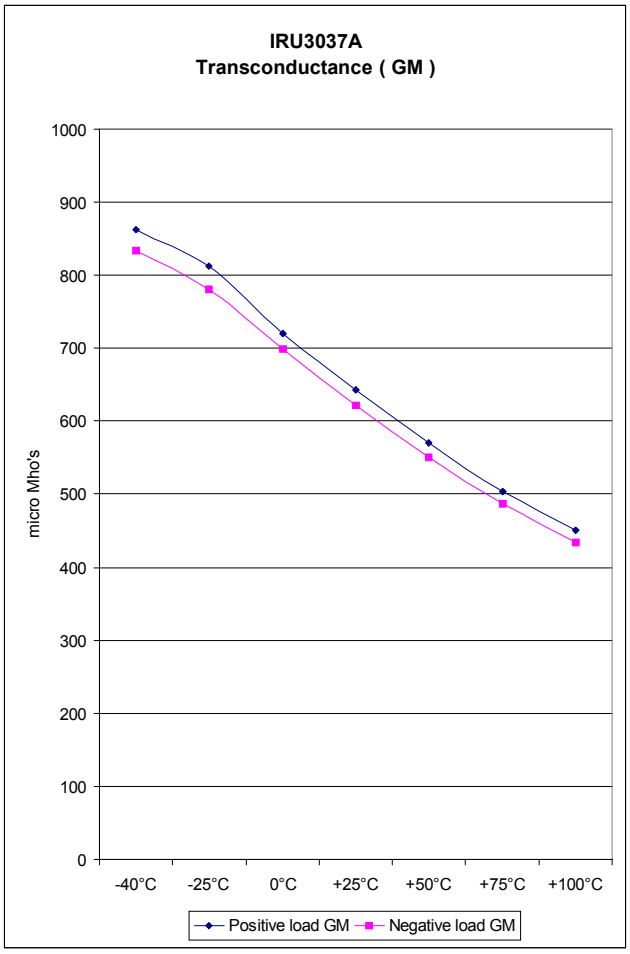
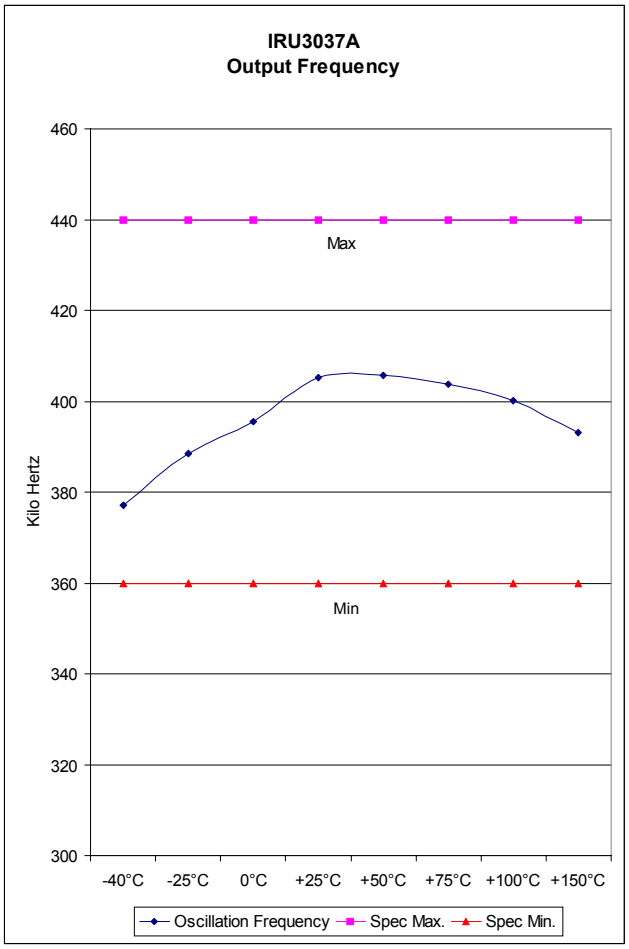



Figure 8 - Suggested layout.
(Topside shown only)

## TEMPERATURE CHARACTERISTICS

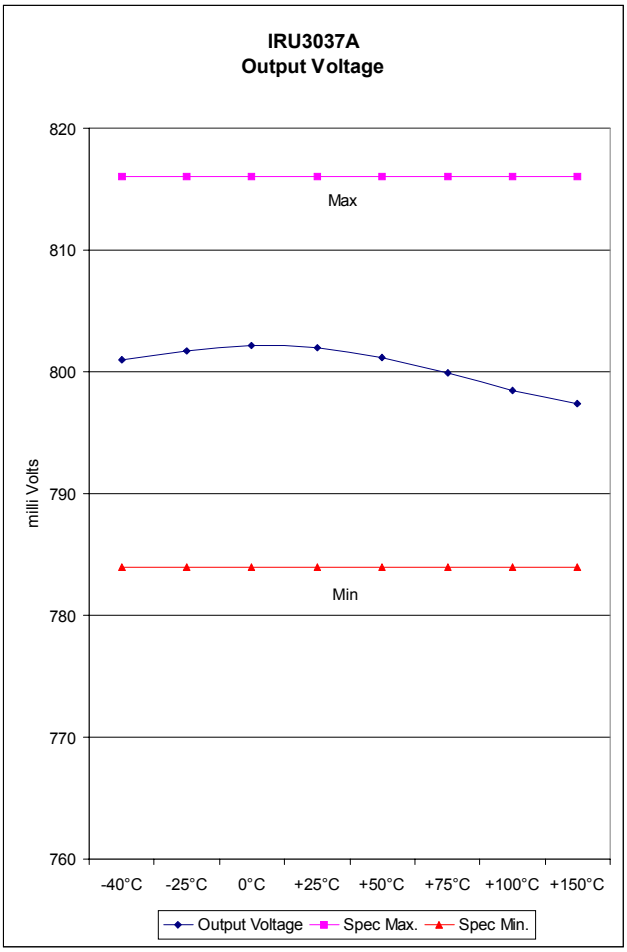



Graph 1

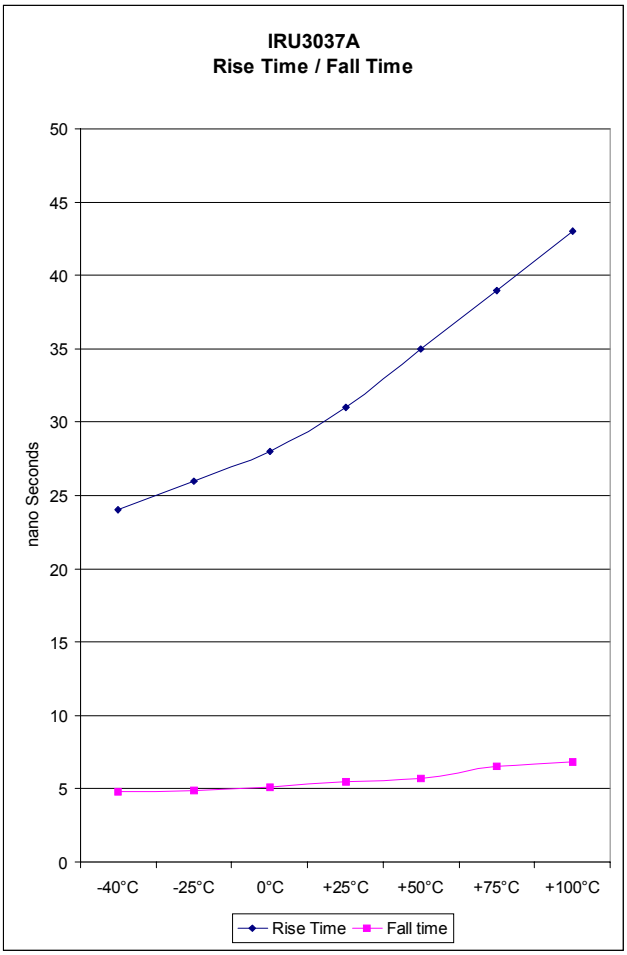



Graph 2

# TEMPERATURE CHARACTERISTICS




Graph 3




Graph 4

# TYPICAL APPLICATION

**Single Supply 5V Input**

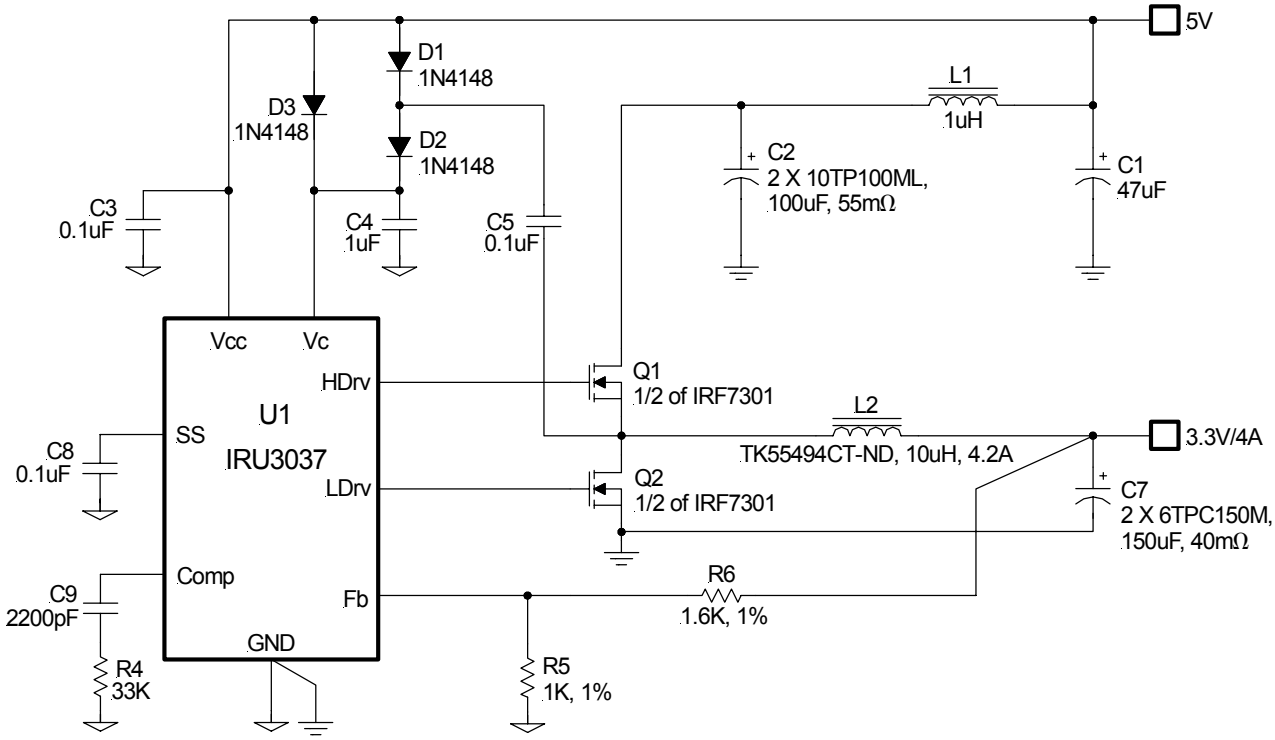



Figure 9 - Typical application of IRU3037 or IRU3037A in an on-board DC-DC converter using a single 5V supply.

# TYPICAL APPLICATION

**Dual Supply, 5V Bus and 12V Bias Input**

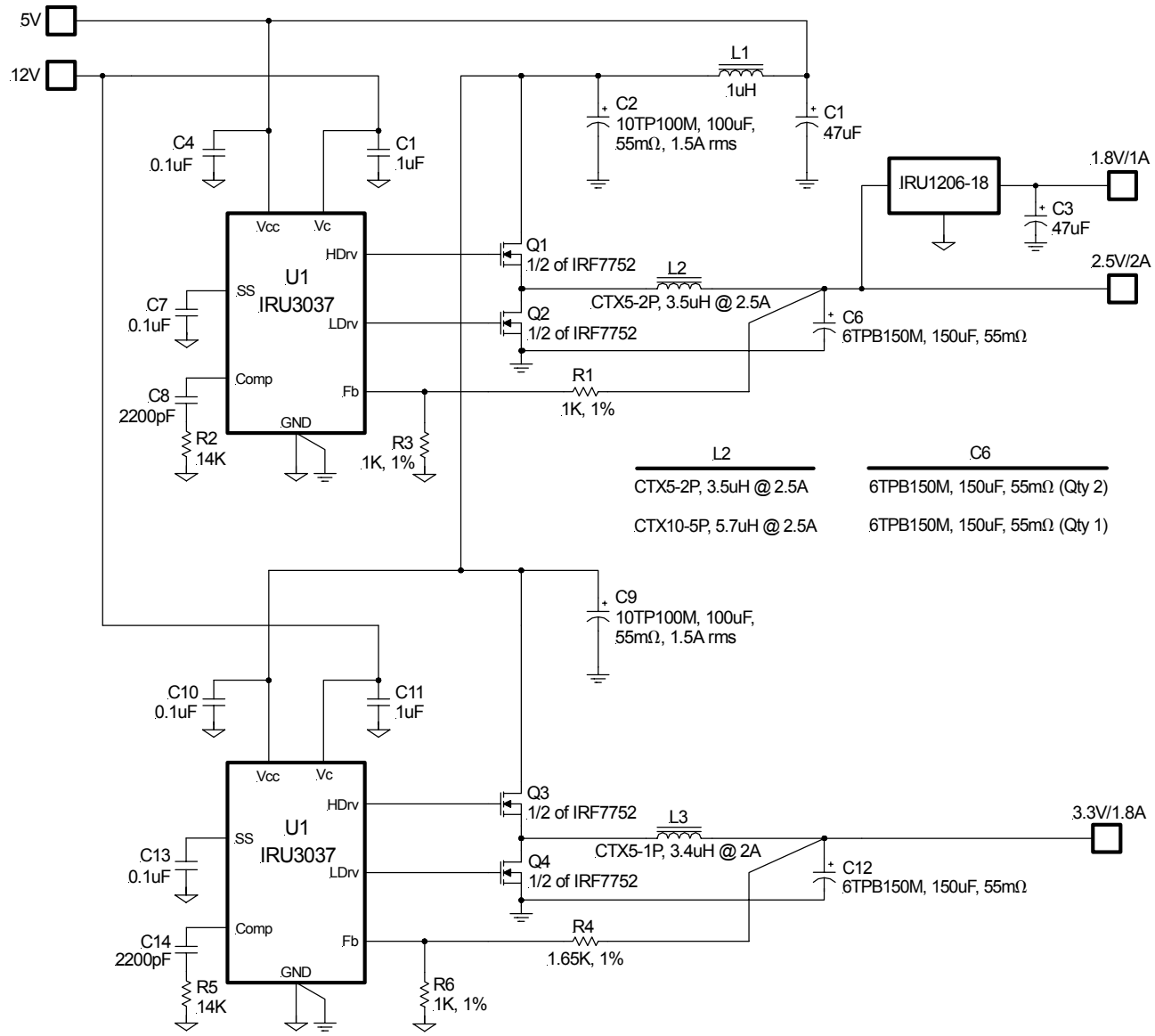



Figure 10 - Typical application of IRU3037 or IRU3037A in an on-board DC-DC converter providing the Core, GTL+, and Clock supplies for the Pentium II microprocessor.

## TYPICAL APPLICATION

**1.8V to 7.5V / 0.5A Boost Converter**

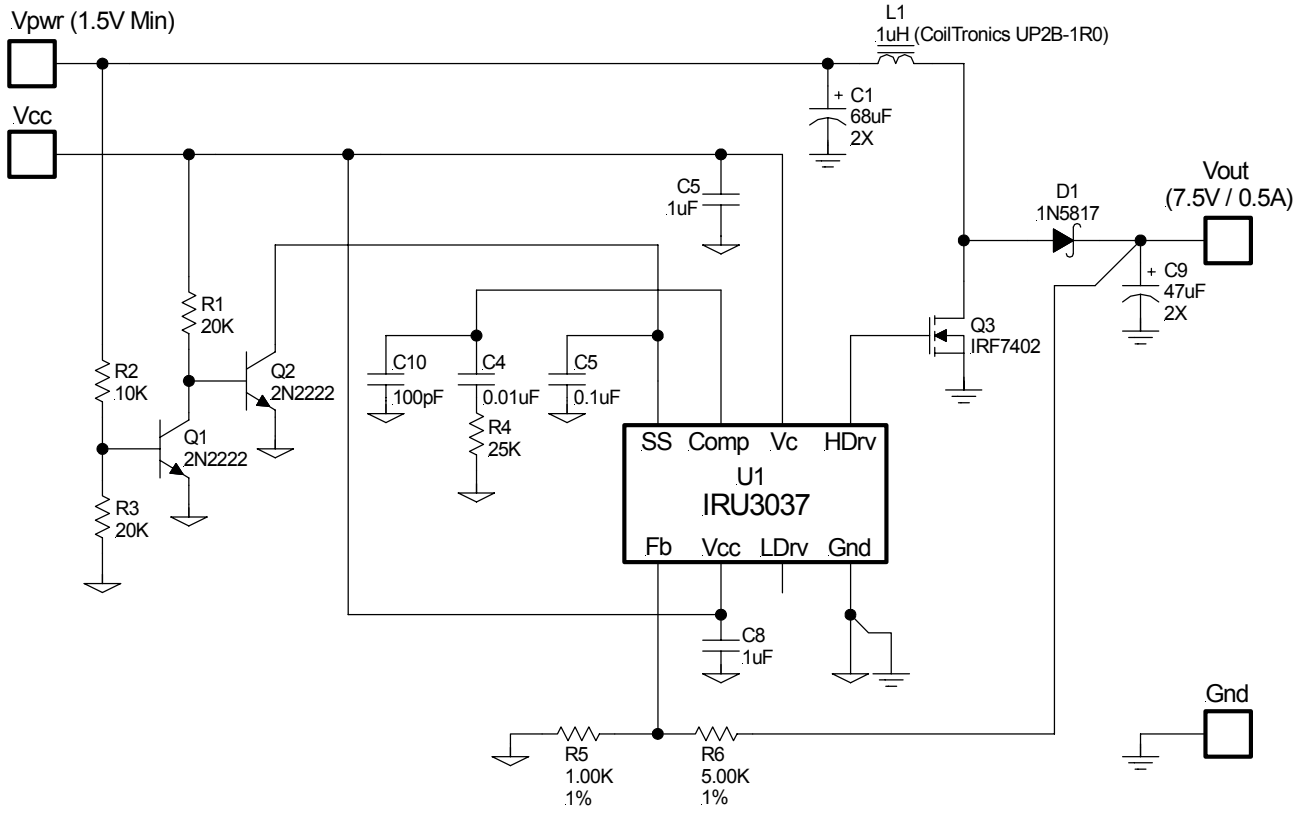



Figure 11 - Typical application of IRU3037 or IRU3037A.

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