8K×8 Bit CMOS EEPROM

FEATURES

- **Simple Byte Write**
  - **Single TTL Level Write Signal**
  - **Latched Address and Data**
  - **Automatic Internal Erase-before-Write**
  - **Automatic Write Timing**
  - **$\overline{\text{DATA}}$ Polling and Verification**
  - **Ready/$\overline{\text{Busy}}$ Output Pin (KM28C65)**
- **32-byte page write: 5ms max**
  - **Effective 150μS/byte write**
- **Enhanced Write Protection**
- **Single 5 volt Supply**
- **Fast Access Time: 150ns**
- **Power: 100 μA — Standby (max)**
  30 mA — Operating (max)
- **Two Line Control-Eliminates Bus Contention**
- **10,000 Cycle Endurance**
- **JEDEC Byte-wide Memory Pinout**

GENERAL DESCRIPTION

The KM28C64/C65 is a 65,536 bit electrically erasable and programable Read-Only-Memory. Its data can be modified using simple TTL level signals and a single 5 volt power supply.

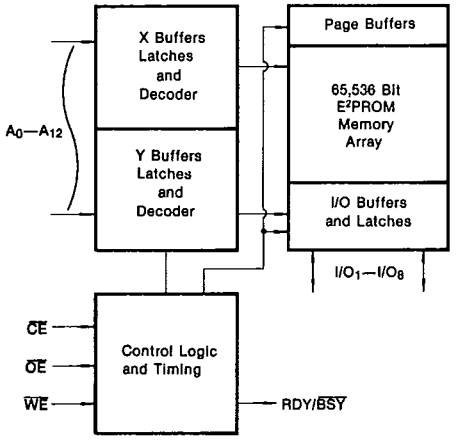
Writing data into the KM28C64/C65 is very simple. The internally self-timed write cycle latches both address and data to provide a free system bus during the 5ms (max) write period.

A 32-byte page write enables an entire chip written in 1.3 second.

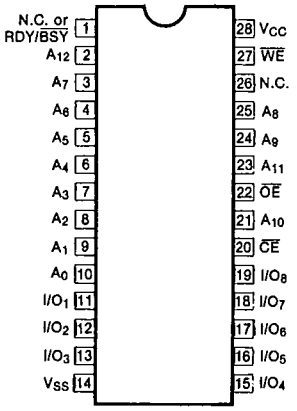
The KM28C64/C65 features $\overline{\text{DATA}}$-polling, which enables the EEPROM to signal the processor that a write operation is complete without requiring the use of any external hardware. Ready/$\overline{\text{Busy}}$ is a hardware scheme in which Pin 1 is used to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM28C64/C65 is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A_0—A_{12}	Address Inputs
I/O_1—I/O_8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RDY/$\overline{BSY}$	Ready/$\overline{Busy}$ Output
N.C.	No Connection
V_{CC}	+5V
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Units
Voltage on any Pin Relative to V_{SS}	V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	T_{bias}	−10 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Short Circuit Output Current	I_{os}	5	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, $T_A = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage, Inputs	V_{IH}	2.0	—	$V_{CC}+0.3$	V
Input Low Voltage, all Inputs	V_{IL}	−0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Operating Current	I_{CC}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ all I/O's = open all addresses* (NOTE 1)		30	mA
Standby Current (TTL)	I_{SB1}	$\overline{CE} = V_{IH}$ all I/O's = open		1	mA
Standby Current (CMOS)	I_{SB2}	$\overline{CE} = V_{CC} - 0.2V$ all I/O's = open		100	μA
Input Leakage Current	I_{LI}	$V_{IN} = 0$ to V_{CC}		10	μA
Output Leakage Current	I_{LO}	$V_{In} = 0$ to V_{CC}		10	μA
Output High Voltage Level	V_{OH}	$I_{OH} = -400\mu A$	2.4		V
Output Low Voltage Level	V_{OL}	$I_{OL} = 2.1mA$		0.4	V
Write Inhibit V_{CC} Level	V_{WL}		3.5		V

* Note 1. All addresses toggling from V_{IL} to V_{IH} at 5MHz

CAPACITANCE ($T_A = 25°C$, $V_{CC} = 5V$, f = 1.0 MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	8	pF
Input Capacitance	C_{IN}	$V_{IN} = 0V$	—	8	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby & Write Inhibit	High-Z	Standby
L	L	H	$\overline{\text{Data}}$-Polling	$I/O_6 = \overline{D_6}$	Active
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

AC CHARACTERISTICS

($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted.)

TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100$ pF

READ CYCLE

Parameter	Symbol	KM28C64-15 KM28C65-15		KM28C64-20 KM28C65-20		KM28C64-25 KM28C65-25		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		ns
Chip Enable Access Time	t_{CE}		150		200		250	ns
Address Access Time	t_{AA}		150		200		250	
Output Enable Access Time	t_{OE}		60		80		100	ns
Chip Enable to Output in Low-Z	t_{LZ}	0		0		0		ns
Chip Disable to Output in High-Z	t_{HZ}	5	50	5	70	5	90	ns
Output Enable to Output in Low-Z	t_{OLZ}	5		5		5		ns
Output Disable to Output in High-Z	t_{OHZ}	5	50	5	70	5	90	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

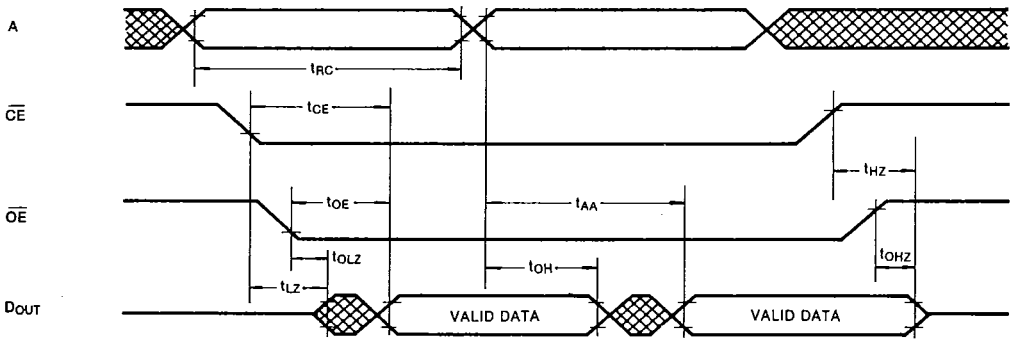
WRITE CYCLE

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{WC}	5		ms
Address Set-Up Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	80		ns
Write Set-Up Time	t_{CS}	0		ns
Write Hold Time	t_{CH}	0		ns
Chip Enable to End of Write Input	t_{CW}	100		ns
Output Enable Set-Up Time	t_{OES}	10		ns
Output Enable Hold Time	t_{OEH}	10		ns
Write Pulse Width	t_{WP}	100		ns
Data Set-Up Time	t_{DS}	50		ns
Data Hold Time	t_{DH}	10		ns
Time to Device Busy	t_{DB}		100	ns
Busy to Write Recovery Time	t_{BWR}	50		ns
Byte Load Cycle	t_{BLC}	0.2|	30	μs

Note: The timer for t_{BLC} is reset at a falling edge of $\overline{WE}$ and start at a rising edge of $\overline{WE}$.

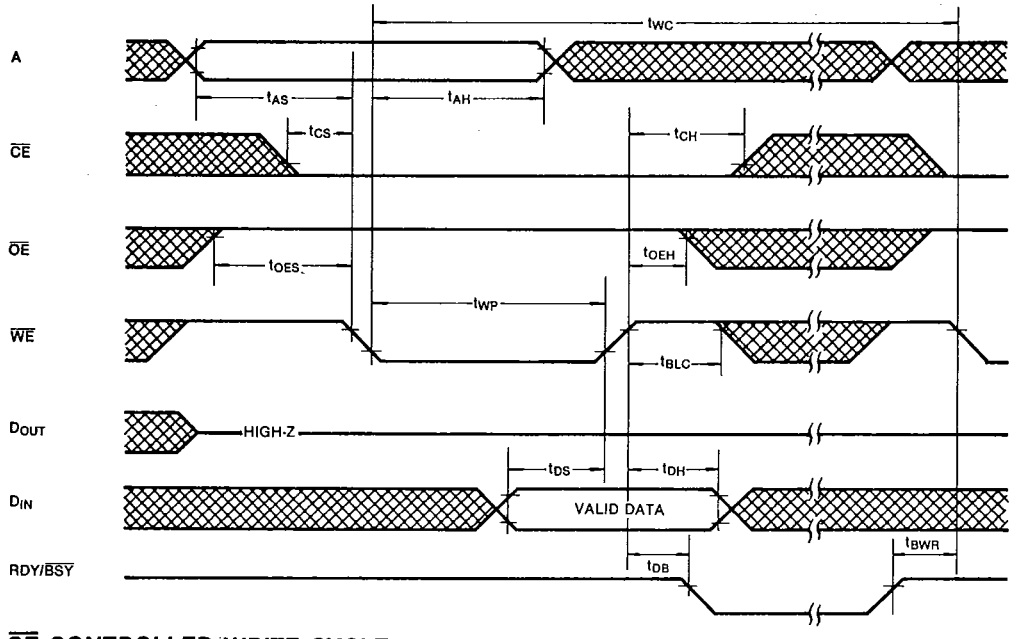
TIMING DIAGRAMS

READ CYCLE $\overline{WE} = V_{IH}$

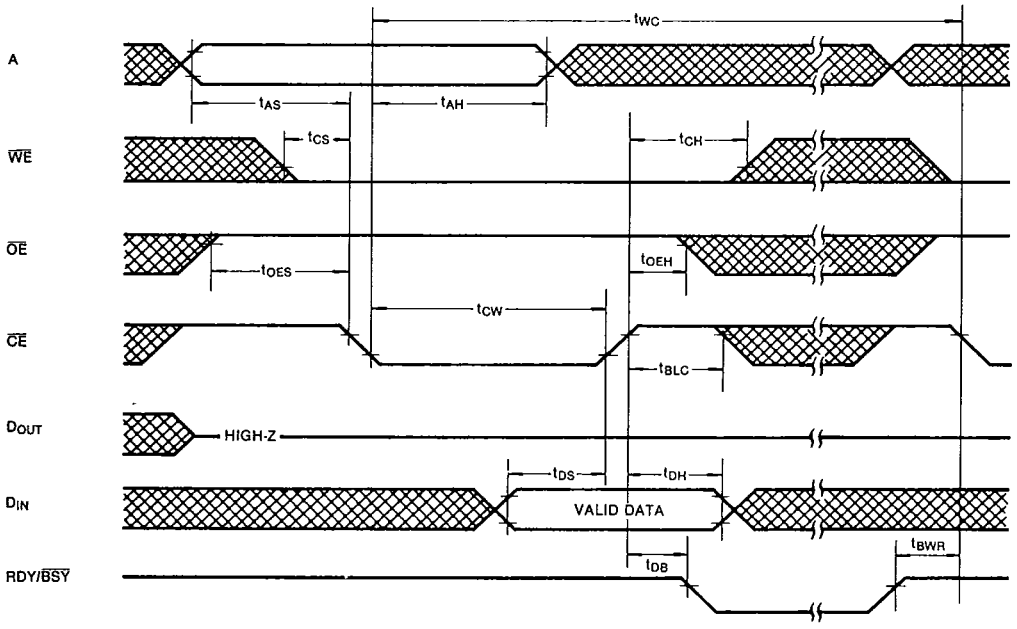


TIMING DIAGRAMS (Continued)

$\overline{WE}$ CONTROLLED WRITE CYCLE

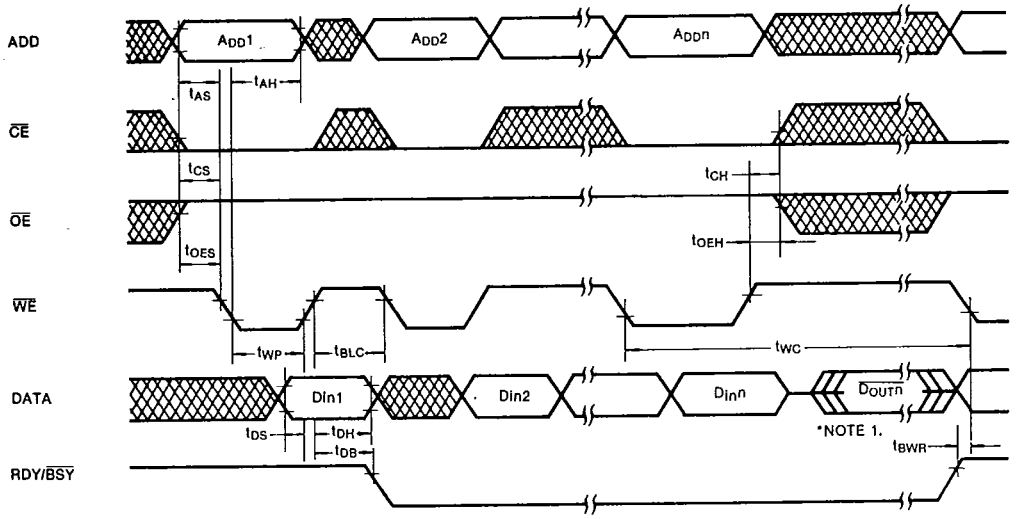


$\overline{CE}$ CONTROLLED WRITE CYCLE

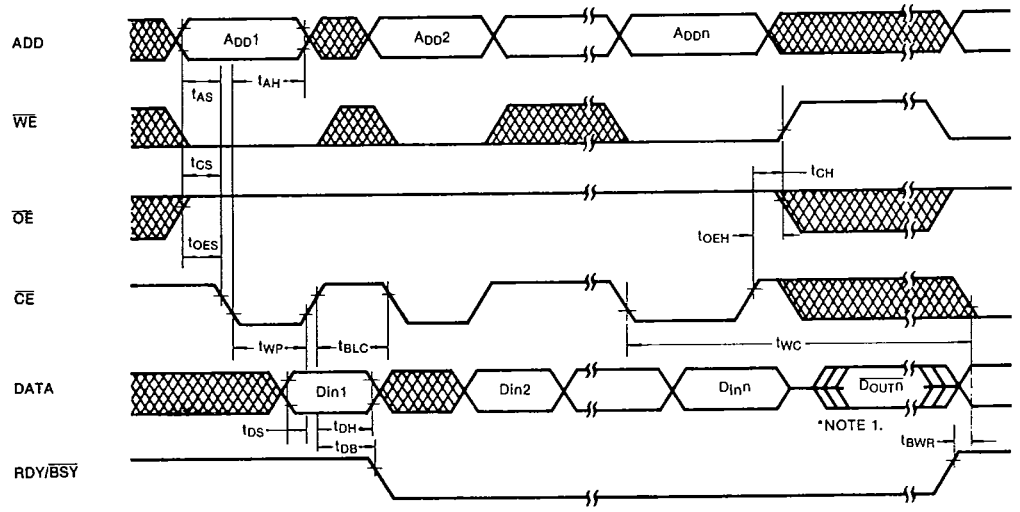


TIMING DIAGRAMS (Continued)

PAGE MODE WRITE ($\overline{WE}$ CONTROLLED WRITE CYCLE)



PAGE MODE WRITE ($\overline{CE}$ CONTROLLED WRITE CYCLE)



*Note 1. Tristate for I/O_1-I/O_7, $\overline{D_{out}}^n$ for I/O_8 if the chip is read (see $\overline{Data}$-polling)

DEVICE OPERATION

Read

Reading data from the KM28C64/C65 is similar to reading data from a SRAM. A read cycle occurs when $\overline{WE}$ is high and $\overline{CE}$ and $\overline{OE}$ are low. If either $\overline{CE}$ or $\overline{OE}$ goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The Data I/O pins are in the high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is high.

Write

Writing data into the KM28C64/C65 is very easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator and fully self-timed control logic make writing as easy as writing to a SRAM.

**** BYTE WRITE MODE ****

The byte write mode of the KM28C64/C65 is only a part of the page write mode. A single byte data loading followed by a t_{BLC} time out and by a write cycle will complete a byte mode write. In this mode, the write is exactly identical to that of the KM2864A/65A.

**** PAGE WRITE MODE ****

The KM28C64/C65 allows up to 32 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 32 bytes data are loaded into the KM28C64/C65 internal registers and a write period, in which the loaded datas in the registers are written to the EEPROM cells of the selected page.

Data are loaded into the KM28C64/C65 by sequentially pulsing $\overline{WE}$ with $\overline{CE}$ LOW and $\overline{OE}$ HIGH. On each $\overline{WE}$, address is latched on the falling edge of the $\overline{WE}$ and data is latched on the rising edge of the $\overline{WE}$. The data can be loaded in any "Y" address order and can be renewed in the data loading period.

Since the timer for the data loading period (t_{BLC}) is reset at the falling edge of $\overline{WE}$ and starts at every rising edge of $\overline{WE}$, the only requirement on $\overline{WE}$ to continue the data loading is that the interval between $\overline{WE}$ pulses does not exceed the maximum t_{BLC} (30μs). If $\overline{OE}$ goes LOW during the data loading period, further attempt to load the data will be ignored because the external $\overline{WE}$ signal is blocked by $\overline{OE}$ signal internally. Consequently, the t_{BLC} timer is not reset by the external $\overline{WE}$ pulse if $\overline{OE}$ is LOW.

The page address for the write is the "X" address (A5-A12) latched on the last $\overline{WE}$. The write period consists of an erase cycle followed by a program cycle. During the erase cycle the existing data of the locations being addressed are erased. The new data latched at the registers are written into the locations during the program cycle. Note that only the addressed locations in a page are rewritten during a page write cycle.

The KM28C64/C65 also supports $\overline{CE}$ controlled write cycle. That means $\overline{CE}$ can be used to latch address and data as well as $\overline{WE}$.

Standby

Power consumption may be reduced to less than 100μA by deselecting the device with a high input on $\overline{CE}$. Whenever $\overline{CE}$ is high, the device is in the standby mode and I/O_1-I/O_8 are in the high impedance state, regardless of the state of $\overline{OE}$ or $\overline{WE}$.

Data Protection

Features have been designed into the KM28C64/C65 that prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64/C65 has an protection feature against $\overline{WE}$ noises, a $\overline{WE}$ noise having width shorter than 20ns (typ.) will not start any unwanted write cycle.

Write cycles are also inhibited when V_{CC} is less than V_{WI} = 3.5 volts, the Write Inhibits V_{CC} level.

During power-up, the KM28C64/C65 automatically prevents any write operation for a period of 5ms (max.) after V_{CC} reaches the V_{WI} level. This will provide the system with sufficient time to bring $\overline{WE}$ and $\overline{CE}$ to a high level before a write can occur. Read cycles can be executed during this initialization period.

Holding either $\overline{OE}$ low or $\overline{WE}$ high or $\overline{CE}$ high during power-On and power-Off will inhibit inadvertent writes.

$\overline{\text{Data}}$ Polling

The KM28C64/C65 features $\overline{DATA}$-Polling at I/O_8 to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. Reading the device at any time during a write operation will produce, at I/O_8 an inverted value of Last data loaded into the EEPROM (I/O_1-I/O_7 are at the high impedance state). True data will be produced at I/O_8 once the write cycle has been completed.

Ready/$\overline{\text{Busy}}$

The KM28C65 has a Ready/$\overline{Busy}$ output on pin 1 that indicates when the write cycle is complete. The pin is normally high except when a write cycle is in progress, In which case the pin is low.

DEVICE OPERATION (Continued)

The Read/$\overline{Busy}$ output is configured as open-drain driver there-by allowing two or more Ready/$\overline{Busy}$ output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value maybe calculated as follows

$$R_P = \frac{V_{CC}(max) - V_{OL}(max)}{I_{OL} + I_L} = \frac{5.1V}{2.1mA + I_L}$$

where I_L is the sum of the input currents of all devices tied to the Ready/Busy pin.

Endurance and Data Retention

The KM28C64/C65 is designed for applications requiring up to 10,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 10,000 times without degrading device operation and that the data in the byte will remain valid after its last write operation for ten years with or without power applied.

PACKAGE DIMENSIONS

28 LEAD PLASTIC DUAL IN LINE PACKAGE