MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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M29F800A3
M29F800A2

8M CMOS Flash Memory

- **Organization:** 524,288 words x 16 bits
  1,048,576 words x 8 bits
- **Power Supply Voltage:** V_{CC} = 3.3 V ± 0.3 V
- **Access Time:** M29F800A3–80 = 80 ns (Max)
  M29F800A3–10 = 100 ns (Max)
  M29F800A3–12 = 120 ns (Max)
- **Power Consumption:**

Read	7 mA (Typ)
Program/Erase	40 mA (Typ)
Standby (CMOS)	1 µA (Typ)
Deep Power Down Mode	3.3 µA (Typ)

- **Auto Program:**

Program Time	7.5 ms (Typ)
Program Unit	128 Word (256 Byte)

- **Auto Erase:**

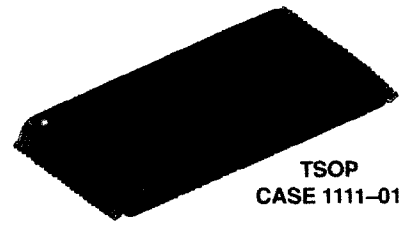
Erase Time	50 ms (Typ)
Erase Unit:	
Boot Block	8K Word/16 Kbyte x 1
Parameter Block	4K Word/8 Kbyte x 2
	16K Word/32 Kbyte x 1
Main Block	32K Word/64 Kbyte x 15

- **Other Functions:**
  Software Command Control
  Selective Block Lock
  Erase Suspend/Resume
  Program Suspend/Resume
  Status Register Read
  Sleep Mode
- **Packages:**
  48–Pin 12mm x 20mm TSOP (Type–I)
  48–Pin 12mm x 20mm TSOP Reverse
- **Program Erase Cycle:**
  10,000 Times/Min (– 40°C – 85°C)
  100,000 Times/Min (0 °C – 70 °C)
- **Boot Block**

M29F800A3U	Top Boot Block
M29F800A3B	Bottom Boot Block

The M29F800A3 is a 3.3 V high speed 8,388,608–bit CMOS Boot Block Flash Memory suitable for use in systems such as mobile, personal computing, and communication products.

The M29F800A3 is organized as 524,288 words x 16 bits and 1,048,576 words x 8 bits, fabricated using CMOS technology for the peripheral circuits and DiNOR (Divided bit line NOR) architecture for the memory cells. It is available in a 48–pin TSOP(I), 48–pin TSOP reverse. This device is available in either top or bottom Boot Block.



TSOP
CASE 1111–01

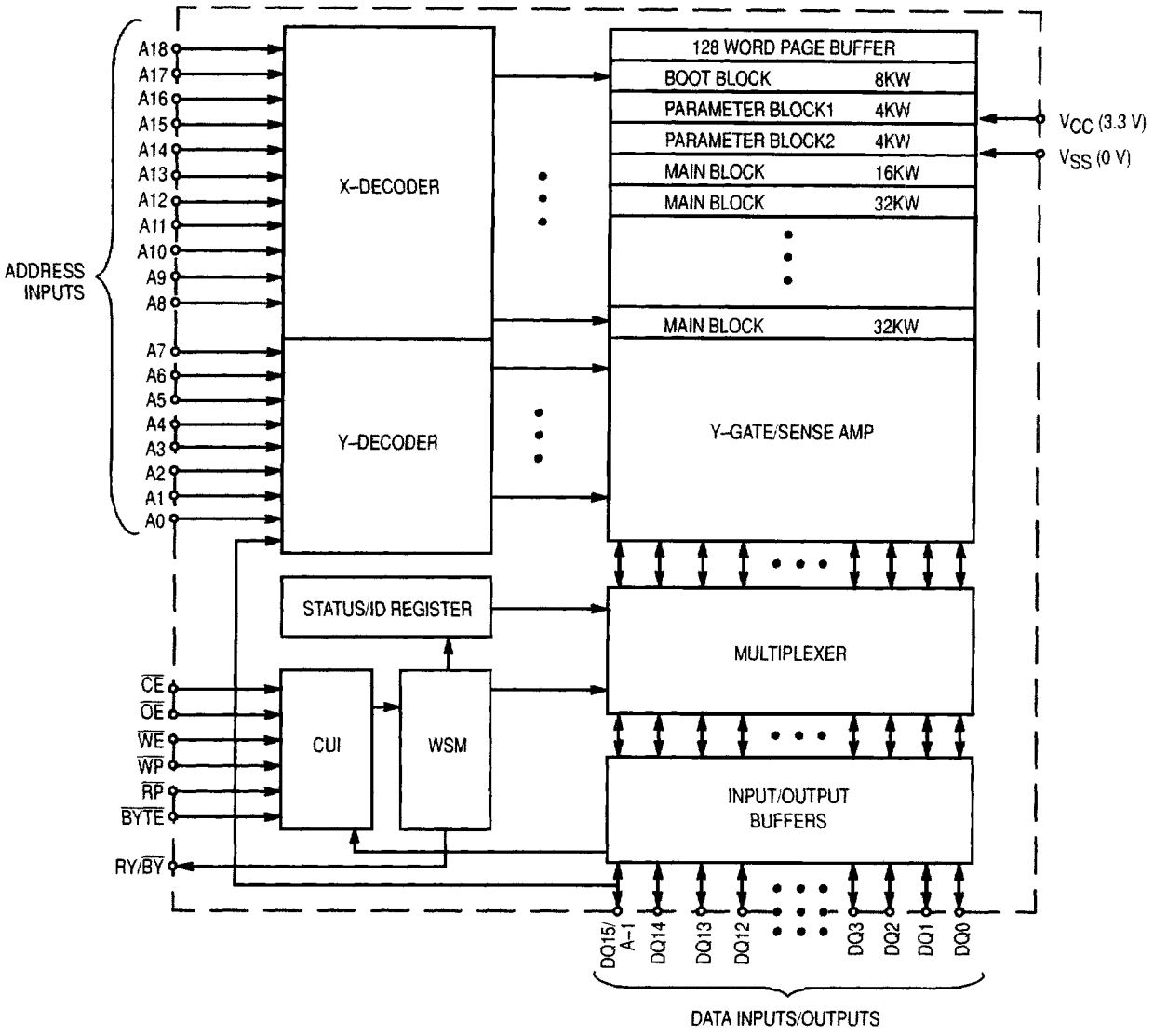
TSOP REVERSE
CASE 1111A–01

NOTOSD77

IMPORTANT NOTE: Please consult Specification Update Document M29F800A3ER/D for errata, specification clarifications, and documentation changes pertaining to this data sheet.

REV 4
10/7/97

BLOCK DIAGRAM



APPLICATION INFORMATION

Motorola's family of 8 Mb high-integration flash devices combine hardware read-while-write (M28F800A2, M28F800A1 devices only), fast access, highspeed page programming, and ultra low power with three flash architectures into one form factor (a main code array, a parameter storage array, and a boot block array). These features and others make this family of flash memories ideal for systems requiring low chip count, high performance, and low power, such as portable embedded applications.

The 8 Mb high-integration flash memory family by Motorola is an optimal non-volatile memory solution for applications, such as digital cellular phones, PDA's, pagers, and many other hand held communications and computing devices. These space/power constrained applications require a high performance, low power non-volatile memory subsystem for both main processor code execution as well as high speed parameter storage. Motorola's M29F800Ax family provides a low voltage, high performance solution for systems in which code is either executed directly from the flash (XIP – execute in place) or merely stored in flash before being downloaded into DRAM upon boot–up (SDL – store and download). This includes, but is not exclusive to, wireless and wired infrastructure applications, such as base stations, routers, hubs, and switches. These applications, although not necessarily power constrained, tend to value performance. As more desktop applications, such as PCs, migrate from 5 V to 3 V the M29F800Ax is designed to deliver 80 ns access times across the full industrial temperature range (– 40 to 85 °C).

In many of today's portable embedded applications, the system spends a vast majority of its time awaiting user instructions, such as phone numbers, while in standby mode. The flash memory in many of these applications accounts for a significant proportion of the total power consumed while in standby mode wasting precious battery life. Motorola's M29F800Ax high-integration flash memory allows battery life to be significantly extended by drawing less than 5 µA (CMOS) while in standby mode and less than 25 mA while in read mode.

As more functionality is incorporated into today's portable communication and computing devices (such as paging, faxing, etc.), the performance demand on the flash memory sub-system becomes greater. Motorola's 8Mb high-integration flash memories feature access times as low as 80 ns at 3.0 V and 90 ns at 1.8 V. This reduces processor wait-states allowing room to grow in performance and therefore higher integration of functionality in the system.

KEY FEATURES

The M29F800Ax supports a feature set optimized for the needs of today's small form-factor, low power, high performance designs. Program and erase suspend functions are included allowing the user to suspend a program or erase operation in order to service an interrupt by reading main processor code. This allows flexibility when storing parameter data that may be read later. After issuing a program or erase suspend to service a read function, the user may resume the program/erase operation within a cycle time.

In order to enable maximum write throughput performance when performing factory programming, the M29F800Ax supports page-programming on all blocks. This allows main processor code to be programmed in quickly, saving time and money in the manufacturing line.

The M29F800Ax features Address Transition Detection (ATD) technology which allows the device to read data continuously by simply toggling the appropriate addresses. This alleviates the need to toggle $\overline{CE}$ or $\overline{OE}$ to read new data. The user must, however, toggle one of these signals to update status register data when in read status register mode.

Finally, the M29F800Ax includes on–chip program/erase control circuitry. The Write State Machine (WSM) controls block erase, byte program and page (256 byte) program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The status register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

Read

The M29F800Ax has three access read modes; the memory array, the device identifier, and the status register. The appropriate read commands must be written to the CUI. Upon initial device power–up or after exit from reset mode, the device automatically enters the read array mode. In the read array mode, low level input to $\overline{CE}$ and $\overline{OE}$, high level input to $\overline{WE}$ and $\overline{RST}$, and address signals to the address inputs (A0 – A18: word mode, A – 1, A0 – A18: byte mode) output the data of the addressed location to the data input/output (DQ0 – DQ15: word mode, DQ0 – DQ7: byte mode).

Device manufacturing, device and revision codes may read any time while the M29F800Ax is powered up by issuing the read device identifier command (90H) followed by the appropriate address which points to the device code you wish to read (see Standard Software Command Definitions for addresses and bus definitions). The manufacturing code identifies the source manufacturer of the flash die. The device code identifies the product in the manufacturers product portfolio. The revision code identifies the process and mask set used to manufacture the device. This allows the user to identify if he is using material that has been changed in feature set or product parameters that may not exist on earlier versions of the device. Refer to the Device Identifier Codes table for the manufacturing, device, and revision codes of the M29F800Ax.

The status of internal operations such as read, write, and erase, may be retrieved by issuing the read status register command at any time during the operation of the M28F900Ax. The status register shows when the device is busy performing a function (SR.7), when a block is locked or an erase/program is suspended (SR.6), program and erase success status (SR.5, and 4 respectively), when V_{PP} has dropped below allowable voltage range (SR.3), and which bank is active dur[illegible] a background program or erase operation (SR.2). See the Status Register Data table for a detailed summary of the status register bits and what they represent. The status register information can be polled at any time by issuing the read status register command or when in this mode, it can be updated by toggling $\overline{CE}$.

Write

In this and all Motorola flash memory documentation, writes will refer to data written to the command user interface and not the flash array. Data written to the flash array will be known as program operations. Writes to the Command User Interface (CUI) enable reading, programming, or erasing of memory array data, reading device identifiers as well as reading and clearing the status register. The CUI is written by

bringing $\overline{WE}$ low, while $\overline{CE}$ is low and $\overline{OE}$ is high. Addresses and data are latched on the rising edge of $\overline{WE}$ or $\overline{CE}$. Standard microprocessor write timings are used. See the Standard Software Command Definitions table for a list of commands that may be written to the CUI.

Output Disable

When $\overline{OE}$ is at V_{IH}, output from the devices is disabled and data input/output are in a high impedance (high–Z) state.

Standby

When $\overline{CE}$ is at V_{IH}, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high–Z state. If memory is deselected during block erase or program, the internal control circuits remain active and the device consumes normal active power until the operation completes.

Reset

When $\overline{RST}$ is set to V_{IL}, any program or erase operation will be aborted and the memory will be reset to the Read Array mode. Additionally, when $\overline{RST}$ is at V_{IL}, the memory is protected against accidental program or erase operation due to invalid system bus conditions that may occur during power transitions.

SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software commands into the CUI.

Read Array Command (FFH)

The device defaults to read array mode on initial device power-up. The M29F800Ax may be placed into read array mode anytime after power-up by writing FFH to the CUI. The device remains in read array mode until the other commands are written. Array reads may be accomplished either by toggling $\overline{CE}$ or $\overline{OE}$ or by leaving these signals low and toggling the appropriate address lines. This latter method is possible due to Motorola's Address Transition Detection technology which allows reads to be initiated upon detection of address line transitioning from 0 to 1 or vice versa. This alleviates the need for $\overline{CE}$ or $\overline{OE}$ hold times between reads and data may be read at minimum t_{ACC} timings continuously. Data may be read from the device in x8 data bus configuration or x16 data bus configuration depending on the state of $\overline{BYTE}$. Array reads do not cause the RY/$\overline{BY}$ pin to drive low nor does the device indicate busy in status register bit 7.

Read Device Identifier Command (90H)

Device manufacturing, device, and revision codes may read any time while the M29F800Ax is powered up by issuing the read device identifier command (90H) followed by the appropriate address which points to the device code you wish to read (see Standard Software Command Definitions for addresses and bus definitions). The manufacturing code identifies the source manufacturer of the flash die. The device code identifies the product in the manufacturers product portfolio. The revision code identifies the process and mask set used to manufacture the device. This allows the user to identify if he is using material that has been changed in feature set or product parameters that may not exist on earlier versions of the device. Refere to the Device Identifier Codes table for the manufacturing, device, and revision codes of the M29F800Ax.

Read Status Register Command (70H)

The status of internal operations such as read, write, and erase, may be retrieved by issuing the read status register command (70H) at any time during the operation of the M29F800Ax. The status register shows when the device is busy performing a function (SR.7), when a block is locked or an erase/program is suspended (SR.6), program and erase success status (SR.5, and 4 respectively), when Vpp has dropped below allowable voltage range (SR.3), and which bank is active during a background program or erase operation (SR.2). See the Status Register Data table for a detailed summary of the status register bits and what they represent. The status register information can be polled at any time by issuing the Read Status Register command or, when in this mode, it can be updated by toggling $\overline{CE}$.

Clear Status Register Command (50H)

The WSM sets the erase status and program status bits to "1"s whenever there is an error with either of these operations. The bits can only be reset by the clear status register command (50H). The user should be sure to reset these before resuming operation after a read status register command. Otherwise, a fail condition may mistakenly be given for subsequent program and erase operations.

Block Erase/Confirm Command (20H/D0H)

Automated block erase is initiated by writing the erase set-up command (20H) followed by the erase confirm command (D0H). An address within the block to be erased is required. The user may initiate a block erase operation and be able to read data in any block in the opposite bank within a processor cycle time. This allows operations such as block reclaim (when updated linked lists, such as phone numbers) to complete without the processor having to experience latencies or down time. In addition, the Motorola M29F800Ax erases any block typically in 50 ms. This streamlines the entire block reclaim/link list update process tremendously.

Program Commands

Page Program (41H) – Page program allows fast programming of 128 words/256 bytes at once. The M29F800Ax uses a very low–current programming mechanism known as Fowler–Nordheim tunneling. This method of flash cell programming allows for better reliability over the life of the device, greatly reduces the current draw during programming operations, and allows program and erase times to remain relatively constant throughout the cycling lifetime of the device. Fowler–Nordheim tunneling allows fast factory programming without the use of high voltage (12 V) to a separate programming pin. This is important from a factory programming throughput standpoint where every second costs money.

Data may also be programmed to the M29F800Ax via the 256 byte page. However, since most data storage operations typically will not store 256 bytes at a time, programming throughput is reduced. Since in–system data storage operations may be interrupted by end user inputs or internal interrupts, the M29F800Ax supports program and erase suspend operations in which the processor may service an interrupt within a cycle time and immediately resume the program/erase operation after the interrupt has been serviced.

Writing of 41H initiates the page program operation for any block in the M29F800Ax. Data/code may then be written to the device from second cycle to 129th cycle (word mode)/257th cycle (byte mode) sequentially. Address A6 – A0

(word mode)/A6 – A-1 (byte mode) have to be incremented from 00H to 7FH/FFH. After completion of data loading, the WSM controls the program pulse application and verify operation. The user may either poll RY/$\overline{BY}$ to determine when the programming operation is complete or poll the status register (SR.7). In addition, the status register may be polled to determined the success or failure of the program operations (SR.4).

DATA PROTECTION

The M29F800Ax features a flexible data protection scheme in which the user may configure protection on any block with software and enable this protection with a hardware pin. This allows maximum flexibility in choosing block protection, while enabling a two–layered guarantee against data corruption with hardware. Total data protection in all blocks may be enabled by dropping V_{CC} below the lockout voltage (1.5 V). Each method of data protection is described in detail in the following sections. See the table below for a summary of how the block locking is implemented.

Power Supply Voltages

In the flash memory industry, there exists two basic power supply standards — a single supply for performing both read and program operations (AMD devices adopt this) and a dual supply standard where one power supply is used for read operations (V_{CC}) while the second is used for program operations (V_{PP}) (Intel devices adopt this). The M29F800Ax follows the single supply standard. The V_{CC} power supply of the M29F800Ax is tolerant to 2.7 to 3.6 V. In many of today's portable applications as well as many others, two supplies do not exist in the system. Therefore, these systems should have no problem utilizing the M29F800Ax from a power supply perspective. As mentioned above, when V_{CC} is less than 1.5 V, the device is set to the read-only mode and all data in the device is completely protected. When V_{CC} is below 1.5 V, the status register will indicate this in bit 3. Any writes attempted to the device will result in a program failure state indicated by status register bit 4.

$\overline{WP}$ = V_{IL} for Block Locking

When $\overline{WP}$ is set at V_{IL}, all blocks are locked that have been configured via the lock block bits. Any program or erase operation will result in an error in the status register (SR.4) and the CUI is set to the status register read mode. All other blocks are not locked at this condition and can be programmed or erased. Therefore, $\overline{WP}$ enables via hardware block locking while software configures block locking by setting the appropriate commands. No block lock bit will take effect until $\overline{WP}$ is driven low. Data can be written in protected blocks if the $\overline{WP}$ pin is not driven low. The user should drive $\overline{WP}$ high before clearing lock block bits or setting new ones.

$\overline{WP}$ = V_{IH} for Block Unlocking

To unlock the block, $\overline{WP}$ must be set at V_{IH}. At this time, the user may clear any combination of block lock bits, set new ones or simply update the block data regardless of the state of the lock block bit associated with a particular block. Blocks are not locked until $\overline{WP}$ is high. The truth table shows the write protection status.

LOCK BLOCK COMMAND (77/D0H)

The lock block command allows software to configure locking of any of 22 blocks via 22 lock block bits. This allows not only code to be protected from spurious data writes, but parameter and boot blocks as well. Locking is enabled by driving $\overline{WP}$ low. A block is locked by issuing the lock block setup command (B0H), followed by any address within the block and the confirm command (D0H).

When $\overline{WP}$ is at a low level, data is protected only in those blocks whose block–lock bit has been set. Conversely, no lock bit will take effect until $\overline{WP}$ is driven to a low level. Block Lock bits may not be cleared. Instead, if the user wishes to change data in a locked block, the $\overline{WP}$ must be raised to a logic 1 and then desired block data changes may be made.

Vpp	$\overline{RST}$	$\overline{WP}$	Locking Status
$<V_{CCLK}$	X	X	All Block Locked
X	V_{IL}	X	Reset
$>V_{CCLK}$	V_{IH}	V_{IL}	Blocks Locked Designated
$>V_{CCLK}$	V_{IH}	V_{IH}	All Block Unlocked

PROGRAM/ERASE SUSPEND COMMAND (B0H/)

The user may suspend a program or erase operation at any time to service read functions. This is also true when program and erase are performed in the background. A program/erase suspend will allow the user to read from any block upon the next cycle. This includes the block that is currently being programmed. This is useful in applications where the system may be programming data to a particular block and receive an interrupt whose interrupt handler or associated data is stored in the block being programmed. Erase may not be suspended to read data in the block being erased. Data integrity in a block currently being erased cannot be guaranteed to read correct data. Program/erase is resumed by issuing the resume command (D0H).

READ LOCK BLOCK STATUS COMMAND (71H)

The user may read a lock bit status to check if a block is protected by issuing the read lock block status command, issuing the desired block address, and reading the status register bit on pin DQ6. If DQ6 = 1, block is locked. If DQ6 = 0, block is unlocked.

CHIP ERASE COMMAND (A7H)

The M29F800Ax supports full chip erase. The user merely issues the chip erase command (A7H) and each block is erased sequentially.

AVAILABLE TOOLS

Operating Software

All software necessary to operate all functions of the M29F800Ax is provided by Motorola on an order basis or by downloading the software from the Motorola Flash home page. This is meant to help minimize the software development effort when using Motorola Flash and therefore minimizing OEM time to market.

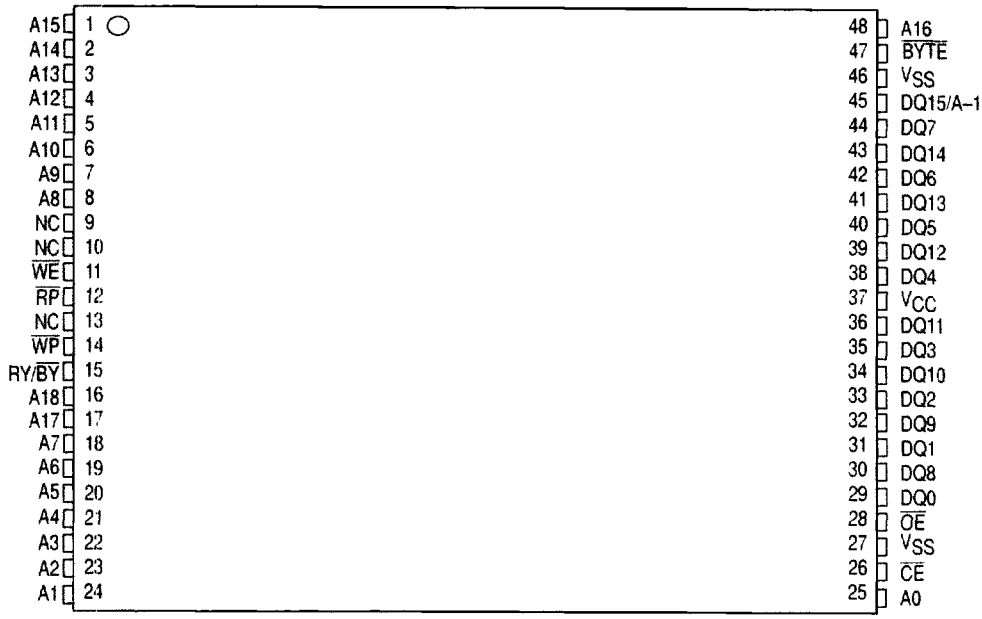
MEMORY BLOCKS

x 8 Byte Mode	x 16 Word Mode	Bottom Boot Block
F0000H – FFFFFH	78000H – 7FFFFH	32 Kword Main Block
E0000H – EFFFFH	70000H – 77FFFH	32 Kword Main Block
D0000H – DFFFFH	68000H – 6FFFFH	32 Kword Main Block
C0000H – CFFFFH	60000H – 67FFFH	32 Kword Main Block
B0000H – BFFFFH	58000H – 5FFFFH	32 Kword Main Block
A0000H – AFFFFH	50000H – 57FFFH	32 Kword Main Block
90000H – 9FFFFH	48000H – 4FFFFH	32 Kword Main Block
80000H – 8FFFFH	40000H – 47FFFH	32 Kword Main Block
70000H – 7FFFFH	38000H – 3FFFFH	32 Kword Main Block
60000H – 6FFFFH	30000H – 37FFFH	32 Kword Main Block
50000H – 5FFFFH	28000H – 2FFFFH	32 Kword Main Block
40000H – 4FFFFH	20000H – 27FFFH	32 Kword Main Block
30000H – 3FFFFH	18000H – 1FFFFH	32 Kword Main Block
20000H – 2FFFFH	10000H – 17FFFH	32 Kword Main Block
10000H – 1FFFFH	08000H – 0FFFFH	32 Kword Main Block
08000H – 0FFFFH	04000H – 07FFFH	16 Kword Main Block
06000H – 07FFFH	03000H – 03FFFH	4 Kword Parameter Block
04000H – 05FFFH	02000H – 02FFFH	4 Kword Parameter Block
00000H – 03FFFH	00000H – 01FFFH	8 Kword Boot Block

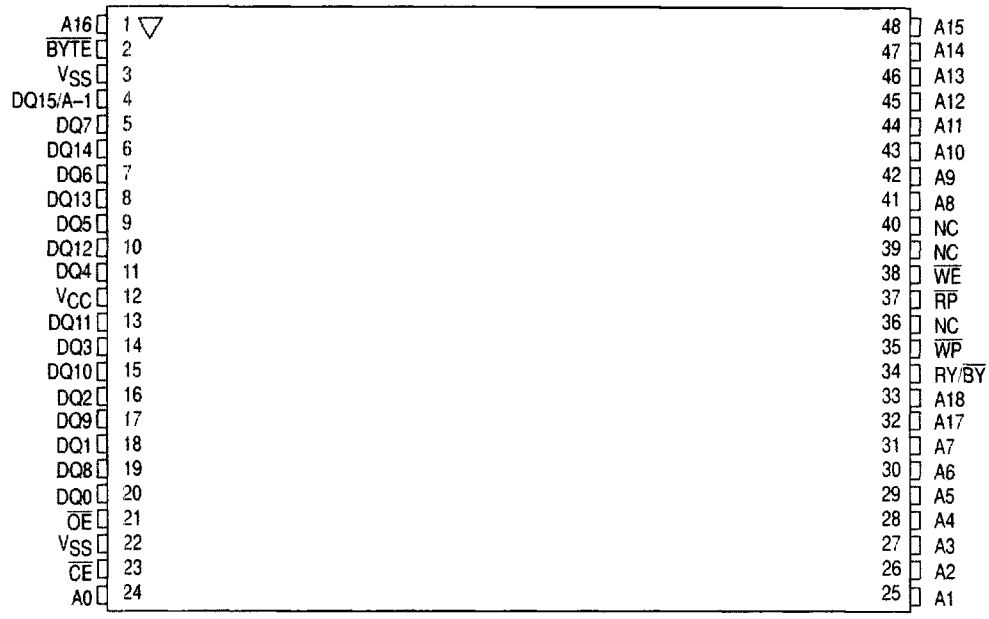
x 8 Byte Mode	x 16 Word Mode	Top Boot Block
FC000H – FFFFFH	7E000H – 7FFFFH	8 Kword Boot Block
FA000H – FBFFFH	7D000H – 7DFFFH	4 Kword Parameter Block
F8000H – F9FFFH	7C000H – 7CFFFH	4 Kword Parameter Block
F0000H – F7FFFH	78000H – 7BFFFH	16 Kword Main Block
E0000H – EFFFFH	70000H – 77FFFH	32 Kword Main Block
D0000H – DFFFFH	68000H – 6FFFFH	32 Kword Main Block
C0000H – CFFFFH	60000H – 67FFFH	32 Kword Main Block
B0000H – BFFFFH	58000H – 5FFFFH	32 Kword Main Block
A0000H – AFFFFH	50000H – 57FFFH	32 Kword Main Block
90000H – 9FFFFH	48000H – 4FFFFH	32 Kword Main Block
80000H – 8FFFFH	40000H – 47FFFH	32 Kword Main Block
70000H – 7FFFFH	38000H – 3FFFFH	32 Kword Main Block
60000H – 6FFFFH	30000H – 37FFFH	32 Kword Main Block
50000H – 5FFFFH	28000H – 2FFFFH	32 Kword Main Block
40000H – 4FFFFH	20000H – 27FFFH	32 Kword Main Block
30000H – 3FFFFH	18000H – 1FFFFH	32 Kword Main Block
20000H – 2FFFFH	10000H – 17FFFH	32 Kword Main Block
10000H – 1FFFFH	08000H – 0FFFFH	32 Kword Main Block
00000H – 0FFFFH	00000H – 07FFFH	32 Kword Main Block

PIN ASSIGNMENTS

TSOP STANDARD PINOUT



TSOP REVERSE PINOUT



PIN DESCRIPTIONS

TSOP Pin Locations	TSOP Reverse Pin Locations	Symbol	Type	Description
1 – 8, 16 – 25, 48	1, 24 – 33, 41 – 48	A0 – A18	Input	Memory Address Input.
47	2	$\overline{BYTE}$	Input	Byte Enable Input: $\overline{BYTE}$ low places device in x8 mode. All data is then input or output on DQ0 – DQ7, and other DQs float. DQ15 becomes the lowest order address that decodes between the upper and lower byte. $\overline{BYTE}$ high places the device in word–wide (x16) mode and DQ15 reverts back to the data I/O function.
26	23	$\overline{CE}$	Input	Chip Enable Input activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ high deselects the device and reduces power consumption to standby levels upon completion of any current data write or erase operation.
29 – 36, 38 – 45	4 – 11, 13 – 20	DQ0 – DQ15/A–1	I/O	Input/Output for data and commands.
28	21	$\overline{OE}$	Input	Output Enable Input gates device data through the output buffers.
12	37	$\overline{RP}$	Input	Reset/Power Down Input.
15	34	RY/$\overline{BY}$	Output	Ready/Busy Output indicates internal WSM status. RY/$\overline{BY}$ low indicates that the WSM is busy performing an operation. RY/$\overline{BY}$ high indicates that the WSM has completed all operations, or erase or program is suspended.
11	38	$\overline{WE}$	Input	Write Enable Input controls access to the CUI and page buffer.
14	35	$\overline{WP}$	Input	Write Protect Input prevents any modifications to memory blocks where lock–bits are set to "0" and WP is low.
37	12	V_{CC}	Supply	Power Supply (3.3 V).
27, 46	3, 22	V_{SS}	Supply	Ground.
9, 10, 13	36, 39, 40	NC	—	No Connection.

MODE SELECTION (Word–Wide Mode ($\overline{BYTE}$ = V_{IH}), Byte–Wide Mode ($\overline{BYTE}$ = V_{IL})) (See Note 1)

Operation		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	DQ	RY/$\overline{BY}$
Read	Array	L	L	H	H	Data Out	V_{OH}
	Status Register	L	L	H	H	Status Register	X[1]
	Lock Bit Status	L	L	H	H	Lock Bit (DQ6)	X
	Identifier Code	L	L	H	H	Identifier Code	V_{OH}
Output Disable		L	H	H	H	High–Z	X
Standby		H	X[2]	X	H	High–Z	X
Write	Program	L	H	L	H	Command/D_{in}	X
	Erase	L	H	L	H	Command	X
	Others	L	H	L	H	Command	X
Deep Power Down		X	X	X	L	High–Z	V_{OH}

NOTES:
1. X at RY/$\overline{BY}$ is V_{OL} or $V_{OH(Hi-Z)}$. The RY/$\overline{BY}$ is an open drain output pin and indicates status of the internal WSM. When low, it indicates that the WSM is Busy performing an operation. A pull–up resistor of 10 KΩ is required to allow the RY/$\overline{BY}$ signal to transistion high indicating a Ready WSM condition.
2. X can be V_{IL} or V_{IH} for control pins.

STANDARD SOFTWARE COMMAND DEFINITIONS (See Note 1)

Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle		
	Mode	Addr	Data (DQ7 – DQ0)	Mode	Addr	Data (DQ7 – DQ0)	Mode	Addr	Data (DQ7 – DQ0)
Read Array	Write	X	FFH						
Read Device Identifier	Write	X	90H	Read	IA[2]	ID[2]			
Read Status Register	Write	X	70H	Read	X	SRD[3]			
Clear Status Register	Write	X	50H						
Page Program[4]	Write	X	41H	Write	WA0[4]	WD0[4]	Write	WA1	WD1
Block Erase/Confirm	Write	X	20H	Write	BA[5]	D0H			
Suspend	Write	X	B0H						
Resume	Write	X	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA	DQ6[6]			
Lock Bit Program/Confirm	Write	X	77H	Write	BA	D0H			
Erase all Unlocked Blocks	Write	X	A7H	Write	X	D0H			
Sleep[7]	Write	X	F0H						

NOTES:
1. In the word–wide mode, upper byte data (DQ8 – DQ15) is ignored.
2. IA = ID code address: A0 = V_{IL} (manufacturer's code) : A0 = V_{IH} (device code), ID = ID code, $\overline{BYTE}$ = V_{IL}: A–1, A1 – A18 = V_{IL}, $\overline{BYTE}$ = V_{IH}: A1 – A18 = V_{IL}.
3. SRD = Status Register Data.
4. WA = Write Address, WD = Write Data. $\overline{BYTE}$ = V_{IL}: Write Address and Write Data must be provided sequentially from 00H to FFH for A–1 – A6. Page size is 256 Byte (256 byte x 8 bit), $\overline{BYTE}$ = V_{IH}: Write Address and Write Data must be provided sequentially from 00H to 7FH for A0 – A6. Page size is 128 word (128 word x 16 bits).
5. BA = Block Address (Address except Block Address must be V_{IH}).
6. DQ6 provides Block Lock Status, DQ6 = 1: Block Unlock, DQ6 = 0: Block Locked.
7. Sleep command (F0H) put the device into the sleep mode after completing the current operation. The active current is reduced to Deep Power Down levels. The Read Array command (FFH) must be written to get the device out of sleep mode.

BLOCK LOCKING (See Notes 1 and 2)

$\overline{RP}$	$\overline{WP}$	Lock Bit (Internally)	Write Protection Provided
V_{IL}	X	X	All Blocks Locked (Deep Power Down Mode)
V_{HH}	X	X	All Blocks Unlocked
V_{IH}	V_{IL}	0	Blocks Locked (Depend on Lock Bit Data)
V_{IH}	V_{IL}	1	Blocks Unlocked (Depend on Lock Bit Data)
V_{IH}	V_{IH}	X	All Blocks Unlocked

NOTES:
1. DQ6 provides Lock Status of each block after writing the Read Lock Status command (71H).
2. $\overline{WP}$ pin must not be switched during performing Read/Write operations or WSM Busy (WSM = 0).

STATUS REGISTER DATA (SRD) (See Notes 1 through 3)

Symbol	Status	Definition	
		"1"	"0"
SR.7 (DQ7)	Write State Machine Status	Ready	Busy
SR.6 (DQ6)	Suspend Status	Suspend	Operation in Progress/Completed
SR.5 (DQ5)	Erase Status	Error	Successful
SR.4 (DQ4)	Program Status	Error	Successful
SR.3 (DQ3)	Block Status after Program	Error	Successful
SR.2 (DQ2)	Reserved	—	—
SR.1 (DQ1)	Reserved	—	—
SR.0 (DQ0)	Device Sleep	Device in Sleep	Device Not in Sleep

NOTES:
1. The RY/$\overline{BY}$ is an open drain output pin and indicates status of the internal WSM. When low, it indicates that the WSM is Busy performing an operation.
2. A pull–up resistor of 10 kΩ to 100 kΩ is required to allow the RY/$\overline{BY}$ signal to transition high indicating a Ready WSM condition.
3. D3 indicates the block status after the page programming. When D3 is "1", the block must be erased before reprogramming.

DEVICE INDENTIFIER CODES (See Notes 1 and 2)

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	1CH	0	0	0	1	1	1	0	0
Device Code (T)	V_{IH}	5DH	0	1	0	1	1	1	0	1
Device Code (B)	V_{IH}	5EH	0	1	0	1	1	1	1	0

NOTES:
1. In the word–wide mode, the same data as DQ0 – DQ7 is read out from DQ8 – DQ15.
2. A9 = V_{HH} mode: A9 = 11.5 V – 13 V. Set A9 to V_{HH} min 200 ns before falling edge of $\overline{CE}$ in ready status. Minimum 200 ns after return to V_{IH}, device cannot be accessed. A1 – A8, A10 – A18, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}. D15/A–1 = V_{IL} ($\overline{BYTE}$ = L).

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Parameter	Symbol	Conditions	Min	Max	Unit	Notes
Power Supply Voltage	V_{CC}	With Respect to Ground	– 0.2	4.6	V	
All Input or Output Voltage Except V_{CC}, A9, $\overline{RP}$	V_{in}, V_{out}		– 0.6	4.6	V	1
A9, $\overline{RP}$ Supply Voltage	V_{in}, V_{out}		– 0.6	14	V	
Ambient Temperature	T_A		– 40	85	°C	
Temperature Under Bias	T_{BS}		– 50	95	°C	
Storage Temperature Range	T_{stg}		– 65	125	°C	
Output Short Circuit Current	I_{out}			100	mA	

NOTES:
1. Minimum dc voltage on input or I/O pins is – 0.5 V. During transitions this level may undershoot V_{SS} to – 2.0 V for periods of up to 20 ns. Maximum dc voltage on I/O pins is V_{CC} + 0.5 V. During voltage transitions, I/O pins may overshoot to V_{CC} + 1.5 V for periods of up to 20 ns.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = – 40 to 85°C, Unless Otherwise Noted)

DC CHARACTERISTICS (Typical Values at V_{CC} = 3.3 V, T_A = 25°C, All Currents are in RMS Unless Otherwise Noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit	Notes
V_{CC} Read Current for Word or Byte	V_{CC} = 3.6 V, V_{in} = V_{IL}/V_{IH}, $\overline{CE}$ = V_{IL}, $\overline{RP}$ = $\overline{OE}$ = V_{IH}, f = 10 MHz, I_{out} = 0 mA	I_{CC1}	—	7	25	mA	
V_{CC} Write Current for Word or Byte	V_{CC} = 3.6 V, V_{in} = V_{IL}/V_{IH}, $\overline{CE}$ = $\overline{WE}$ = V_{IL}, $\overline{RP}$ = $\overline{OE}$ = V_{IH}	I_{CC2}	—	—	30	mA	
V_{CC} Program Current	V_{CC} = 3.6 V, V_{in} = V_{IL}/V_{IH}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}	I_{CC3}	—	—	40	mA	
V_{CC} Erase Current	V_{CC} = 3.6 V, V_{in} = V_{IL}/V_{IH}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}	I_{CC4}	—	—	40	mA	
V_{CC} Suspend Current	V_{CC} = 3.6 V, V_{in} = V_{IL}/V_{IH}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH}	I_{CC5}	—	—	200	µA	
V_{CC} Standby Current	V_{CC} = 3.6 V, V_{in} = V_{IL}/V_{IH}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{IH} V_{CC} = 3.6 V, V_{in} = V_{SS} or V_{CC}, $\overline{CE}$ = $\overline{RP}$ = $\overline{WP}$ = V_{CC} ± 0.3 V	I_{SB1} I_{SB2}	— —	50 1	200 5	µA	
V_{CC} Deep Power Down Current	V_{CC} = 3.6 V, V_{in} = V_{IL}/V_{IH}, $\overline{RP}$ = V_{IL} V_{CC} = 3.6 V, V_{in} = V_{SS} or V_{CC}, $\overline{RP}$ = V_{SS} ± 0.3 V	I_{SB3} I_{SB4}	— —	5 1	15 5	µA	
$\overline{RP}$ All Block Unlock Current	$\overline{RP}$ = V_{HH} max	I_{RP}	—	—	100	µA	
A9 Intelligent Identifier Current	A9 = V_{ID} max	I_{ID}	—	—	100	µA	
$\overline{RP}$ Unlock Voltage		V_{IHH}	11.4	12	12.6	V	
A9 Intelligent Identifier Voltage		V_{ID}	11.4	12	12.6	V	
Input Leakage Current	0 V ≤ V_{in} ≤ V_{CC}	I_{LI}	—	—	± 1.0	µA	
Output Leakage Current	0 V ≤ V_{out} ≤ V_{CC}	I_{LO}	—	—	± 10	µA	
Input Low Voltage		V_{IL}	– 0.5	—	0.8	V	
Input High Voltage		V_{IH}	2.0	—	V_{CC} + 0.5	V	
Output Low Voltage	I_{OL} = 5.8 mA	V_{OL}	—	—	0.45	V	
Output High Voltage	I_{OH} = – 2.5 mA I_{OH} = – 100 µA	V_{OH1} V_{OH2}	0.85 V_{CC} V_{CC} – 0.4	— —	— —	V	
Low V_{CC} Lock Out Voltage		V_{LKO}	1.5	—	2.5	V	1

NOTES:

1. To protect against initiation of write cycle during V_{CC} Power Up/Down, a write cycle is locked out for V_{CC} less than V_{LKO}. If V_{CC} is less than V_{LKO}, Write State Machine is reset to read mode. When the Write State Machine is in busy state, if V_{CC} is less than V_{LKO}, the alteration of memory contents may occur.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 3.3 V, V_{in} = V_{out} = 0 V, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (Address, Control Pins)	C_{in}	—	8	pF
Output Capacitance	C_{out}	—	12	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = – 40 to 85°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Voltage Level ..... V_{IL} = 0 V, V_{IH} = 3.0 V
Input Rise/Fall Time ..... ≤ 10 ns (100/120 ns), ≤ 5 ns (80 ns)

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ ONLY MODE

Parameter	Symbol		M29F800A3–80		M29F800A3–10		M29F800A3–12		Unit
	Std	Alt	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	80	—	100	—	120	—	ns
Address Access Time	t_{AVQV}	t_{AD}	—	80	—	100	—	120	ns
Chip Enable Access Time	t_{ELQV}	t_{CE}	—	80	—	100	—	120	ns
Output Enable Access Time	t_{GLQV}	t_{OE}	—	40	—	50	—	60	ns
$\overline{RP}$ Access Time	t_{PHQV}	t_{RP}	—	300	—	300	—	600	ns
Chip Enable to Output Low–Z	t_{ELQX}	t_{CLZ}	0	—	0	—	0	—	ns
Chip Enable High to Output High–Z	t_{EHQZ}	t_{DFCE}	—	25	—	25	—	30	ns
Output Enable to Output Low–Z	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns
Output Enable High to Output High–Z	t_{GHQZ}	t_{DFOE}	—	25	—	25	—	30	ns
$\overline{RP}$ Low to Output High–Z	t_{PLQZ}	t_{PHZ}	—	150	—	150	—	300	ns
$\overline{BYTE}$ Access Time	$t_{FL/HQV}$	t_{BYTE}	—	80	—	100	—	120	ns
$\overline{BYTE}$ Low to Output High–Z	t_{FLQZ}	t_{BHZ}	—	25	—	25	—	30	ns
Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$	t_{OH}	t_{OH}	0	—	0	—	0	—	ns
$\overline{CE}$ Low to $\overline{BYTE}$ High or Low	$t_{ELFL/H}$	t_{BCD}	—	5	—	5	—	5	ns
Address to $\overline{BYTE}$ High or Low	$t_{AVFL/H}$	t_{BAD}	—	5	—	5	—	5	ns
$\overline{OE}$ Hold from $\overline{WE}$ High Read Busy Other Read	t_{WHGL}	t_{OEH}	80 0	—	100 0	—	120 0	—	ns
$\overline{RP}$ Recovery Time Before Read	t_{PHEL}	t_{PWH}	0	—	0	—	0	—	ns

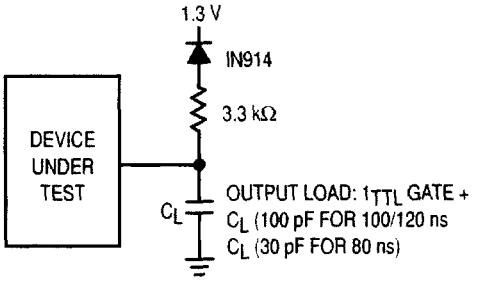
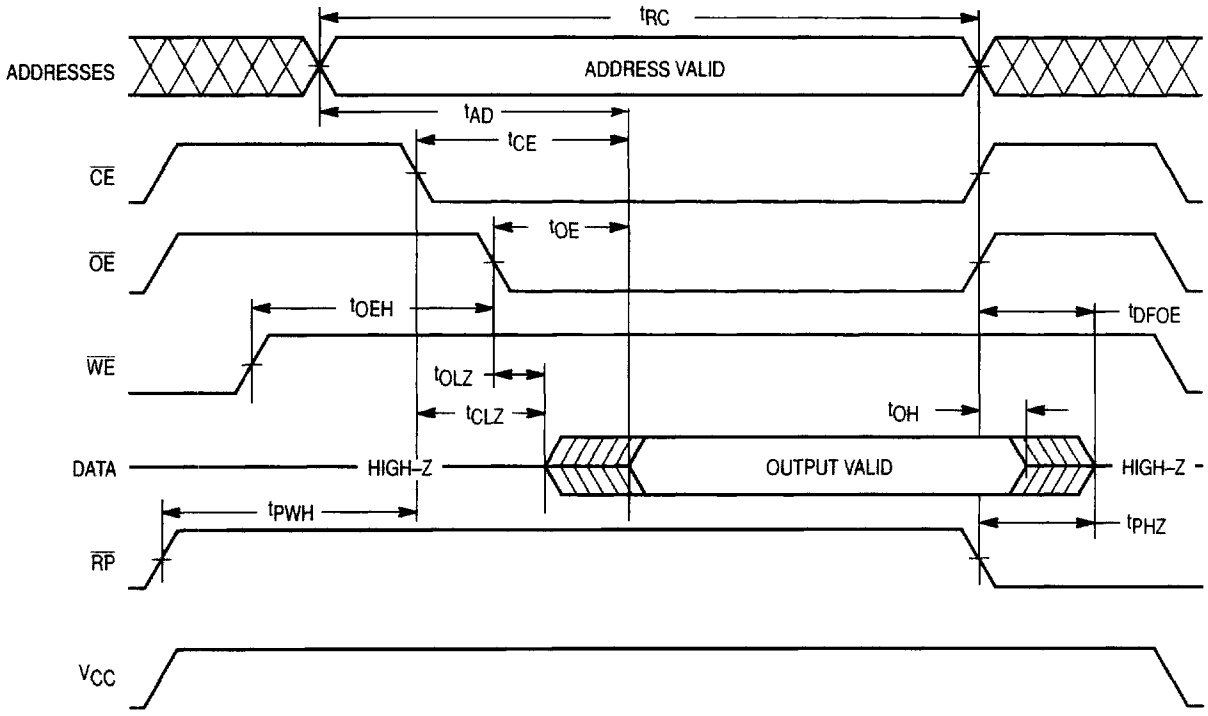


Figure 1. Test Conditions

READ CYCLE


tRC
ADDRESSES
ADDRESS VALID
tAD
tCE
CE
tOE
OE
tOEH
tDFOE
WE
tOLZ
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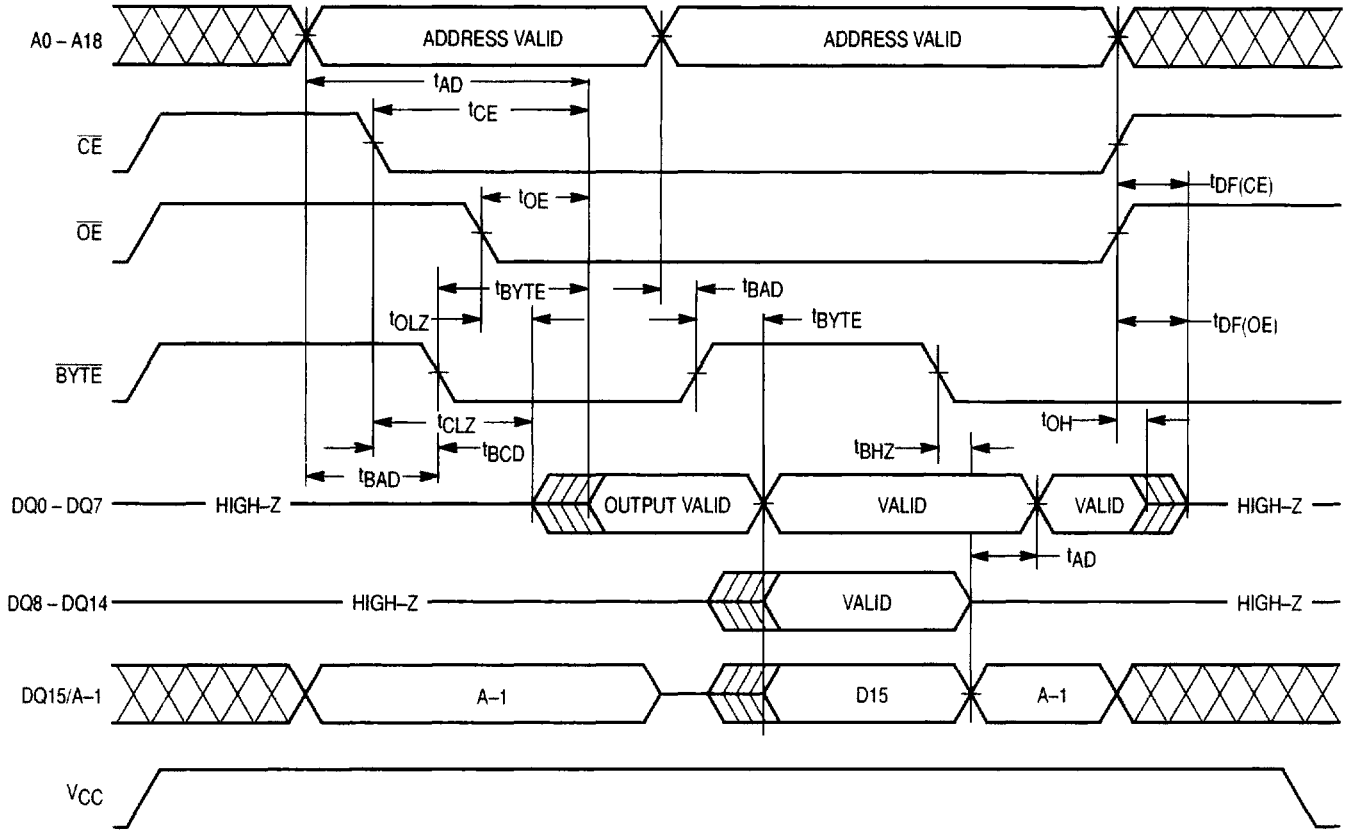
tOH
DATA
HIGH-Z
OUTPUT VALID
HIGH-Z
tPWH
tPHZ
RP
VCC

BYTE READ CYCLE



COMMAND WRITE OPERATIONS ($\overline{WE}$ CONTROL) (Typical Values at V_{CC} = 3.3 V, T_A = 25°C)

Parameter	Symbol		M29F800A3–80			M29F800A3–10			M29F800A3–12			Unit
	Std	Alt	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	80		—	100		—	120		—	ns
Address Setup Time	t_{AVWL}	t_{AS}	50		—	50		—	50		—	ns
Address Hold Time	t_{WHAX}	t_{AH}	10		—	10		—	10		—	ns
Data Setup Time	t_{DVWH}	t_{DS}	50		—	50		—	50		—	ns
Data Hold Time	t_{WHDX}	t_{DH}	10		—	10		—	10		—	ns
Chip Enable Setup Time	t_{ELWL}	t_{CS}	0		—	0		—	0		—	ns
Chip Enable Hold Time	t_{WHEH}	t_{CH}	0		—	0		—	0		—	ns
Write Pulse Width	t_{WLWH}	t_{WP}	60		—	60		—	60		—	ns
Write Pulse Width High	t_{WHWL}	t_{WPH}	20		—	20		—	20		—	ns
$\overline{BYTE}$ Enable High or Low Setup Time	$t_{FL/HWH}$	t_{BS}	50		—	50		—	50		—	ns
$\overline{BYTE}$ Enable High or Low Hold Time	$t_{WHFL/H}$	t_{BH}	80		—	100		—	120		—	ns
Block Lock Setup to Write Enable High	t_{PHHWH}	t_{BLS} t_{WPS}	80		—	100		—	120		—	ns
Block Lockhold from Valid SRD	t_{QVPH}	t_{BLH} t_{WPH}	0		—	0		—	0		—	ns
Duration of Auto Program Operation	t_{WHRH1}	t_{DAP}	—	15	120	—	15	120	—	15	120	ms
Duration of Auto Block Erase Operation	t_{WHRH2}	t_{DAE}	—	50	600	—	50	600	—	50	600	ms
Write Enable High to RY/$\overline{BY}$ Low	t_{WHRL}	t_{WHRL}	—		80	—		100	—		120	ns
$\overline{RP}$ High Recovery to Write Enable Low	t_{PHWL}	t_{PS}	500		—	500		—	500		—	ns

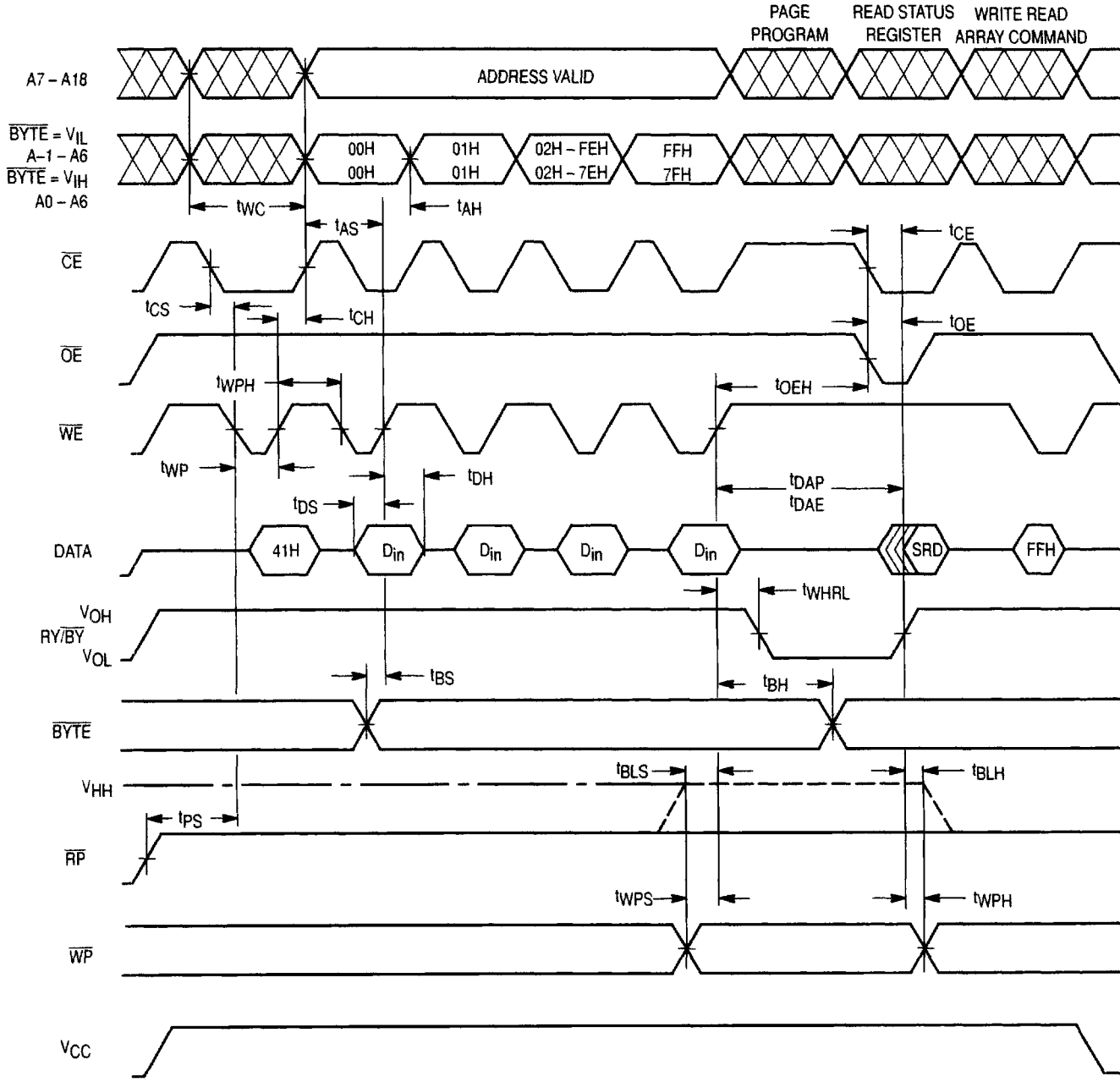
IMPORTANT NOTE:

Read timing parameters during command write operations mode are the same as during read–only operations mode.

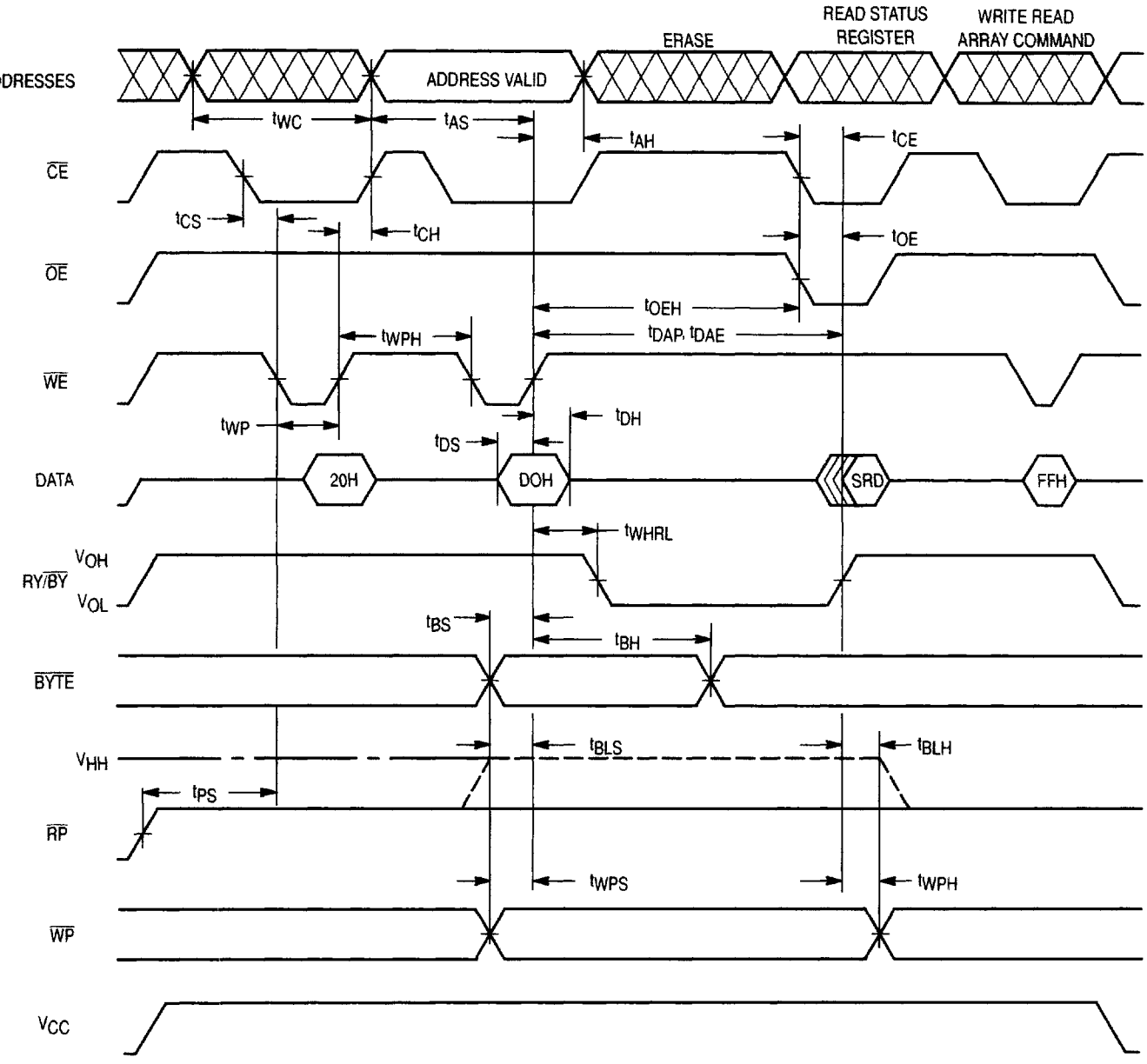
ERASE AND PROGRAM PERFORMANCE (Typical Values at V_{CC} = 3.3 V, T_A = 25°C. These values exclude system level overhead.)

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Block Erase Time	t_{BERS}	—	50	600	ms
Main Block Write Time (Page Mode)	t_{BW}	—	1.9	3.8	s
Page Write Time	t_{PW}	—	7.5	120	ms

PAGE PROGRAM OPERATION ($\overline{WE}$ CONTROLLED)



ERASE OPERATION ($\overline{WE}$ CONTROLLED)



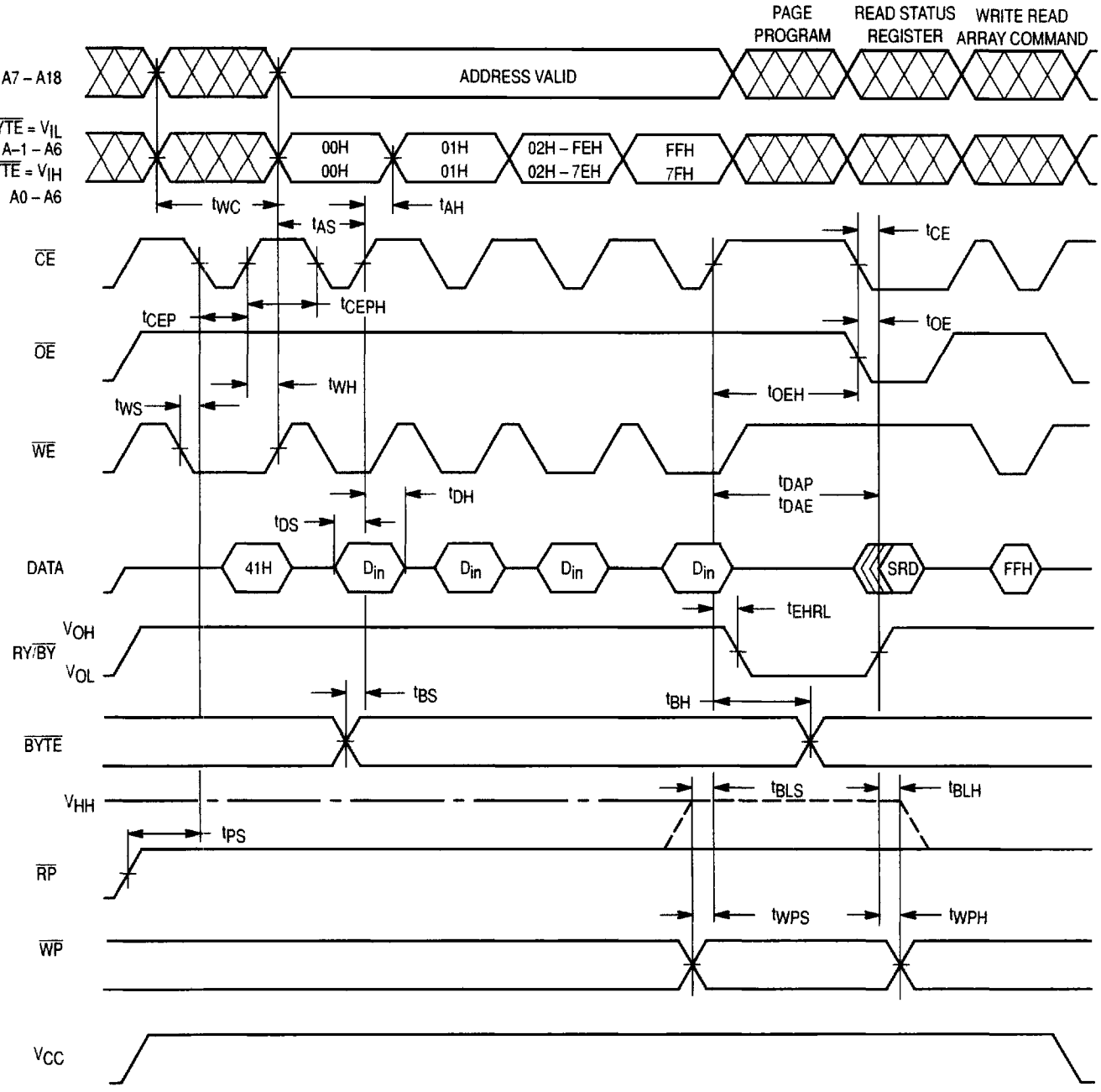
COMMAND WRITE OPERATIONS ($\overline{CE}$ CONTROL) (Typical values at V_{CC} = 3.3 V, T_A = 25°C)

Parameter	Symbol		M29F800A3–80			M29F800A3–10			M29F800A3–12			Unit
	Std	Alt	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	80		—	100		—	120		—	ns
Address Setup Time	t_{AVEH}	t_{AS}	50		—	50		—	50		—	ns
Address Hold Time	t_{EHAX}	t_{AH}	10		—	10		—	10		—	ns
Data Setup Time	t_{DVEH}	t_{DS}	50		—	50		—	50		—	ns
Data Hold Time	t_{EHDX}	t_{DH}	10		—	10		—	10		—	ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		—	0		—	0		—	ns
Write Enable Hold Time	t_{EHWH}	t_{WH}	0		—	0		—	0		—	ns
$\overline{CE}$ Pulse Width	t_{ELEH}	t_{CEP}	60		—	60		—	60		—	ns
$\overline{CE}$ Pulse Width High	t_{EHEL}	t_{CEPH}	20		—	20		—	20		—	ns
$\overline{BYTE}$ Enable High or Low Setup Time	$t_{FL/HEH}$	t_{BS}	50		—	50		—	50		—	ns
$\overline{BYTE}$ Enable High or Low Hold Time	$t_{EHFL/H}$	t_{BH}	80		—	100		—	120		—	ns
Block Lock Setup to Write Enable High	t_{PHHEH}	t_{BLS} t_{WPS}	80		—	100		—	120		—	ns
Block Lockhold from Valid SRD	t_{QVPH}	t_{BLH} t_{WPH}	0		—	0		—	0		—	ns
Duration of Auto Program Operation	t_{EHRH1}	t_{DAP}	—	15	120	—	15	120	—	15	120	ms
Duration of Auto Block Erase Operation	t_{EHRH2}	t_{DAE}	—	50	600	—	50	600	—	50	600	ms
$\overline{CE}$ Enable High to RY/$\overline{BY}$ Low	t_{EHRL}	t_{EHRL}	—		80	—		100	—		120	ns
$\overline{RP}$ High Recovery to Write Enable Low	t_{PHEL}	t_{PS}	500		—	500		—	500		—	ns

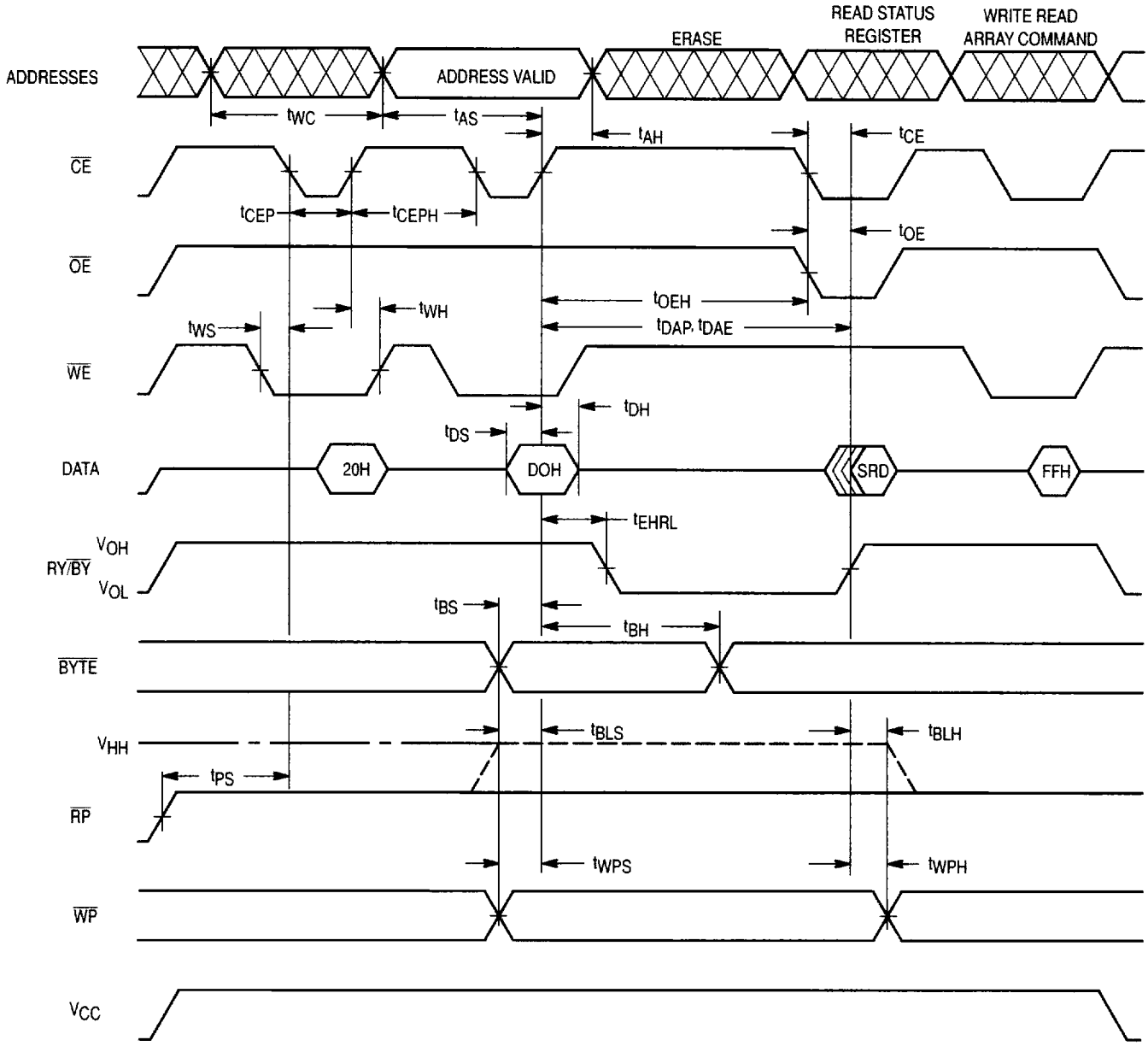
IMPORTANT NOTE:

Read timing parameters during command write operations mode are the same as during read–only operations mode.

PAGE PROGRAM OPERATION ($\overline{CE}$ CONTROLLED)



ERASE OPERATION ($\overline{CE}$ CONTROLLED)



V_{CC} POWER UP/DOWN TIMING

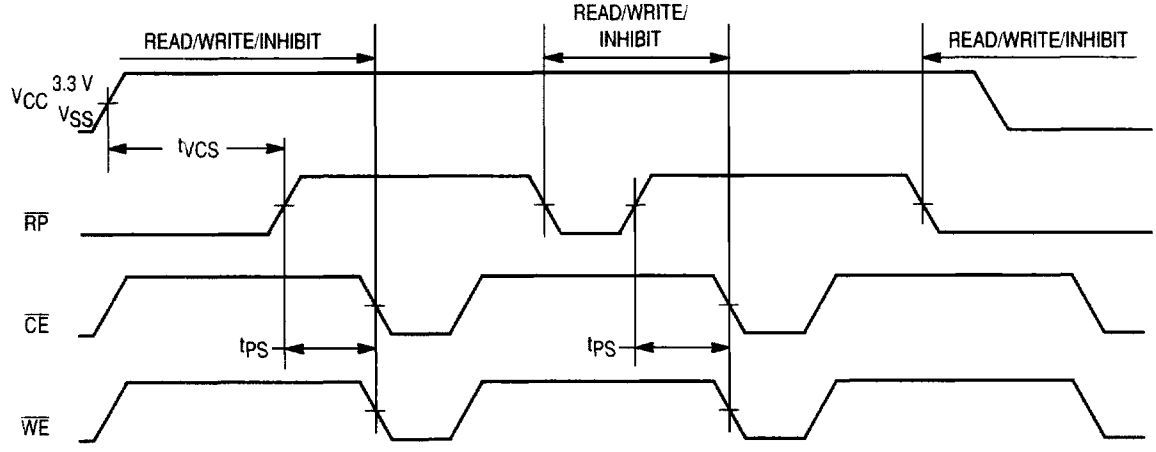
(Typical Values at V_{CC} = 3.3 V, T_A = 25°C. These values exclude system level overhead.) (See Notes 1 through 6.)

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
$\overline{RP}$ = V_{IH} Setup Time from V_{CC} Min.	t_{VCS}	2	—	—	µs

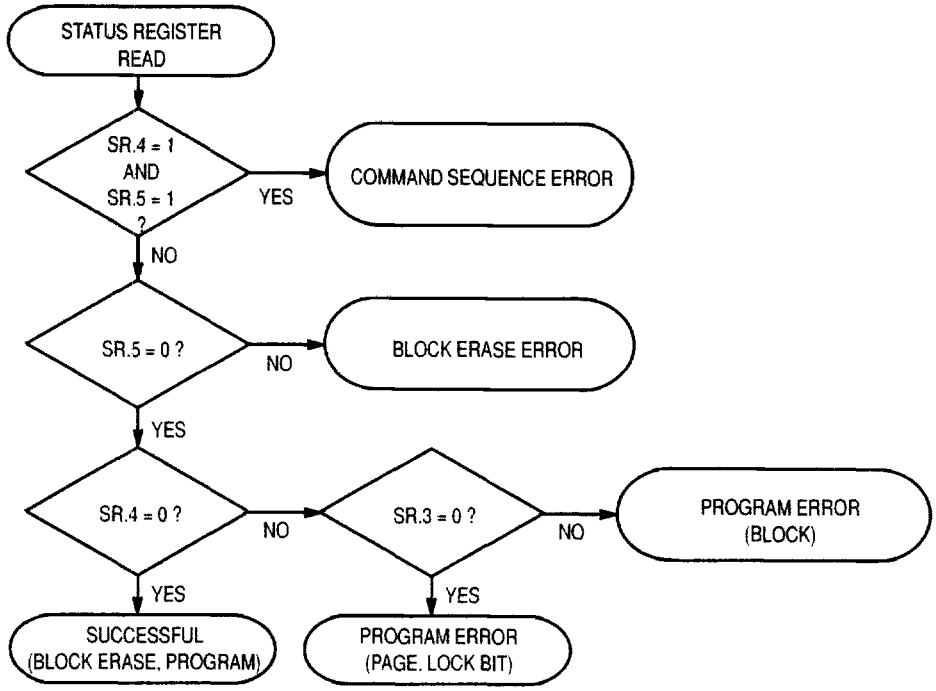
NOTES:

1. During Power Up/Down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
2. The device must be protected against initiation of Write cycle for memory contents during Power Up/Down.
3. The delay time of minimum 2 µs is always required before Read operation or Write operation is initiated from the time V_{CC} reaches V_{CC} min during Power Up/Down. By holding $\overline{RP}$ V_{IL}, the contents of memory is protected during V_{CC} Power Up/Down.
4. During Power Up, $\overline{RP}$ must be held V_{IL} for minimum 2 µs from the time V_{CC} reaches V_{CC} min.
5. During Power Down, $\overline{RP}$ must be held V_{IL} until V_{CC} reaches V_{SS}.
6. $\overline{RP}$ does not have latch mode so $\overline{RP}$ must be held V_{IH} during Read operation or Erase/Program operation.

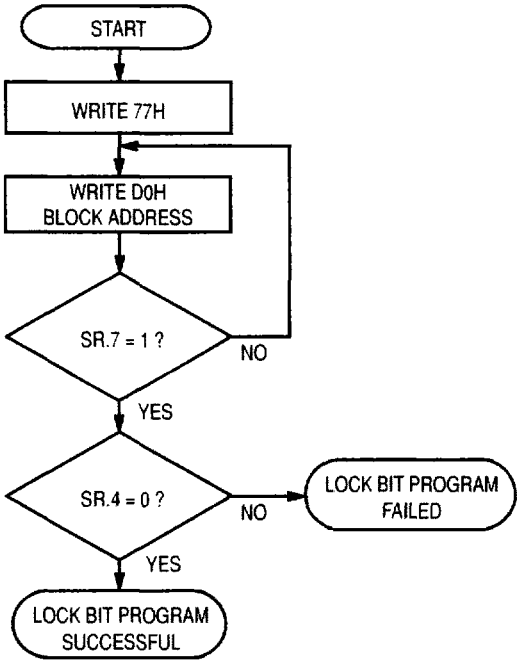
V_{CC} POWER UP/DOWN



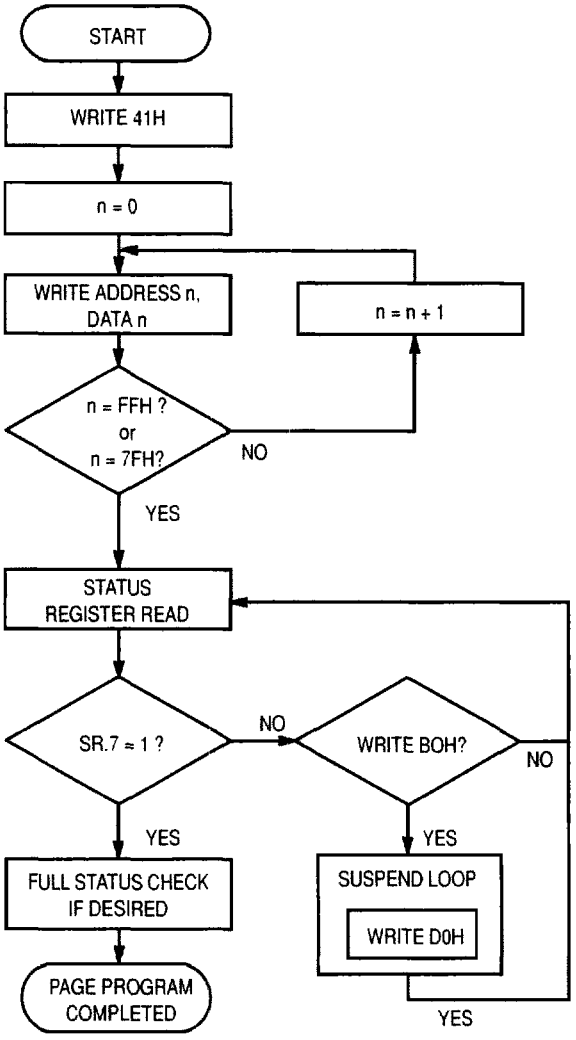
FULL STATUS CHECK PROCEDURE



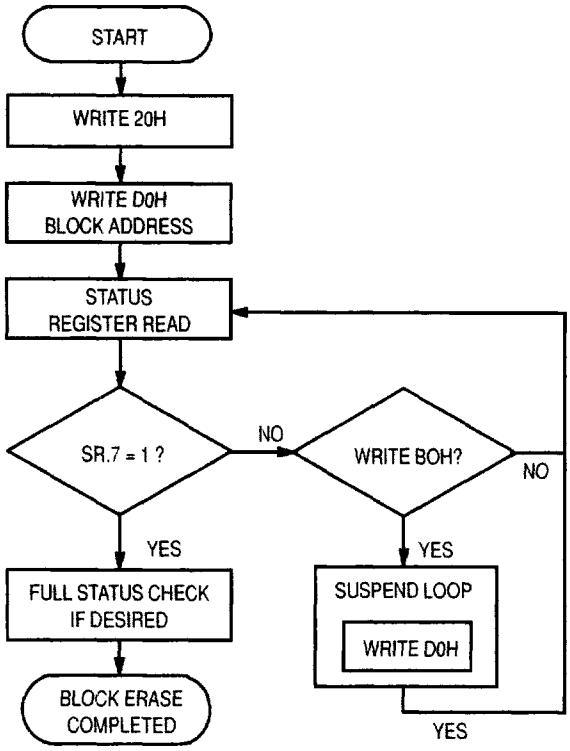
LOCK BIT FLOW CHART



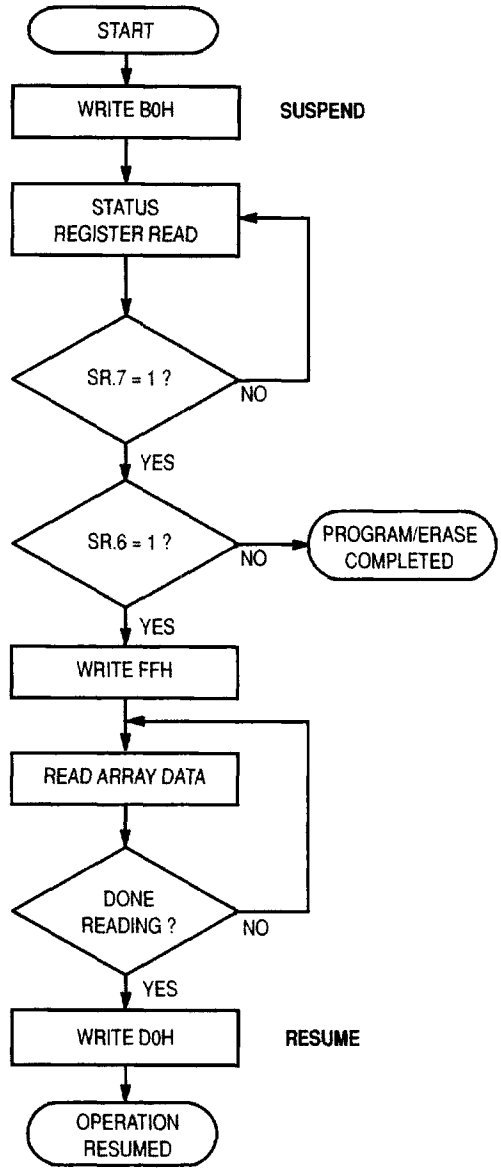
PAGE PROGRAM FLOW CHART



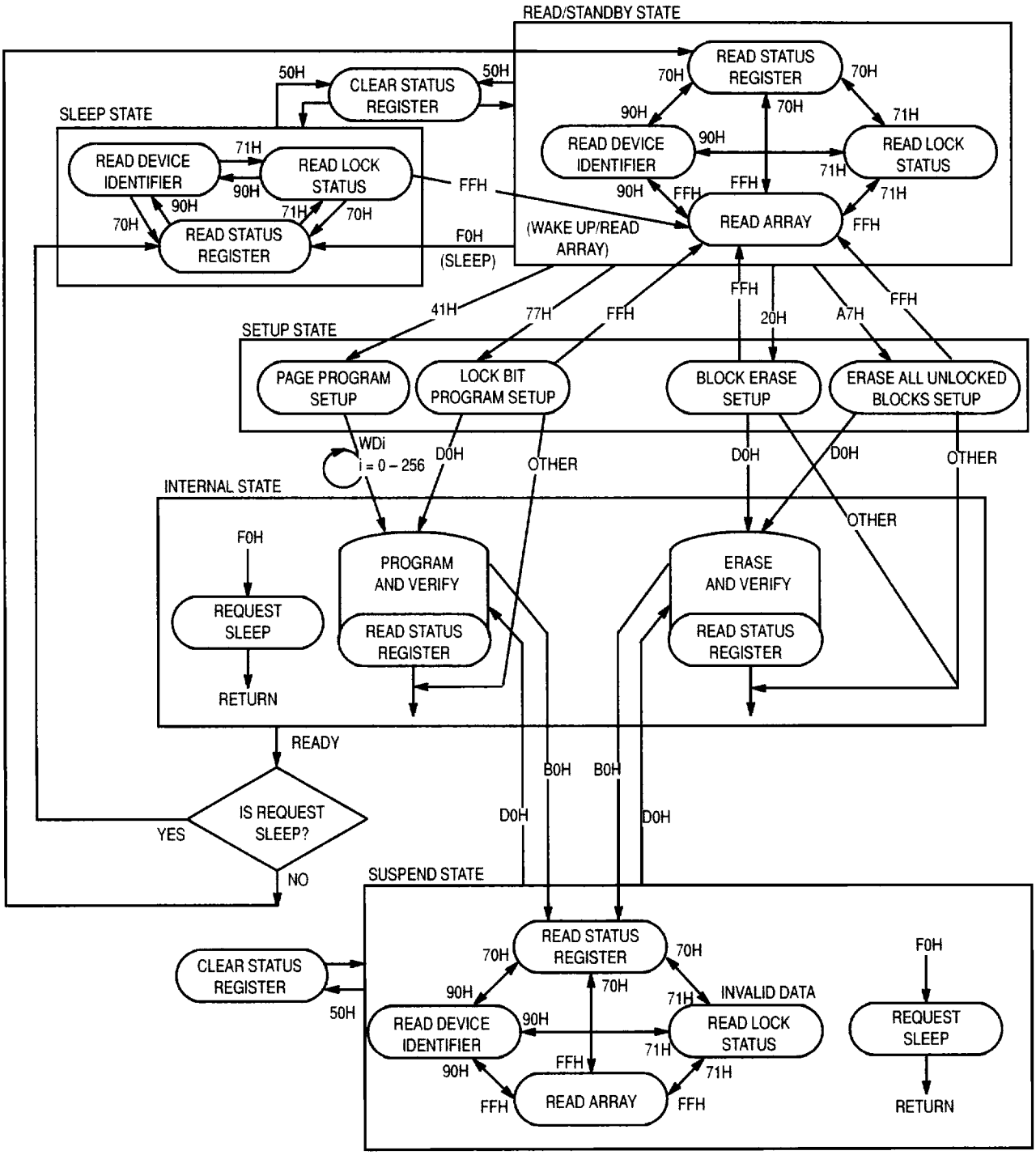
BLOCK ERASE FLOW CHART



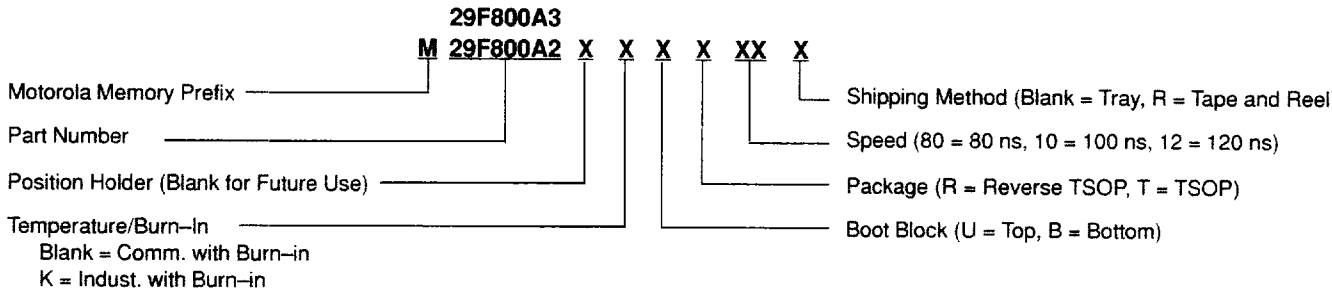
SUSPEND/RESUME FLOW CHART



OPERATION STATUS AND EFFECTIVE COMMANDS



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —

M29F800A3KUT80	M29F800A3KUT10	M29F800A3KUT12
M29F800A3KUR80	M29F800A3KUR10	M29F800A3KUR12
M29F800A3KUT80R	M29F800A3KUT10R	M29F800A3KUT12R
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M29F800A3KBT80	M29F800A3KBT10	M29F800A3KBT12
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M29F800A3BR80	M29F800A3BR10	M29F800A3BR12
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M29F800A3BR80R	M29F800A3BR10R	M29F800A3BR12R
M29F800A2KUT80	M29F800A2KUT10	M29F800A2KUT12
M29F800A2KUR80	M29F800A2KUR10	M29F800A2KUR12
M29F800A2KUT80R	M29F800A2KUT10R	M29F800A2KUT12R
M29F800A2KUR80R	M29F800A2KUR10R	M29F800A2KUR12R
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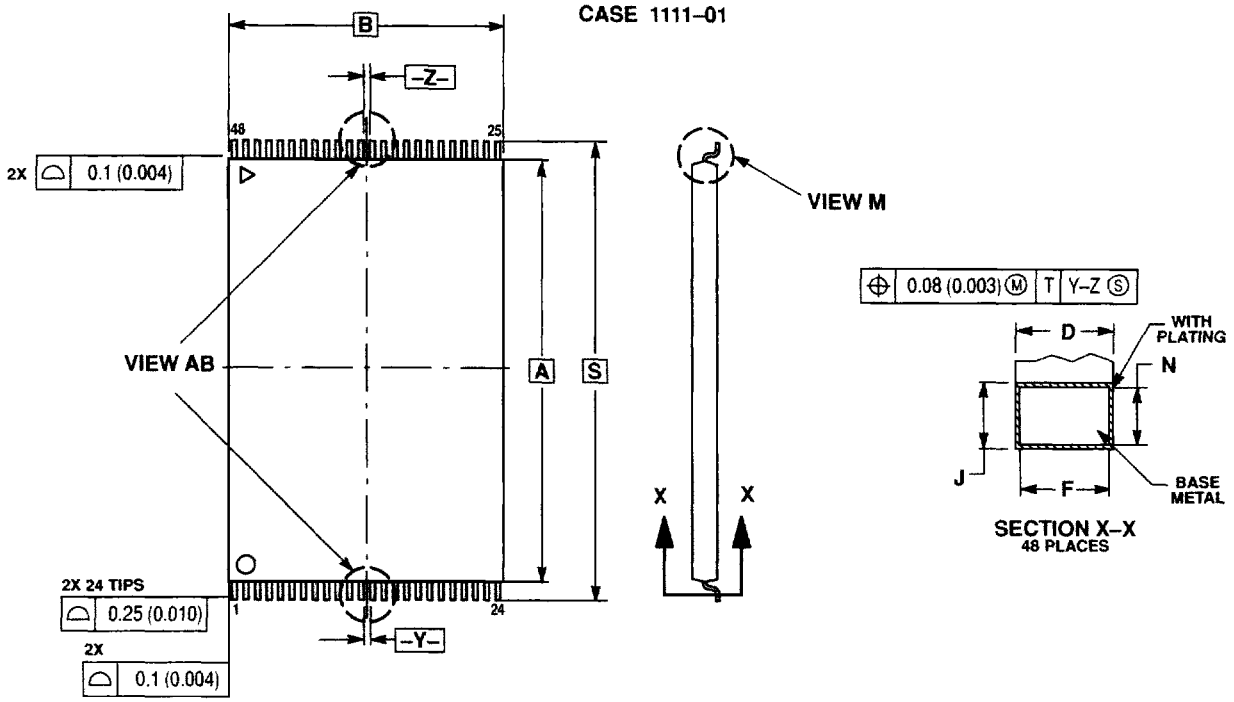
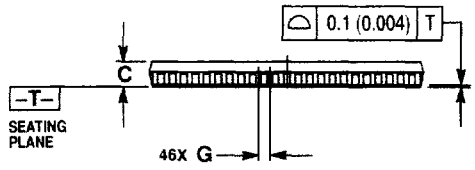
M29F800A2KBR80	M29F800A2KBR10	M29F800A2KBR12
M29F800A2KBT80R	M29F800A2KBT10R	M29F800A2KBT12R
M29F800A2KBR80R	M29F800A2KBR10R	M29F800A2KBR12
M29F800A2UT80	M29F800A2UT10	M29F800A2UT12
M29F800A2UR80	M29F800A2UR10	M29F800A2UR12
M29F800A2UT80R	M29F800A2UT10R	M29F800A2UT12R
M29F800A2UR80R	M29F800A2UR10R	M29F800A2UR12R
M29F800A2BT80	M29F800A2BT10	M29F800A2BT12
M29F800A2BR80	M29F800A2BR10	M29F800A2BR12
M29F800A2BT80R	M29F800A2BT10R	M29F800A2BT12R
M29F800A2BR80R	M29F800A2BR10R	M29F800A2BR12R

PACKAGE DIMENSIONS

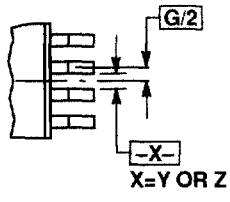
T PACKAGE
48–PIN TSOP
CASE 1111–01



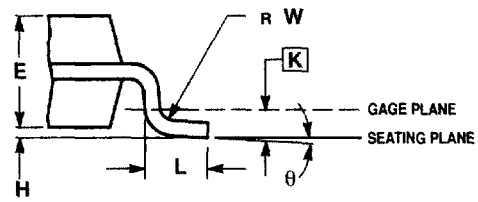


NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.40 BSC		0.724 BSC	
B	12.00 BSC		0.472 BSC	
C	—	1.20	—	0.047
D	0.17	0.27	0.007	0.011
E	0.95	1.05	0.037	0.041
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	0.25 BSC		0.010 BSC	
L	0.50	0.70	0.020	0.028
N	0.10	0.16	0.004	0.006
S	20.00 BSC		0.787 BSC	
W	0.08	0.20	0.003	0.008
θ	0°	5°	0°	5°

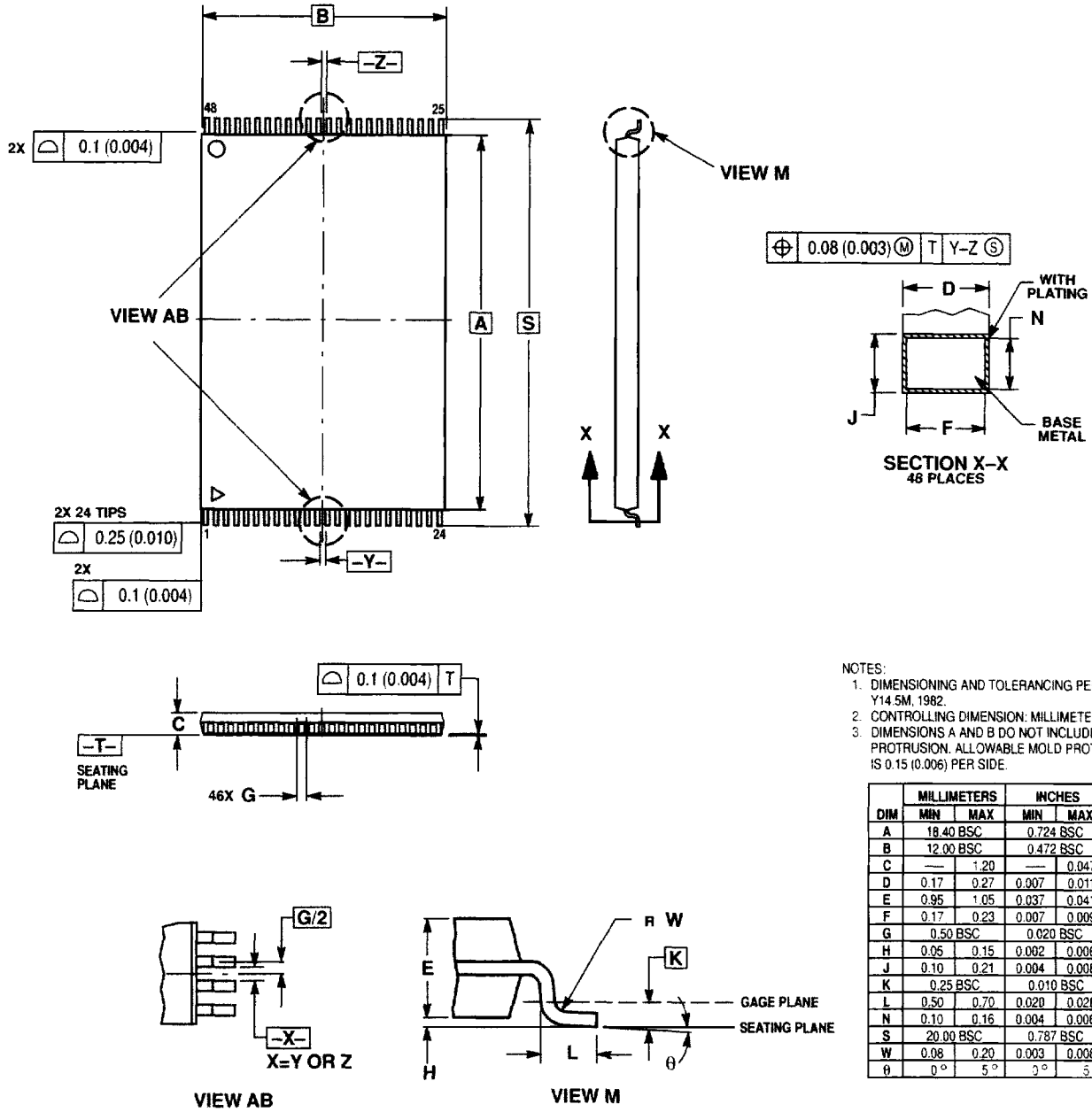


VIEW AB



VIEW M

R PACKAGE
48–PIN REVERSE TSOP
CASE 1111A–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.40 BSC		0.724 BSC	
B	12.00 BSC		0.472 BSC	
C	—	1.20	—	0.047
D	0.17	0.27	0.007	0.011
E	0.95	1.05	0.037	0.041
F	0.17	0.23	0.007	0.009
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	0.25 BSC		0.010 BSC	
L	0.50	0.70	0.020	0.028
N	0.10	0.16	0.004	0.006
S	20.00 BSC		0.787 BSC	
W	0.08	0.20	0.003	0.008
θ	0°	5°	0°	5°

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