M16C/62 Group (M16C/62P)

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0001-0110Z
Rev.1.10
2003.05.28

Overview

The M16C/62 group (M16C/62P) of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 100-pin and 128-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

Applications

Audio, cameras, office/communications/portable/industrial equipment, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

Performance Outline

Table 1.1.1 lists performance outline of M16C/62P group.

Table 1.1.1. Performance outline of M16C/62P group

Item		Performance	
Number of basic instructions		91 instructions	
Shortest instruction execution time		41.7 ns (f(BCLK)= 24MHz, V_{CC1}= 3.0V to 5.5V) 100 ns (f(BCLK)= 10MHz, V_{CC1}= 2.7V to 5.5V)	
Memory capacity	ROM	(See the product list)	
	RAM	(See the product list)	
I/O port	100-pin version P0 to P10 (except P8$_5$)	8 bits x 10, 7 bits x 1	P0 to P5: V_{CC2} ports P6 to P10: V_{CC1} ports
	128-pin version P0 to P14 (except P8$_5$)	8 bits x 13, 7 bits x 1, 2 bits x 1	P0 to P5, P12, P13: V_{CC2} ports P6 to P10, P11, P14: V_{CC1} ports
Input port	P8$_5$	1 bit x 1 ($\overline{NMI}$ pin level judgment): V_{CC1} ports	
Multifunction timer			
	Output	16 bits x 5 channels (TA0, TA1, TA2, TA3, TA4)	
	Input	16 bits x 6 channels (TB0, TB1, TB2, TB3, TB4, TB5)	
Serial I/O		3 channels (UART0, UART1, UART2) UART, clock synchronous, I^{2}C bus[1] (option[4]), or IEBus[2] (option4) 2 channels (SI/O3, SI/O4) Clock synchronous	
A-D converter		10 bits x (8 x 3 + 2) channels	
D-A converter		8 bits x 2	
DMAC		2 channels (trigger: 25 sources)	
CRC calculation circuit		CRC-CCITT	
Watchdog timer		15 bits x 1 (with prescaler)	
Interrupt		29 internal and 8 external sources, 4 software sources, 7 levels	
Clock generation circuit		4 circuits • Main clock, • Sub-clock (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator) • Ring oscillator(main-clock oscillation stop detect function) • PLL frequency synthesizer	
Voltage detection circuit		Present (option[4])	
Power supply voltage		V_{CC1}=3.0V to 5.5V, V_{CC2}=3.0V to V_{CC1}(f(BCLK)=24MHz) V_{CC1}=V_{CC2}=2.7V to 5.5V (f(BCLK)=10MHz)	
Flash memory	Program/erase voltage	3.3V ± 0.3V or 5.0V ± 0.5V	
	Number of program/erase	100 times, 10000 times[3] (option[4])	
Power consumption		14mA (V_{CC1}=V_{CC2}=5V, f(BCLK)=24MHz) 8mA (V_{CC1}=V_{CC2}=3V, f(BCLK)=10MHz) 1.8µA (V_{CC1}=V_{CC2}=3V, f(X_{CIN})=32kHz, when wait mode)	
I/O characteristics	I/O withstand voltage	5.0V	
	Output current	5mA	
Memory expansion		Available (to 4M bytes)	
Operating ambient temperature		-20 to 85°C -40 to 85°C (option[4])	
Device configuration		CMOS high performance silicon gate	
Package		100-pin and 128-pin plastic mold QFP	

Notes:

1. I^{2}C bus is a registered trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a registered trademark of NEC Electronics Corporation.
3. Block 1 and block A are a 10,000 times of programming and erasure. All other blocks are guaranteed of 1,000 times of programming and erasure. (Under development; mass production scheduled to start in the 3rd quarter of 2003)
4. If you desire this option, please so specify.

Block Diagram

Figure 1.1.1 is a block diagram of the M16C/62P group.

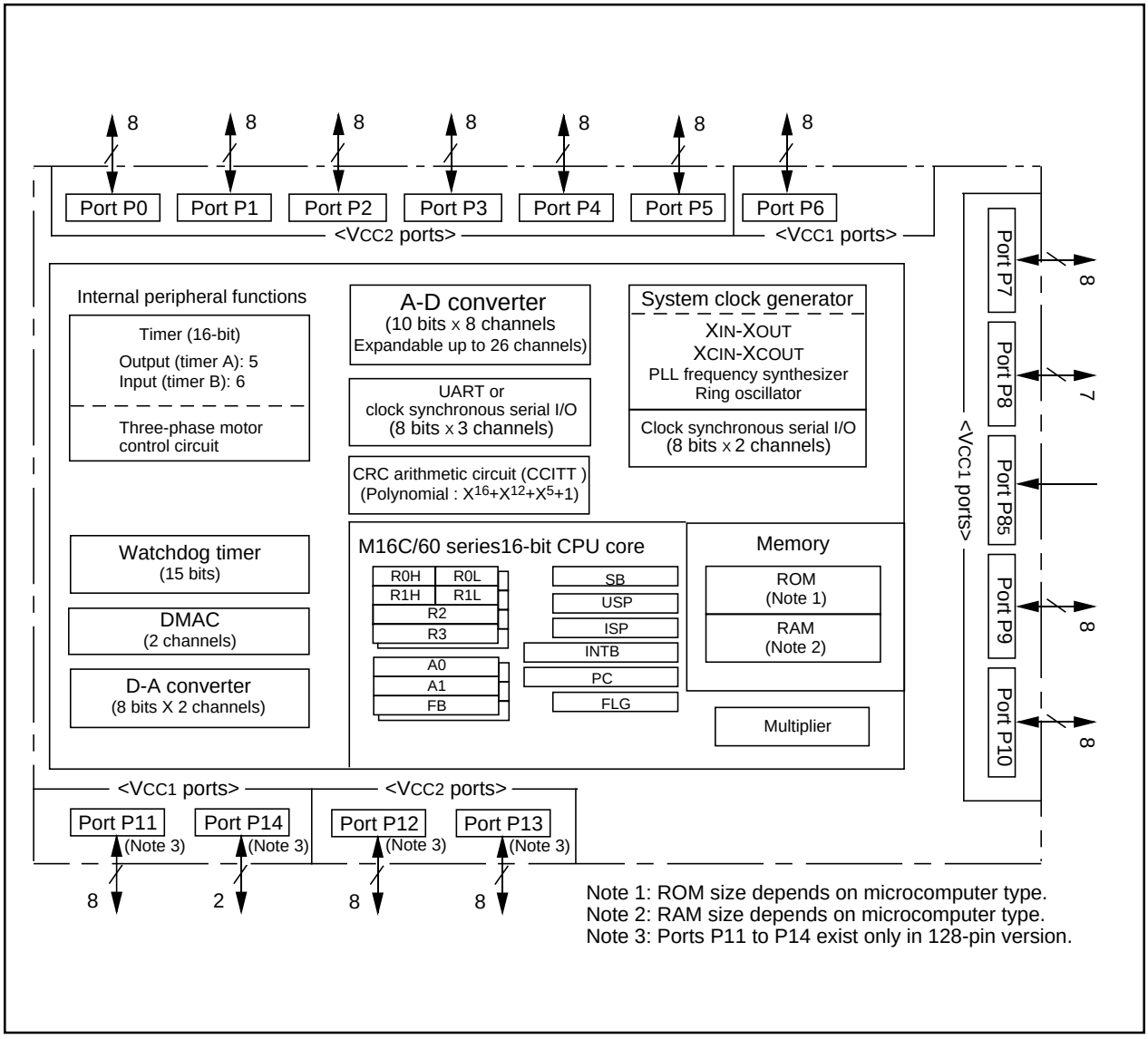


Figure 1.1.1. Block Diagram

Product List

Tables 1.1.2 and 1.1.3 list the M16C/62P group products and Figure 1.1.2 shows the type numbers, memory sizes and packages.

Table 1.1.2. Product List (1)

As of April 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30622M6P-XXXFP ★	48K bytes	4K bytes	100P6S-A	MASK ROM version
M30622M6P-XXXGP ★			100P6Q-A	
M30622M8P-XXXFP ★	64K bytes	4K bytes	100P6S-A	
M30622M8P-XXXGP ★			100P6Q-A	
M30622MAP-XXXFP ★	96K bytes	5K bytes	100P6S-A	
M30622MAP-XXXGP ★			100P6Q-A	
M30620MCP-XXXFP ★	128K bytes	10K bytes	100P6S-A	
M30620MCP-XXXGP ★			100P6Q-A	
M30622MEP-XXXFP ★	192K bytes	12K bytes	100P6S-A	
M30622MEP-XXXGP ★			100P6Q-A	
M30623MEP-XXXGP ★			128P6Q-A	
M30622MGP-XXXFP ★	256K bytes	12K bytes	100P6S-A	
M30622MGP-XXXGP ★			100P6Q-A	
M30623MGP-XXXGP ★			128P6Q-A	
M30624MGP-XXXFP ★		20K bytes	100P6S-A	
M30624MGP-XXXGP ★			100P6Q-A	
M30625MGP-XXXGP ★			128P6Q-A	
M30622MWP-XXXFP ★	320K bytes	16K bytes	100P6S-A	
M30622MWP-XXXGP ★			100P6Q-A	
M30623MWP-XXXGP ★			128P6Q-A	
M30624MWP-XXXFP		24K bytes	100P6S-A	
M30624MWP-XXXGP			100P6Q-A	
M30625MWP-XXXGP ★			128P6Q-A	
M30626MWP-XXXFP ★		31K bytes	100P6S-A	
M30626MWP-XXXGP ★			100P6Q-A	
M30627MWP-XXXGP ★			128P6Q-A	
M30622MHP-XXXFP ★	384K bytes	16K bytes	100P6S-A	
M30622MHP-XXXGP ★			100P6Q-A	
M30623MHP-XXXGP ★			128P6Q-A	
M30624MHP-XXXFP ★		24K bytes	100P6S-A	
M30624MHP-XXXGP			100P6Q-A	
M30625MHP-XXXGP ★			128P6Q-A	
M30626MHP-XXXFP		31K bytes	100P6S-A	
M30626MHP-XXXGP			100P6Q-A	
M30627MHP-XXXGP ★			128P6Q-A	

★ : Under development
★★ : Under planning

Table 1.1.3. Product List (2)

As of April 2003

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30622F8PFP ★	64K bytes	4K bytes	100P6S-A	Flash memory version
M30622F8PGP ★			100P6Q-A	
M30620FCPFP ★	128K bytes	10K bytes	100P6S-A	
M30620FCPGP ★			100P6Q-A	
M30624FGPFP	256K bytes	20K bytes	100P6S-A	
M30624FGPGP			100P6Q-A	
M30625FGPGP ★			128P6Q-A	
M30626FHPFP	384K bytes	31K bytes	100P6S-A	
M30626FHPGP			100P6Q-A	
M30627FHPGP			128P6Q-A	
M30626FJPFP ★★	512K bytes	31K bytes	100P6S-A	
M30626FJPGP ★★			100P6Q-A	
M30627FJPGP ★★			128P6Q-A	
M30620SPFP ★	—	10K bytes	100P6S-A	External ROM version
M30620SPGP ★			100P6Q-A	
M30622SPFP ★		4K bytes	100P6S-A	
M30622SPGP ★			100P6Q-A	

★ : Under development
★★ : Under planning

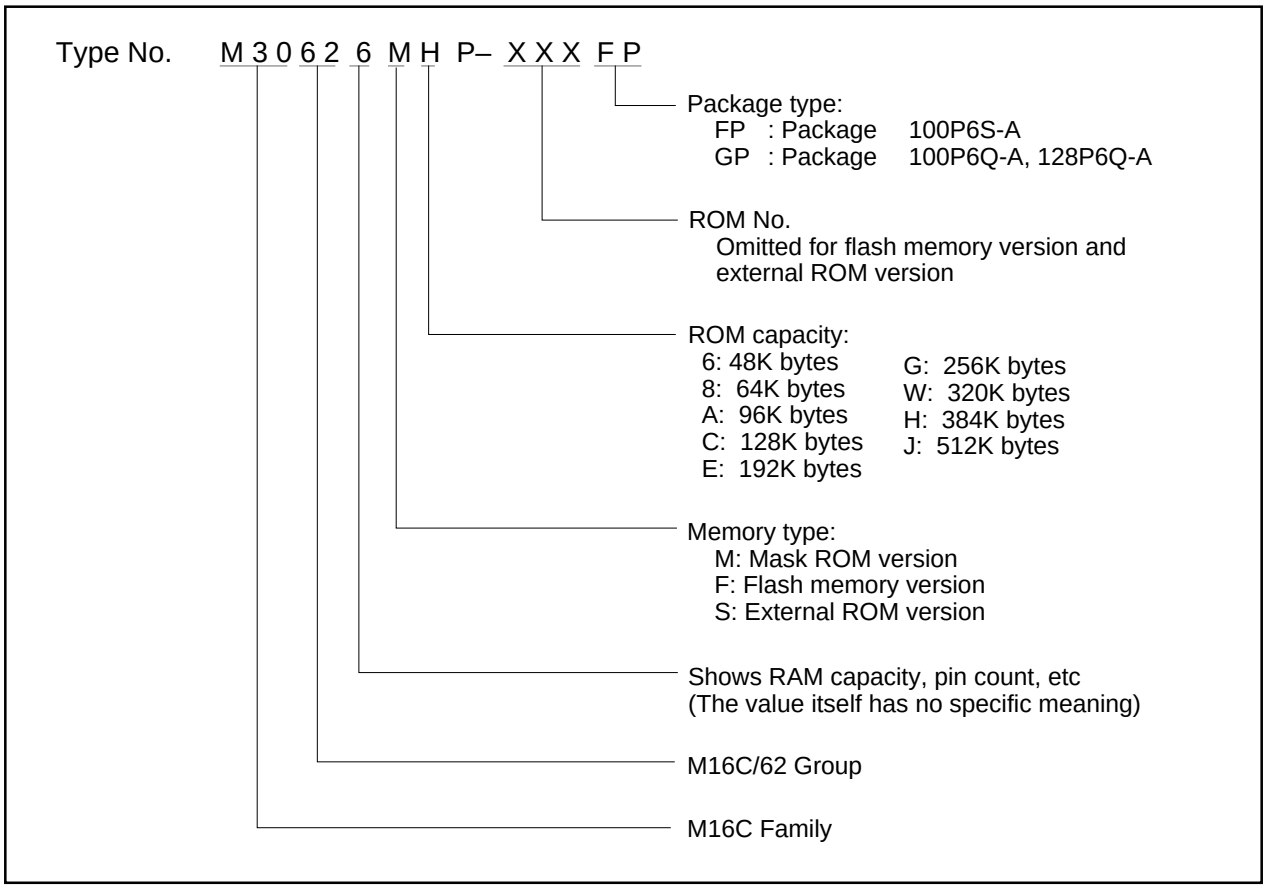


Figure 1.1.2. Type No., Memory Size, and Package

Pin Configuration

Figures 1.1.3 to 1.1.5 show the pin configurations (top view).

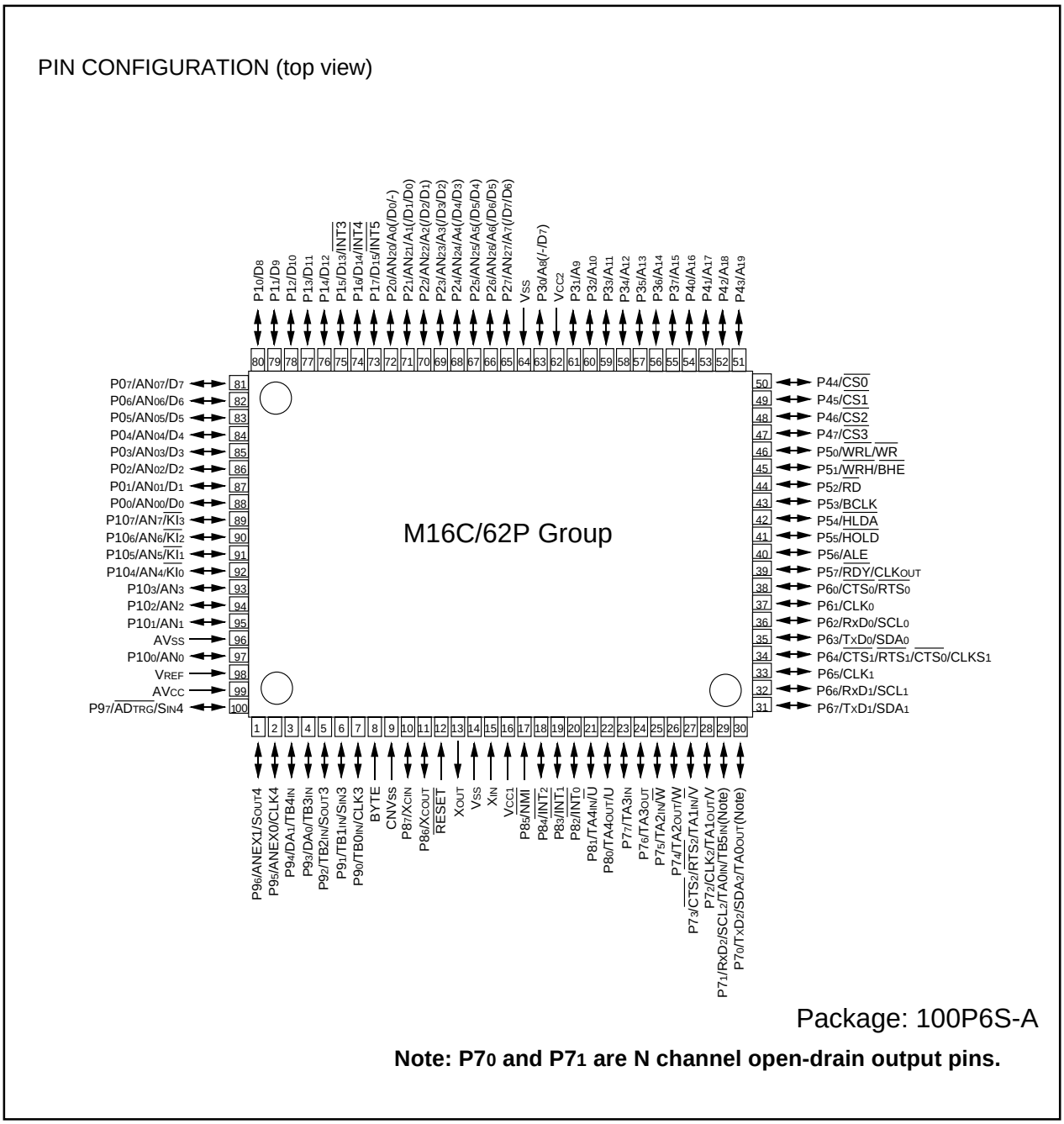
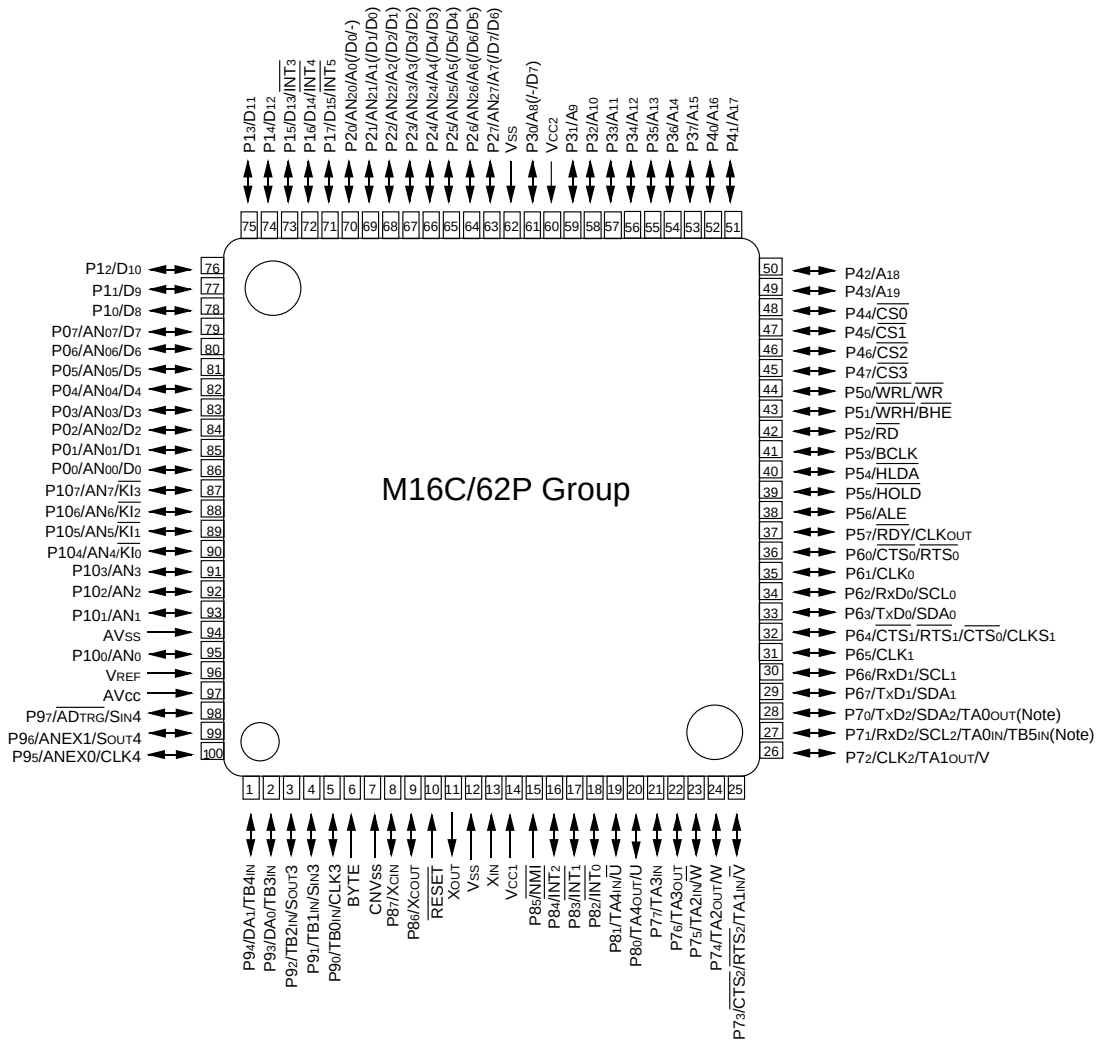


Figure 1.1.3. Pin Configuration (Top View)

PIN CONFIGURATION (top view)

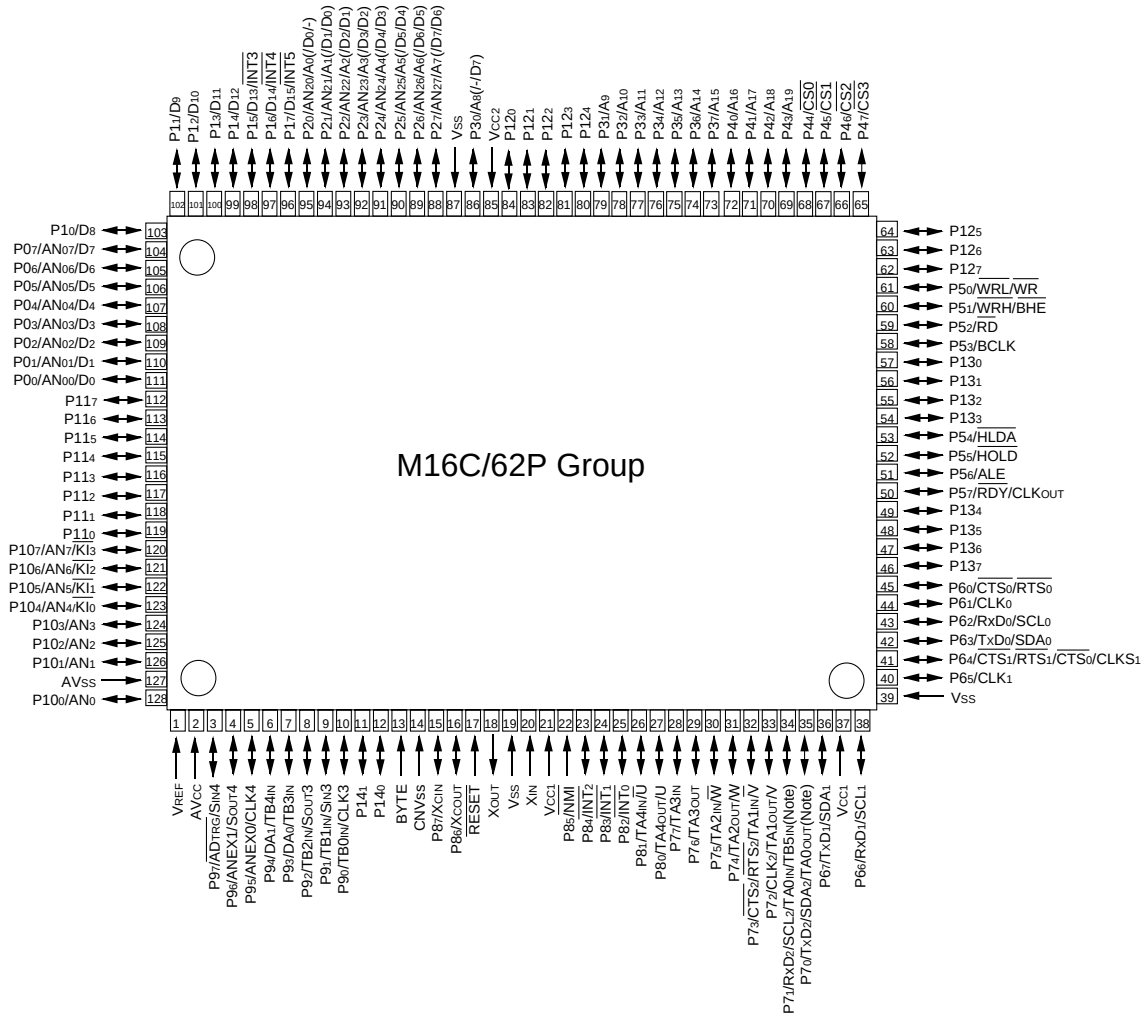


Package: 100P6Q-A

Note: P70 and P71 are N channel open-drain output pins.

Figure 1.1.4. Pin Configuration (Top View)

PIN CONFIGURATION (top view)



Package: 128P6Q-A

Note: P7₀ and P7₁ are N channel open-drain output pins.

Figure 1.1.5. Pin Configuration (Top View)

Table 1.1.4 Pin Description (100-pin and 128-pin Packages)

Pin name	Signal name	I/O type	Power supply	Function
V_{CC1}, V_{CC2}, V_{SS}	Power supply input		—	Apply 2.7V to 5.5 V to the V_{CC1} and V_{CC2} pins and 0 V to the V_{SS} pin. The Vcc apply condition is that $V_{CC2} \leq V_{CC1}$ (Note)
CNV_{SS}	CNV_{SS}	Input	V_{CC1}	This pin switches between processor modes. Connect this pin to V_{SS} pin when after a reset you want to start operation in single-chip mode (memory expansion mode) or the V_{CC1} pin when starting operation in microprocessor mode.
$\overline{RESET}$	Reset input	Input	V_{CC1}	"L" on this input resets the microcomputer.
X_{IN}	Clock input	Input	V_{CC1}	These pins are provided for the main clock generating circuit input/ output. Connect a ceramic resonator or crystal between the X_{IN} and the X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
X_{OUT}	Clock output	Output		
BYTE	External data bus width select input	Input		This pin selects the width of an external data bus. A 16-bit width is selected when this input is "L"; an 8-bit width is selected when this input is "H". This input must be fixed to either "H" or "L". Connect this pin to the V_{SS} pin when operating in single-chip mode.
AV_{CC}	Analog power supply input			This pin is a power supply input for the A-D converter. Connect this pin to V_{CC1}.
AV_{SS}	Analog power supply input			This pin is a power supply input for the A-D converter. Connect this pin to V_{SS}.
V_{REF}	Reference voltage input	Input		This pin is a reference voltage input for the A-D converter.
$P0_0$ to $P0_7$	I/O port P0	Input/output	V_{CC2}	This is an 8-bit CMOS I/O port. This port has an input/output select direction register, allowing each pin in that port to be directed for input or output individually. If any port is set for input, selection can be made for it in a program whether or not to have a pull-up resistor in 4 bit units. This selection is unavailable in memory extension and microprocessor modes. This port can function as input pins for the A-D converter when so selected in a program.
D_0 to D_7		Input/output		When set as a separate bus, these pins input and output data (D_0 –D_7).
$P1_0$ to $P1_7$	I/O port P1	Input/output	V_{CC2}	This is an 8-bit I/O port equivalent to P0. $P1_5$ to $P1_7$ also function as $\overline{INT}$ interrupt input pins as selected by a program.
D_8 to D_{15}		Input/output		When set as a separate bus, these pins input and output data (D_8 –D_{15}).
$P2_0$ to $P2_7$	I/O port P2	Input/output	V_{CC2}	This is an 8-bit I/O port equivalent to P0. This port can function as input pins for the A-D converter when so selected in a program.
A_0 to A_7		Output		These pins output 8 low-order address bits (A_0 to A_7).
A_0/D_0 to A_7/D_7		Input/output		If the external bus is set as an 8-bit wide multiplexed bus, these pins input and output data (D_0 to D_7) and output 8 low-order address bits (A_0 to A_7) separated in time by multiplexing.
A_0 A_1/D_0 to A_7/D_6		Output Input/output		If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D_0 to D_6) and output address (A_1 to A_7) separated in time by multiplexing. They also output address (A_0).
$P3_0$ to $P3_7$	I/O port P3	Input/output	V_{CC2}	This is an 8-bit I/O port equivalent to P0.
A_8 to A_{15}		Output		These pins output 8 middle-order address bits (A_8 to A_{15}).
A_8/D_7, A_9 to A_{15}		Input/output Output		If the external bus is set as a 16-bit wide multiplexed bus, these pins input and output data (D_7) and output address (A_8) separated in time by multiplexing. They also output address (A_9 to A_{15}).
$P4_0$ to $P4_7$	I/O port P4	Input/output	V_{CC2}	This is an 8-bit I/O port equivalent to P0.
$\overline{A_{16}}$ to $\overline{A_{19}}$, $\overline{CS_0}$ to $\overline{CS_3}$		Output Output		These pins output A_{16} to A_{19} and $\overline{CS_0}$ to $\overline{CS_3}$ signals. A_{16} to A_{19} are 4 high- order address bits. $\overline{CS_0}$ to $\overline{CS_3}$ are chip select signals used to specify an access space.

Note: In this manual, hereafter, V_{CC} refers to V_{CC1} unless otherwise noted.

Table 1.1.5 Pin Description (100-pin and 128-pin Packages) (Continued)

Pin name	Signal name	I/O type	Power supply	Function
P5$_0$ to P5$_7$	I/O port P5	Input/output	V_{CC2}	This is an 8-bit I/O port equivalent to P0. In single-chip mode, P5$_7$ in this port outputs a divide-by-8 or divide-by-32 clock of X_{IN} or a clock of the same frequency as X_{CIN} as selected by program.
$\overline{WRL}$ / $\overline{WR}$, $\overline{WRH}$ / $\overline{BHE}$, $\overline{RD}$, BCLK, $\overline{HLDA}$, HOLD, ALE, RDY		Output Output Output Output Output Input Output Input		Output $\overline{WRL}$/$\overline{WR}$, $\overline{WRH}$/$\overline{BHE}$, $\overline{RD}$, BCLK, $\overline{HLDA}$, and ALE signals. $\overline{WRL}$/$\overline{WR}$ and $\overline{WRH}$/$\overline{BHE}$ are switchable in a program. Note that $\overline{WRL}$ and $\overline{WRH}$ are always used as a pair, so as $\overline{WR}$ and $\overline{BHE}$. ■ $\overline{WRL}$, $\overline{WRH}$, and $\overline{RD}$ selected If the external data bus is 16 bits wide, data are written to even addresses when the $\overline{WRL}$ signal is low, and written to odd addresses when the $\overline{WRH}$ signal is low. Data are read out when the $\overline{RD}$ signal is low. ■ $\overline{WR}$, $\overline{BHE}$, and $\overline{RD}$ selected Data are written when the $\overline{WR}$ signal is low, or read out when the $\overline{RD}$ signal is low. Odd addresses are accessed when the $\overline{BHE}$ signal is low. Use this mode when the external data bus is 8 bits wide. The microcomputer goes to a hold state when input to the $\overline{HOLD}$ pin is held low. While in the hold state, $\overline{HLDA}$ outputs a low level. ALE is used to latch the address. While the input level of the $\overline{RDY}$ pin is low, the bus of the microcomputer goes to a wait state.
P6$_0$ to P6$_7$	I/O port P6	Input/output	V_{CC1}	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as UART0 and UART1 I/O pins as selected by program.
P7$_0$ to P7$_7$	I/O port P7	Input/output	V_{CC1}	This is an 8-bit I/O port equivalent to P0 (P7$_0$ and P7$_1$ are N channel open-drain output). This port can function as input/output pins for timers A0 to A3 when so selected in a program. Furthermore, P7$_0$ to P7$_5$, P7$_1$, and P7$_2$ to P7$_5$ can also function as input/output pins for UART2, an input pin for timer B5, and output pins for the three-phase motor control timer, respectively.
P8$_0$ to P8$_4$, P8$_6$, P8$_7$, P8$_5$	I/O port P8 I/O port P8$_5$	Input/output Input/output Input/output Input	V_{CC1}	P8$_0$ to P8$_4$, P8$_6$, and P8$_7$ are I/O ports with the same functions as P0. When so selected in a program, P8$_0$ to P8$_1$ and P8$_2$ to P8$_4$ can function as input/output pins for timer A4 or output pins for the three-phase motor control timer and $\overline{INT}$ interrupt input pins, respectively. P8$_6$ and P8$_7$, when so selected in a program, both can function as input/output pins for the subclock oscillator circuit. In that case, connect a crystal resonator between P8$_6$ (X_{COUT} pin) and P8$_7$ (X_{CIN} pin). P8$_5$ is an input-only port shared with $\overline{NMI}$. An $\overline{NMI}$ interrupt request is generated when input on this pin changes state from high to low. The $\overline{NMI}$ function cannot be disabled in a program. A pull-up cannot be set for this pin.
P9$_0$ to P9$_7$	I/O port P9	Input/output	V_{CC1}	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as SI/O3 and SI/O4 I/O pins, Timer B0 to B4 input pins, D-A converter output pins, A-D converter input pins, or A-D trigger input pins as selected by program.
P10$_0$ to P10$_7$	I/O port P10	Input/output	V_{CC1}	This is an 8-bit I/O port equivalent to P0. Pins in this port also function as A-D converter input pins as selected by program. Furthermore, P10$_4$ to P10$_7$ also function as input pins for the key input interrupt function.

Table 1.1.6 Pin Description (128-pin Package)

Pin name	Signal name	I/O type	Power supply circuit block	Function
P11$_0$ to P11$_7$	I/O port P11	Input/output	V_{CC1}	This is an 8-bit I/O port equivalent to P0.
P12$_0$ to P12$_7$	I/O port P12	Input/output	V_{CC2}	This is an 8-bit I/O port equivalent to P0.
P13$_0$ to P13$_7$	I/O port P13	Input/output	V_{CC2}	This is an 8-bit I/O port equivalent to P0.
P14$_0$, P14$_1$	I/O port P14	Input/output	V_{CC1}	This is an 2-bit I/O port equivalent to P0.

Memory

Figure 1.2.1 is a memory map of the M16C/62P group. The address space extends the 1M bytes from address 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated in a lower address direction beginning with address $FFFFF_{16}$. For example, a 64-Kbyte internal ROM is allocated to the addresses from $F0000_{16}$ to $FFFFF_{16}$.

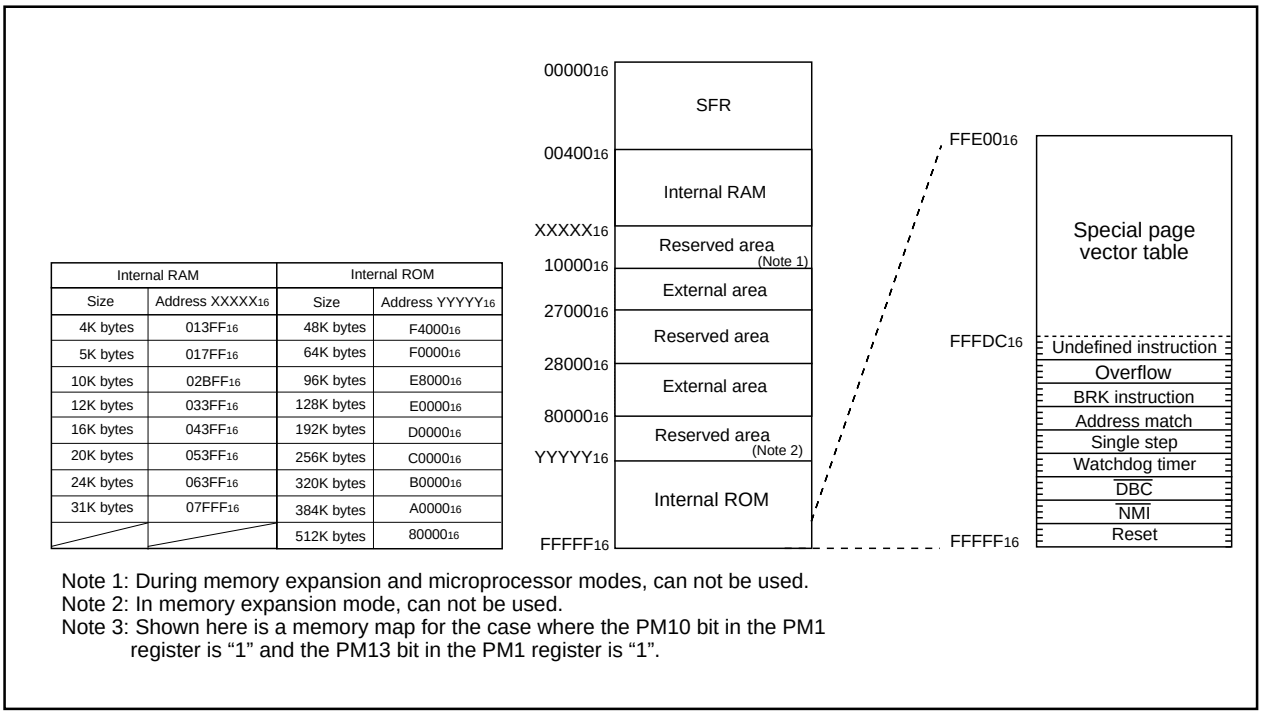
The fixed interrupt vector table is allocated to the addresses from $FFFDC_{16}$ to $FFFFF_{16}$. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400_{16}. For example, a 10-Kbytes internal RAM is allocated to the addresses from 00400_{16} to $02BFF_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SRF is allocated to the addresses from 00000_{16} to $003FF_{16}$. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from $FFE00_{16}$ to $FFFDB_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the “M16C/60 and M16C/20 Series Software Manual.”

In memory expansion and microprocessor modes, some areas are reserved for future use and cannot be used by users.



Internal RAM		Internal ROM	
Size	Address XXXXX$_{16}$	Size	Address YYYYY$_{16}$
4K bytes	013FF$_{16}$	48K bytes	F4000$_{16}$
5K bytes	017FF$_{16}$	64K bytes	F0000$_{16}$
10K bytes	02BFF$_{16}$	96K bytes	E8000$_{16}$
12K bytes	033FF$_{16}$	128K bytes	E0000$_{16}$
16K bytes	043FF$_{16}$	192K bytes	D0000$_{16}$
20K bytes	053FF$_{16}$	256K bytes	C0000$_{16}$
24K bytes	063FF$_{16}$	320K bytes	B0000$_{16}$
31K bytes	07FFF$_{16}$	384K bytes	A0000$_{16}$
		512K bytes	80000$_{16}$

Note 1: During memory expansion and microprocessor modes, can not be used.
Note 2: In memory expansion mode, can not be used.
Note 3: Shown here is a memory map for the case where the PM10 bit in the PM1 register is “1” and the PM13 bit in the PM1 register is “1”.

Figure 1.2.1. Memory Map

Central Processing Unit (CPU)

Figure 1.3.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

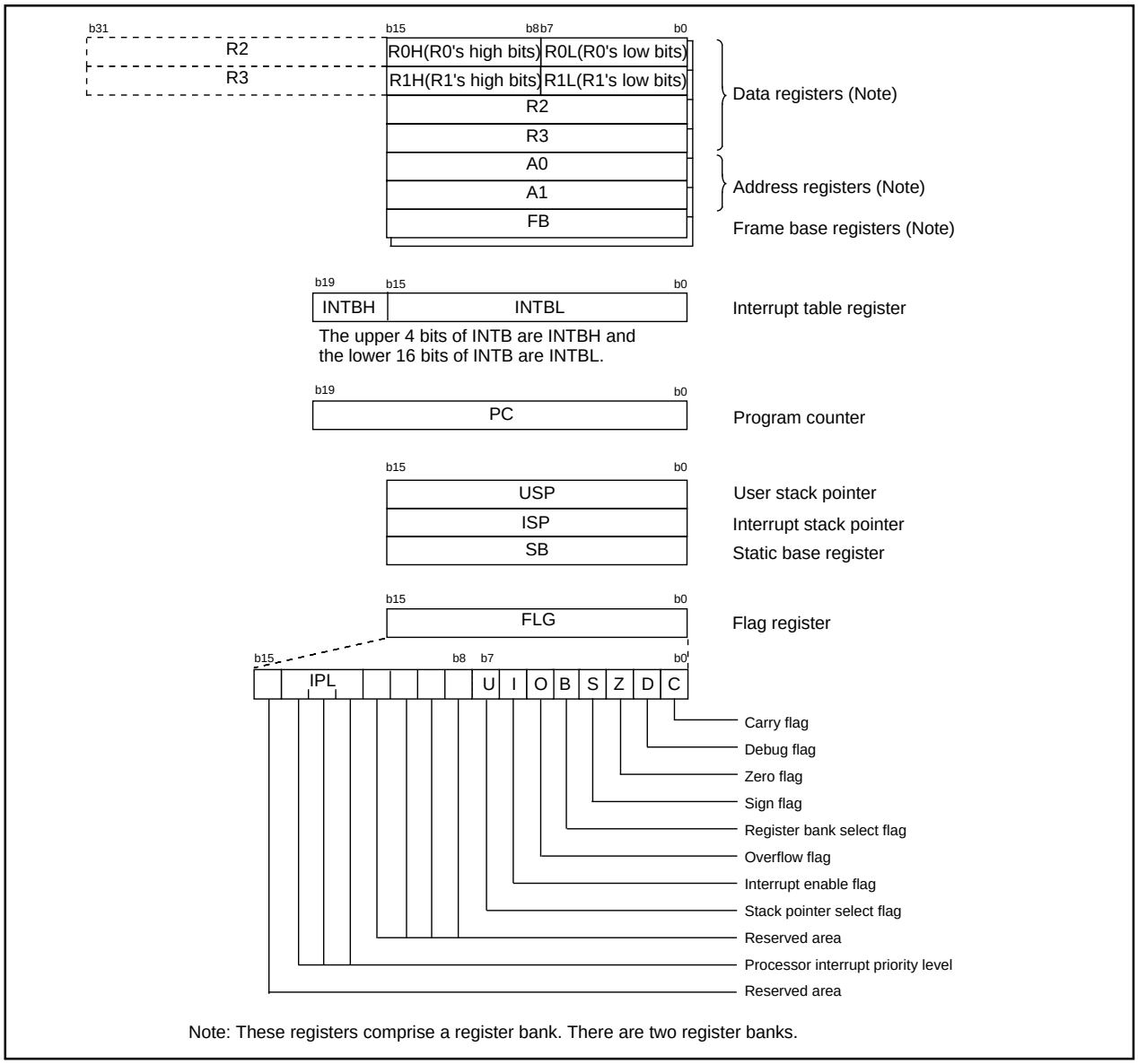


Figure 1.3.1. Central Processing Unit Register

(1) Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

(2) Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

(3) Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

(4) Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

(5) Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

(6) User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

(7) Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

(8) Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

- **Carry Flag (C Flag)**
  This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.
- **Debug Flag (D Flag)**
  The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.
- **Zero Flag (Z Flag)**
  This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.
- **Sign Flag (S Flag)**
  This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.
- **Register Bank Select Flag (B Flag)**
  Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.
- **Overflow Flag (O Flag)**
  This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.
- **Interrupt Enable Flag (I Flag)**
  This flag enables a maskable interrupt.
  Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.
- **Stack Pointer Select Flag (U Flag)**
  ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
  The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.
- **Processor Interrupt Priority Level (IPL)**
  IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
  If a requested interrupt has priority greater than IPL, the interrupt is enabled.
- **Reserved Area**
  When write to this bit, write "0". When read, its content is indeterminate.

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0 (Note 2)	PM0	00000000₂(CNVss pin is "L") 00000011₂(CNVss pin is "H")
0005₁₆	Processor mode register 1	PM1	00001000₂
0006₁₆	System clock control register 0	CM0	01001000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆	Chip select control register	CSR	00000001₂
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	XX000000₂
000B₁₆	Data bank register	DBR	00₁₆
000C₁₆	Oscillation stop detection register (Note 3)	CM2	0000X000₂
000D₁₆			
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00XXXXXX₂(Note 4)
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 (Note 5)	VCR1	00001000₂
001A₁₆	Voltage detection register 2 (Note 5)	VCR2	00₁₆
001B₁₆	Chip select expansion control register	CSE	00₁₆
001C₁₆	PLL control register 0	PLC0	0001X010₂
001D₁₆			
001E₁₆	Processor mode register 2	PM2	XXX00000₂
001F₁₆	Voltage down detection interrupt register	D4INT	00₁₆
0020₁₆	DMA0 source pointer	SAR0	XX₁₆
0021₁₆			XX₁₆
0022₁₆			XX₁₆
0023₁₆			
0024₁₆	DMA0 destination pointer	DAR0	XX₁₆
0025₁₆			XX₁₆
0026₁₆			XX₁₆
0027₁₆			
0028₁₆	DMA0 transfer counter	TCR0	XX₁₆
0029₁₆			XX₁₆
002A₁₆			
002B₁₆			
002C₁₆	DMA0 control register	DM0CON	00000X00₂
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆	DMA1 source pointer	SAR1	XX₁₆
0031₁₆			XX₁₆
0032₁₆			XX₁₆
0033₁₆			
0034₁₆	DMA1 destination pointer	DAR1	XX₁₆
0035₁₆			XX₁₆
0036₁₆			XX₁₆
0037₁₆			
0038₁₆	DMA1 transfer counter	TCR1	XX₁₆
0039₁₆			XX₁₆
003A₁₆			
003B₁₆			
003C₁₆	DMA1 control register	DM1CON	00000X00₂
003D₁₆			
003E₁₆			
003F₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
Note 3: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
Note 4: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program. It is set to "0" when the input voltag
at the V_{CC1} pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1" (RAM retention limit detection circuit enable
Note 5: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆	INT3 interrupt control register	INT3IC	XX00X000₂
0045₁₆	Timer B5 interrupt control register	TB5IC	XXXXX000₂
0046₁₆	Timer B4 interrupt control register, UART1 BUS collision detection interrupt control register	TB4IC, U1BCNIC	XXXXX000₂
0047₁₆	Timer B3 interrupt control register, UART0 BUS collision detection interrupt control register	TB3IC, U0BCNIC	XXXXX000₂
0048₁₆	SI/O4 interrupt control register (S4IC), INT5 interrupt control register	S4IC, INT5IC	XX00X000₂
0049₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXXX000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXXX000₂
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	A-D conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	Timer A0 interrupt control register	TA0IC	XXXXX000₂
0056₁₆	Timer A1 interrupt control register	TA1IC	XXXXX000₂
0057₁₆	Timer A2 interrupt control register	TA2IC	XXXXX000₂
0058₁₆	Timer A3 interrupt control register	TA3IC	XXXXX000₂
0059₁₆	Timer A4 interrupt control register	TA4IC	XXXXX000₂
005A₁₆	Timer B0 interrupt control register	TB0IC	XXXXX000₂
005B₁₆	Timer B1 interrupt control register	TB1IC	XXXXX000₂
005C₁₆	Timer B2 interrupt control register	TB2IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00X000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00X000₂
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

Note :The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0080₁₆			
0081₁₆			
0082₁₆			
0083₁₆			
0084₁₆			
0085₁₆			
0086₁₆			
≈			≈
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆			
01B4₁₆	Flash identification register (Note 2)	FIDR	XXXXXX00₂
01B5₁₆	Flash memory control register 1 (Note 2)	FMR1	0X00XX0X₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (Note 2)	FMR0	XX000001₂
01B8₁₆ 01B9₁₆ 01BA₁₆	Address match interrupt register 2	RMAD2	00₁₆ 00₁₆ X0₁₆
01BB₁₆	Address match interrupt enable register 2	AIER2	XXXXXX00₂
01BC₁₆ 01BD₁₆ 01BE₁₆	Address match interrupt register 3	RMAD3	00₁₆ 00₁₆ X0₁₆
01BF₁₆			
≈			≈
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆			
025B₁₆			
025C₁₆			
025D₁₆			
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆			
≈			≈
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆			
033F₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: This register is included in the flash memory version.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0340₁₆	Timer B3, 4, 5 count start flag	TBSR	000XXXXX₂
0341₁₆			
0342₁₆	Timer A1-1 register	TA11	XX₁₆
0343₁₆			XX₁₆
0344₁₆	Timer A2-1 register	TA21	XX₁₆
0345₁₆			XX₁₆
0346₁₆	Timer A4-1 register	TA41	XX₁₆
0347₁₆			XX₁₆
0348₁₆	Three-phase PWM control register 0	INVC0	00₁₆
0349₁₆	Three-phase PWM control register 1	INVC1	00₁₆
034A₁₆	Three-phase output buffer register 0	IDB0	00₁₆
034B₁₆	Three-phase output buffer register 1	IDB1	00₁₆
034C₁₆	Dead time timer	DTT	XX₁₆
034D₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX₁₆
034E₁₆			
034F₁₆			
0350₁₆	Timer B3 register	TB3	XX₁₆
0351₁₆			XX₁₆
0352₁₆	Timer B4 register	TB4	XX₁₆
0353₁₆			XX₁₆
0354₁₆	Timer B5 register	TB5	XX₁₆
0355₁₆			XX₁₆
0356₁₆			
0357₁₆			
0358₁₆			
0359₁₆			
035A₁₆			
035B₁₆	Timer B3 mode register	TB3MR	00XX0000₂
035C₁₆	Timer B4 mode register	TB4MR	00XX0000₂
035D₁₆	Timer B5 mode register	TB5MR	00XX0000₂
035E₁₆	Interrupt cause select register 2	IFSR2A	00XXXXXX₂
035F₁₆	Interrupt cause select register	IFSR	00₁₆
0360₁₆	SI/O3 transmit/receive register	S3TRR	XX₁₆
0361₁₆			
0362₁₆	SI/O3 control register	S3C	01000000₂
0363₁₆	SI/O3 bit rate generator	S3BRG	XX₁₆
0364₁₆	SI/O4 transmit/receive register	S4TRR	XX₁₆
0365₁₆			
0366₁₆	SI/O4 control register	S4C	01000000₂
0367₁₆	SI/O4 bit rate generator	S4BRG	XX₁₆
0368₁₆			
0369₁₆			
036A₁₆			
036B₁₆			
036C₁₆	UART0 special mode register 4	U0SMR4	00₁₆
036D₁₆	UART0 special mode register 3	U0SMR3	000X0X0X₂
036E₁₆	UART0 special mode register 2	U0SMR2	X0000000₂
036F₁₆	UART0 special mode register	U0SMR	X0000000₂
0370₁₆	UART1 special mode register 4	U1SMR4	00₁₆
0371₁₆	UART1 special mode register 3	U1SMR3	000X0X0X₂
0372₁₆	UART1 special mode register 2	U1SMR2	X0000000₂
0373₁₆	UART1 special mode register	U1SMR	X0000000₂
0374₁₆	UART2 special mode register 4	U2SMR4	00₁₆
0375₁₆	UART2 special mode register 3	U2SMR3	000X0X0X₂
0376₁₆	UART2 special mode register 2	U2SMR2	X0000000₂
0377₁₆	UART2 special mode register	U2SMR	X0000000₂
0378₁₆	UART2 transmit/receive mode register	U2MR	00₁₆
0379₁₆	UART2 bit rate generator	U2BRG	XX₁₆
037A₁₆	UART2 transmit buffer register	U2TB	XXXXXXXX₂
037B₁₆			XXXXXXXX₂
037C₁₆	UART2 transmit/receive control register 0	U2C0	00001000₂
037D₁₆	UART2 transmit/receive control register 1	U2C1	00000010₂
037E₁₆	UART2 receive buffer register	U2RB	XXXXXXXX₂
037F₁₆			XXXXXXXX₂

Note : The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0380₁₆	Count start flag	TABSR	00₁₆
0381₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX₂
0382₁₆	One-shot start flag	ONSF	00₁₆
0383₁₆	Trigger select register	TRGSR	00₁₆
0384₁₆	Up-down flag	UDF	00₁₆
0385₁₆			
0386₁₆ 0387₁₆	Timer A0 register	TA0	XX₁₆ XX₁₆
0388₁₆ 0389₁₆	Timer A1 register	TA1	XX₁₆ XX₁₆
038A₁₆ 038B₁₆	Timer A2 register	TA2	XX₁₆ XX₁₆
038C₁₆ 038D₁₆	Timer A3 register	TA3	XX₁₆ XX₁₆
038E₁₆ 038F₁₆	Timer A4 register	TA4	XX₁₆ XX₁₆
0390₁₆ 0391₁₆	Timer B0 register	TB0	XX₁₆ XX₁₆
0392₁₆ 0393₁₆	Timer B1 register	TB1	XX₁₆ XX₁₆
0394₁₆ 0395₁₆	Timer B2 register	TB2	XX₁₆ XX₁₆
0396₁₆	Timer A0 mode register	TA0MR	00₁₆
0397₁₆	Timer A1 mode register	TA1MR	00₁₆
0398₁₆	Timer A2 mode register	TA2MR	00₁₆
0399₁₆	Timer A3 mode register	TA3MR	00₁₆
039A₁₆	Timer A4 mode register	TA4MR	00₁₆
039B₁₆	Timer B0 mode register	TB0MR	00XX0000₂
039C₁₆	Timer B1 mode register	TB1MR	00XX0000₂
039D₁₆	Timer B2 mode register	TB2MR	00XX0000₂
039E₁₆	Timer B2 special mode register	TB2SC	XXXXXX00₂
039F₁₆			
03A0₁₆	UART0 transmit/receive mode register	U0MR	00₁₆
03A1₁₆	UART0 bit rate generator	U0BRG	XX₁₆
03A2₁₆ 03A3₁₆	UART0 transmit buffer register	U0TB	XXXXXXXX₂ XXXXXXXX₂
03A4₁₆	UART0 transmit/receive control register 0	U0C0	00001000₂
03A5₁₆	UART0 transmit/receive control register 1	U0C1	00000010₂
03A6₁₆ 03A7₁₆	UART0 receive buffer register	U0RB	XXXXXXXX₂ XXXXXXXX₂
03A8₁₆	UART1 transmit/receive mode register	U1MR	00₁₆
03A9₁₆	UART1 bit rate generator	U1BRG	XX₁₆
03AA₁₆ 03AB₁₆	UART1 transmit buffer register	U1TB	XXXXXXXX₂ XXXXXXXX₂
03AC₁₆	UART1 transmit/receive control register 0	U1C0	00001000₂
03AD₁₆	UART1 transmit/receive control register 1	U1C1	00000010₂
03AE₁₆ 03AF₁₆	UART1 receive buffer register	U1RB	XXXXXXXX₂ XXXXXXXX₂
03B0₁₆	UART transmit/receive control register 2	UCON	X0000000₂
03B1₁₆			
03B2₁₆			
03B3₁₆			
03B4₁₆			
03B5₁₆			
03B6₁₆			
03B7₁₆			
03B8₁₆	DMA0 request cause select register	DM0SL	00₁₆
03B9₁₆			
03BA₁₆	DMA1 request cause select register	DM1SL	00₁₆
03BB₁₆			
03BC₁₆ 03BD₁₆	CRC data register	CRCD	XX₁₆ XX₁₆
03BE₁₆	CRC input register	CRCIN	XX₁₆
03BF₁₆			

Note : The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
03C0₁₆ 03C1₁₆	A-D register 0	AD0	XXXXXXXX₂ XXXXXXXX₂
03C2₁₆ 03C3₁₆	A-D register 1	AD1	XXXXXXXX₂ XXXXXXXX₂
03C4₁₆ 03C5₁₆	A-D register 2	AD2	XXXXXXXX₂ XXXXXXXX₂
03C6₁₆ 03C7₁₆	A-D register 3	AD3	XXXXXXXX₂ XXXXXXXX₂
03C8₁₆ 03C9₁₆	A-D register 4	AD4	XXXXXXXX₂ XXXXXXXX₂
03CA₁₆ 03CB₁₆	A-D register 5	AD5	XXXXXXXX₂ XXXXXXXX₂
03CC₁₆ 03CD₁₆	A-D register 6	AD6	XXXXXXXX₂ XXXXXXXX₂
03CE₁₆ 03CF₁₆	A-D register 7	AD7	XXXXXXXX₂ XXXXXXXX₂
03D0₁₆			
03D1₁₆			
03D2₁₆			
03D3₁₆			
03D4₁₆	A-D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A-D control register 0	ADCON0	00000XXX₂
03D7₁₆	A-D control register 1	ADCON1	00₁₆
03D8₁₆	D-A register 0	DA0	XX₁₆
03D9₁₆			
03DA₁₆	D-A register 1	DA1	XX₁₆
03DB₁₆			
03DC₁₆	D-A control register	DACON	00₁₆
03DD₁₆			
03DE₁₆	Port P14 control register	PC14	XX00XXXX₂
03DF₁₆	Pull-up control register 3	PUR3	00₁₆
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆	Port P4 register	P4	XX₁₆
03E9₁₆	Port P5 register	P5	XX₁₆
03EA₁₆	Port P4 direction register	PD4	00₁₆
03EB₁₆	Port P5 direction register	PD5	00₁₆
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00X000002
03F3₁₆	Port P9 direction register	PD9	00₁₆
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆	Port P11 register	P11	XX₁₆
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆	Port P11 direction register	PD11	00₁₆
03F8₁₆	Port P12 register	P12	XX₁₆
03F9₁₆	Port P13 register	P13	XX₁₆
03FA₁₆	Port P12 direction register	PD12	00₁₆
03FB₁₆	Port P13 direction register	PD13	00₁₆
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00000000₂ (Note 2) 00000010₂
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: At hardware reset 1 or hardware reset 2, the register is as follows:
- "00000000₂" where "L" is inputted to the CNVss pin
- "00000010₂" where "H" is inputted to the CNVss pin

At software reset, watchdog timer reset and oscillation stop detection reset, the register is as follows:
- "00000000₂" where the PM01 to PM00 bits in the PM0 register are "00₂" (single-chip mode)
- "00000010₂" where the PM01 to PM00 bits in the PM0 register are "01₂" (memory expansion mode) or "11₂" (microprocessor mode)

X : Nothing is mapped to this bit

Electrical Characteristics

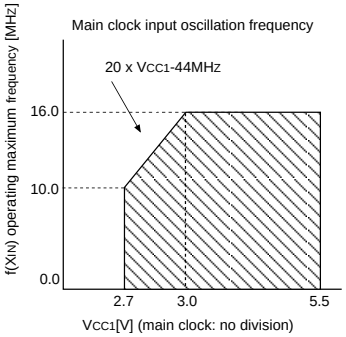
Table 1.5.1. Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated value	Unit
V_{CC1}, V_{CC2}	Supply voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.5	V
V_{CC2}	Supply voltage		V_{CC2}	-0.3 to V_{CC1}+0.1	V
AV$_{CC}$	Analog supply voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.5	V
V_I	Input voltage	$\overline{\text{RESET}}$, CNV$_{SS}$, BYTE, P6$_0$ to P6$_7$, P7$_2$ to P7$_7$, P8$_0$ to P8$_7$, P9$_0$ to P9$_7$, P10$_0$ to P10$_7$, P11$_0$ to P11$_7$, P14$_0$, P14$_1$, V_{REF}, X$_{IN}$		-0.3 to V_{CC1}+0.3	V
		P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P4$_0$ to P4$_7$, P5$_0$ to P5$_7$, P12$_0$ to P12$_7$, P13$_0$ to P13$_7$		-0.3 to V_{CC2}+0.3	V
		P7$_0$, P7$_1$		-0.3 to 6.5	V
V_O	Output voltage	P6$_0$ to P6$_7$, P7$_2$ to P7$_7$, P8$_0$ to P8$_4$, P8$_6$, P8$_7$, P9$_0$ to P9$_7$, P10$_0$ to P10$_7$, P11$_0$ to P11$_7$, P14$_0$, P14$_1$, X$_{OUT}$		-0.3 to V_{CC1}+0.3	V
		P0$_0$ to P0$_7$, P1$_0$ to P1$_7$, P2$_0$ to P2$_7$, P3$_0$ to P3$_7$, P4$_0$ to P4$_7$, P5$_0$ to P5$_7$, P12$_0$ to P12$_7$, P13$_0$ to P13$_7$		-0.3 to V_{CC2}+0.3	V
		P7$_0$, P7$_1$		-0.3 to 6.5	V
P_d	Power dissipation		Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature			-20 to 85 / -40 to 85	°C
T_{stg}	Storage temperature			-65 to 150	°C

Table 1.5.2. Recommended Operating Conditions (Note 1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply voltage($V_{CC1} \geq V_{CC2}$)		2.7	5.0	5.5	V
AVcc	Analog supply voltage			V_{CC1}		V
Vss	Supply voltage			0		V
AVss	Analog supply voltage			0		V
V_{IH}	HIGH input voltage	$P3_1$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P12_0$ to $P12_7$, $P13_0$ to $P13_7$	0.8V_{CC2}		V_{CC2}	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (during single-chip mode)	0.8V_{CC2}		V_{CC2}	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (data input during memory expansion and microprocessor modes)	0.5V_{CC2}		V_{CC2}	V
		$P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$, $P11_0$ to $P11_7$, $P14_0$, $P14_1$, X_{IN}, $\overline{RESET}$, CNV$_{SS}$, BYTE	0.8V_{CC1}		V_{CC1}	V
		$P7_0$, $P7_1$	0.8V_{CC1}		6.5	V
V_{IL}	LOW input voltage	$P3_1$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P12_0$ to $P12_7$, $P13_0$ to $P13_7$	0		0.2V_{CC2}	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (during single-chip mode)	0		0.2V_{CC2}	V
		$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$, $P3_0$ (data input during memory expansion and microprocessor modes)	0		0.16V_{CC2}	V
		$P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_7$, $P10_0$ to $P10_7$, $P11_0$ to $P11_7$, $P14_0$, $P14_1$, X_{IN}, $\overline{RESET}$, CNV$_{SS}$, BYTE	0		0.2V_{CC1}	V
$I_{OH\ (peak)}$	HIGH peak output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$,$P7_2$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$, $P12_0$ to $P12_7$, $P13_0$ to $P13_7$, $P14_0$, $P14_1$			-10.0	mA
$I_{OH\ (avg)}$	HIGH average output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$,$P7_2$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$, $P12_0$ to $P12_7$, $P13_0$ to $P13_7$, $P14_0$, $P14_1$			-5.0	mA
$I_{OL\ (peak)}$	LOW peak output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$,$P7_0$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$, $P12_0$ to $P12_7$, $P13_0$ to $P13_7$, $P14_0$, $P14_1$			10.0	mA
$I_{OL\ (avg)}$	LOW average output current	$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$,$P7_0$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$, $P12_0$ to $P12_7$, $P13_0$ to $P13_7$, $P14_0$, $P14_1$			5.0	mA
f (X_{IN})	Main clock input oscillation frequency (Note 4)	V_{CC1}=3.0 to 5.5V	0		16	MHz
		V_{CC1}=2.7 to 3.0V	0		20 X V_{CC1}-44	MHz
f (X_{CIN})	Sub-clock oscillation frequency			32.768	50	kHz
f (Ring)	Ring oscillation frequency			1		MHz
f (PLL)	PLL clock oscillation frequency (Note 4)	V_{CC1}=3.0 to 5.5V	10		24	MHz
		V_{CC1}=2.7 to 3.0V	10		46.67 X V_{CC1}-116	MHz
f (BCLK)	CPU operation clock		0		24	MHz
T_{SU}(PLL)	PLL frequency synthesizer stabilization wait time	V_{CC1}=5.0V			20	ms
		V_{CC1}=3.0V			50	ms

Note 1: Referenced to Vcc = V_{CC1} = V_{CC2} = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
Note 2: The mean output current is the mean value within 100ms.
Note 3: The total I_{OL} (peak) for ports P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, $P14_0$ and $P14_1$ must be 80mA max. The total I_{OL} (peak) for ports P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12, and P13 must be 80mA max. The total I_{OH} (peak) for ports P0, P1, and P2 must be -40mA max. The total I_{OH} (peak) for ports P3, P4, P5, P12, and P13 must be -40mA max. The total I_{OH} (peak) for ports P6, P7, and $P8_0$ to $P8_4$ must be -40mA max. The total I_{OH} (peak) for ports $P8_6$, $P8_7$, P9, P10, P11, $P14_0$, and $P14_1$ must be -40mA max.
Note 4: Relationship between main clock oscillation frequency, PLL clock oscillation frequency and supply voltage.



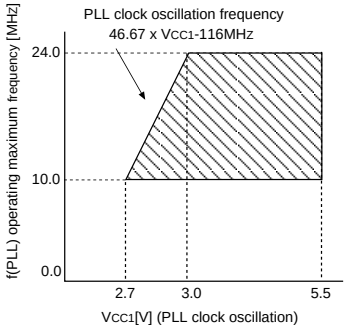


Table 1.5.3. A-D Conversion Characteristics (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{REF} =V_{CC1}				10	Bits
INL	Integral non-linearity error	10 bit	V_{REF}= V_{CC1}= 5V	AN_0 to AN_7 input			±3	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN_{00} to AN_{07} input AN_{20} to AN_{27} input			±7	LSB
			V_{REF}= V_{CC1}= 3.3V	AN_0 to AN_7 input			±5	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN_{00} to AN_{07} input AN_{20} to AN_{27} input			±7	LSB
		8 bit	V_{REF} =V_{CC1}=3.3V				±2	LSB
–	Absolute accuracy	10 bit	V_{REF}= V_{CC1}= 5V	AN_0 to AN_7 input			±3	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN_{00} to AN_{07} input AN_{20} to AN_{27} input			±7	LSB
			V_{REF}= V_{CC1}= 3.3V	AN_0 to AN_7 input			±5	LSB
				ANEX0, ANEX1 input External operation amp connection mode AN_{00} to AN_{07} input AN_{20} to AN_{27} input			±7	LSB
		8 bit	V_{REF} =V_{CC1}=3.3V				±2	LSB
DNL	Differential non-linearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
R_{LADDER}	Ladder resistance		V_{REF} =V_{CC1}		10		40	kΩ
t_{CONV}	Conversion time(10bit), Sample & hold function available		V_{REF} =V_{CC1}=5V, $ø_{AD}$=10MHz		3.3			µs
t_{CONV}	Conversion time(8bit), Sample & hold function available		V_{REF} =V_{CC1}=5V, $ø_{AD}$=10MHz		2.8			µs
t_{SAMP}	Sampling time				0.3			µs
V_{REF}	Reference voltage				2.0		V_{CC1}	V
V_{IA}	Analog input voltage				0		V_{REF}	V

Note 1: Referenced to V_{CC1}=AV_{CC}=V_{REF}=3.3 to 5.5V, V_{SS}=AV_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
Note 2: If V_{CC1} > V_{CC2}, do not use AN_{00} to AN_{07} and AN_{20} to AN_{27} as analog input pins.
Note 3: AD operation clock frequency ($Ø_{AD}$ frequency) must be 10 MHz or less. And divide the f_{AD} if V_{CC1} is less than 4.2V, and make $Ø_{AD}$ frequency equal to or lower than f_{AD}/2.
Note 4: A case without sample & hold function turn $Ø_{AD}$ frequency into 250 kHz or more in addition to a limit of Note 3.
A case with sample & hold function turn $Ø_{AD}$ frequency into 1MHz or more in addition to a limit of Note 3.

Table 1.5.4. D-A Conversion Characteristics (Note 1)

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy				1.0	%
t_{su}	Setup time				3	µs
R_O	Output resistance		4	10	20	kΩ
I_{VREF}	Reference power supply input current	(Note 2)			1.5	mA

Note 1: Referenced to V_{CC1}=V_{REF}=3.3 to 5.5V, V_{SS}=AV_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
Note 2: This applies when using one D-A converter, with the D-A register for the unused D-A converter set to "00_{16}". The A-D converter's ladder resistance is not included. Also, when D-A register contents are not "00_{16}", the current I_{VREF} always flows even though Vref may have been set to be unconnected by the A-D control register.

Table 1.5.5. Flash Memory Version Electrical Characteristics (Note 1) 100 times guarantee article

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Word program time			30	200	µs
–	Block erase time			1	4	s
–	Erase all unlocked blocks time			1 X n	4 X n	s
–	Lock bit program time			30	200	µs
t_{PS}	Flash memory circuit stabilization wait time				15	µs

Note 1: Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C unless otherwise specified.
Note 2: n denotes the number of block erases.

Table 1.5.6. Flash Memory Version Electrical Characteristics (Note 1) 10,000 times guarantee article (block1 and block A(Note 3))

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max	
–	Word program time			30	T.B.D	µs
–	Block erase time			1	T.B.D	s
–	Erase all unlocked blocks time			1 X n	T.B.D	s
–	Lock bit program time			30	T.B.D	µs
t_{PS}	Flash memory circuit stabilization wait time				15	µs

Note 1: Referenced to V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr = 0 to 60 °C unless otherwise specified.
Note 2: n denotes the number of block erases.
Note 3: Shown here are the rated values for block 1 and block A when they have been programmed and erased more than 1,000 times. The rated values up to 1,000 times of programming and erasure are the same for all blocks as those products that are guaranteed of 100 times of programming and erasure.

Table 1.5.7. Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at Topr = 0 to 60°C)

Flash program, erase voltage	Flash read operation voltage
V_{CC1} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V	V_{CC1}=2.7 to 5.5 V

Table 1.5.8. Low Voltage Detection Circuit Electrical Characteristics (Note 1)

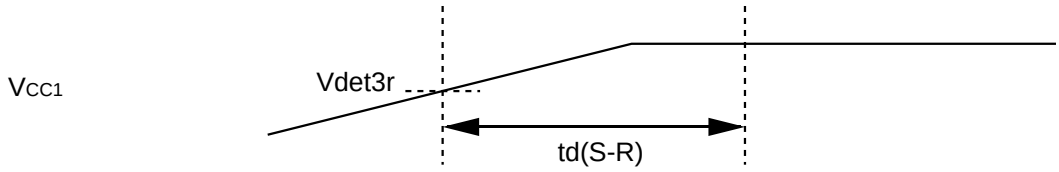
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Voltage down detection voltage (Note 1)	V_{CC1}=0.8 to 5.5V	3.3	3.8	4.4	V
Vdet3	Reset level detection voltage (Notes 1, 2)		2.2	2.8	3.6	V
Vdet3s	Low voltage reset retention voltage		0.8			V
Vdet3r	Low voltage reset release voltage (Note 3)		2.2	2.9	4.0	V
Vdet2	RAM retention limit detection voltage (Note 1)		1.4	2.0	2.7	V

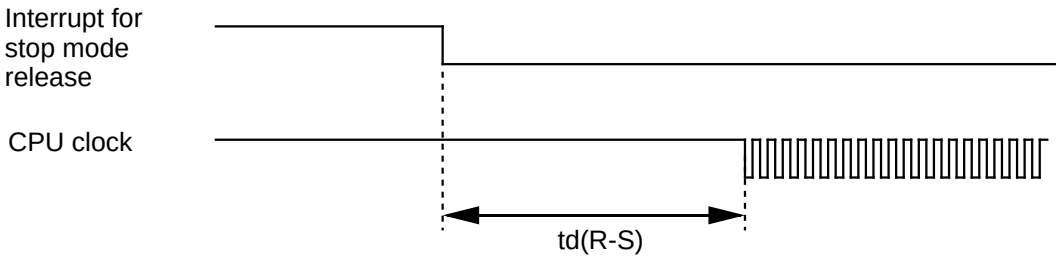
Note 1: Vdet4 > Vdet3 > Vdet2
Note 2: Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the operation at f(BCLK) ≤ 10MHz is guaranteed.
Note 3: Vdet3r > Vdet3 is not guaranteed.

Table 1.5.9. Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on	V_{CC1}=2.7 to 5.5V			2	ms
td(R-S)	STOP release time				150	µs
td(W-S)	Low power dissipation mode wait mode release time				150	µs
td(M-L)	Time for internal power supply stabilization when main clock oscillation starts				50	µs
td(S-R)	Hardware reset 2 release wait time	V_{CC1}=Vdet3r to 5.5V		6 (Note)	20	ms
td(E-A)	Low voltage detection circuit operation start time	V_{CC1}=2.7 to 5.5V			20	µs

Note : When V_{CC1} = 5V





V_{CC1} = V_{CC2} = 5V

Table 1.5.10. Electrical Characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	$P6_0$ to $P6_7$,$P7_2$ to $P7_7$,$P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$, $P10_0$ to $P10_7$,$P11_0$ to $P11_7$,$P14_0$,$P14_1$	I_{OH}=-5mA	V_{CC1}-2.0		V_{CC1}	V
		$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$	I_{OH}=-5mA(Note 2)	V_{CC2}-2.0		V_{CC2}	
V_{OH}	HIGH output voltage	$P6_0$ to $P6_7$,$P7_2$ to $P7_7$,$P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$, $P10_0$ to $P10_7$,$P11_0$ to $P11_7$,$P14_0$,$P14_1$	I_{OH}=-200µA	V_{CC1}-0.3		V_{CC1}	V
		$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$	I_{OH}=-200µA(Note 2)	V_{CC2}-0.3		V_{CC2}	
V_{OH}	HIGH output voltage	X_{OUT} HIGHPOWER	I_{OH}=-1mA	V_{CC1}-2.0		V_{CC1}	V
		X_{OUT} LOWPOWER	I_{OH}=-0.5mA	V_{CC1}-2.0		V_{CC1}	
	HIGH output voltage	X_{COUT} HIGHPOWER	With no load applied		2.5		V
		X_{COUT} LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	$P6_0$ to $P6_7$,$P7_0$ to $P7_7$,$P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$, $P10_0$ to $P10_7$,$P11_0$ to $P11_7$,$P14_0$,$P14_1$	I_{OL}=5mA			2.0	V
		$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$	I_{OL}=5mA(Note 2)			2.0	
V_{OL}	LOW output voltage	$P6_0$ to $P6_7$,$P7_0$ to $P7_7$,$P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$, $P10_0$ to $P10_7$,$P11_0$ to $P11_7$,$P14_0$,$P14_1$	I_{OL}=200µA			0.45	V
		$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$	I_{OL}=200µA(Note 2)			0.45	
V_{OL}	LOW output voltage	X_{OUT} HIGHPOWER	I_{OL}=1mA			2.0	V
		X_{OUT} LOWPOWER	I_{OL}=0.5mA			2.0	
	LOW output voltage	X_{COUT} HIGHPOWER	With no load applied		0		V
		X_{COUT} LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$ to $TA4_{IN}$, $TB0_{IN}$ to $TB5_{IN}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, SCL, SDA, $CLK0$ to $CLK4$,$TA2_{OUT}$ to $TA4_{OUT}$, $\overline{KI0}$ to $\overline{KI3}$, $RxD0$ to $RxD2$, S_{IN3}, S_{IN4}		0.2		1.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		2.2	V
I_{IH}	HIGH input current	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_0$ to $P7_7$, $P8_0$ to $P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$,$P11_0$ to $P11_7$, $P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I=5V			5.0	µA
I_{IL}	LOW input current	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_0$ to $P7_7$, $P8_0$ to $P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$,$P11_0$ to $P11_7$, $P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_2$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$	V_I=0V	30	50	170	kΩ
R_{fXIN}	Feedback resistance	X_{IN}			1.5		MΩ
R_{fXCIN}	Feedback resistance	X_{CIN}			15		MΩ
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

Note 1: Referenced to V_{CC}=V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=24MHz unless otherwise specified.
Note 2: Where the product is used at V_{CC1} = 5 V and V_{CC2} = 3 V, refer to the 3 V version value for the pin specified value on the V_{CC2} port side.

V_{CC1} = V_{CC2} = 5V

Table 1.5.11. Electrical Characteristics (2) (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC1}=4.0 to 5.5V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(BCLK)=24MHz, No division, PLL operation		14	20	mA
				No division, Ring oscillation		1		mA
			Flash memory	f(BCLK)=24MHz, No division, PLL operation		18	27	mA
				No division, Ring oscillation		1.8		mA
			Flash memory Program	f(BCLK)=10MHz, V_{CC1}=5.0V		15		mA
			Flash memory Erase	f(BCLK)=10MHz, V_{CC1}=5.0V		25		mA
			Mask ROM	f(X_{CIN})=32kHz, Low power dissipation mode, ROM(Note 3)		25		µA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		µA
				f(BCLK)=32kHz Low power dissipation mode, Flash memory(Note 3)		420		µA
				Ring oscillation, Wait mode		50		µA
			Mask ROM Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		7.5		µA
				f(BCLK)=32kHz, Wait mode(Note 2), Oscillation capacity Low		2.0		µA
				Stop mode, T_{opr}=25°C		0.8	3.0	µA
Idet4	Voltage down detection dissipation current (Note 4)					0.7	4	µA
Idet3	Reset area detection dissipation current (Note 4)					1.2	8	µA
Idet2	RAM retention limit detection dissipation current (Note 4)					1.1	6	µA

Note 1: Referenced to V_{CC}=V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=24MHz unless otherwise specified.
Note 2: With one timer operated using f_{C32}.
Note 3: This indicates the memory in which the program to be executed exists.
Note 4: Idet is dissipation current when the following bit is set to "1" (detection circuit enabled).
Idet4: VC27 bit of VCR2 register
Idet3: VC26 bit of VCR2 register
Idet2: VC25 bit of VCR2 register

V_{CC1} = V_{CC2} = 5V

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.12. External Clock Input (X_{IN} input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	62.5		ns
$t_{w(H)}$	External clock input HIGH pulse width	25		ns
$t_{w(L)}$	External clock input LOW pulse width	25		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Table 1.5.13. Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	40		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	30		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ input setup time	40		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time		40	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 45 \quad [ns]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 \quad [ns]$$

n is “2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 45 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

V_{CC1} = V_{CC2} = 5V

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.14. Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	100		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	40		ns

Table 1.5.15. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	400		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	200		ns

Table 1.5.16. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	200		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	100		ns

Table 1.5.17. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	100		ns

Table 1.5.18. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	400		ns

Table 1.5.19. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAi_{OUT} input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAi_{IN} input setup time	200		ns

V_{CC1} = V_{CC2} = 5V

Timing Requirements

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.20. Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 1.5.21. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 1.5.22. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 1.5.23. A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	125		ns

Table 1.5.24. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	30		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.5.25. External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	250		ns

V_{CC1} = V_{CC2} = 5V

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.26. Memory Expansion and Microprocessor Modes (for setting with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \quad [ns]$$ f(BCLK) is 12.5MHz or less.

Note 2: Calculated according to the BCLK frequency as follows:

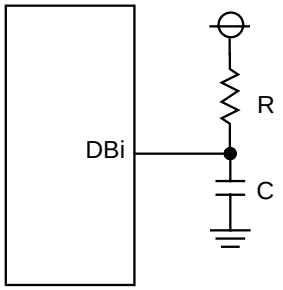
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$t = -CR \times \ln(1 - V_{OL} / V_{CC2})$

by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is

$t = -30pF \times 1k\Omega \times \ln(1 - 0.2V_{CC2} / V_{CC2})$
$= 6.7ns.$



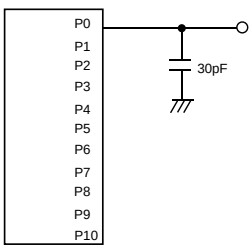


Figure 1.5.1. Ports P0 to P10 Measurement Circuit

V_{CC1} = V_{CC2} = 5V

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.27. Memory Expansion and Microprocessor Modes
(for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n=1, f(BCLK) is 12.5MHz or less.

Note 2: Calculated according to the BCLK frequency as follows:

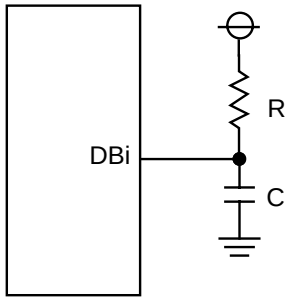
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$$t = -CR \times \ln (1 - V_{OL} / V_{CC2})$$

by a circuit of the right figure.
For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output “L” level is

$$t = -30pF \times 1k\Omega \times \ln (1 - 0.2V_{CC2} / V_{CC2})$$
$$= 6.7ns.$$



V_{CC1} = V_{CC2} = 5V

Switching Characteristics

(V_{CC1} = V_{CC2} = 5V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.28. Memory Expansion and Microprocessor Modes
(for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.5.1		25	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			25	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			25	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			25	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (refers to BCLK)			25	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (refers to BCLK)		– 4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (refers to Address)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (refers to Adderss)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Adress		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of Adress		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 25 \quad [ns]$$

Note 4: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 \quad [ns]$$

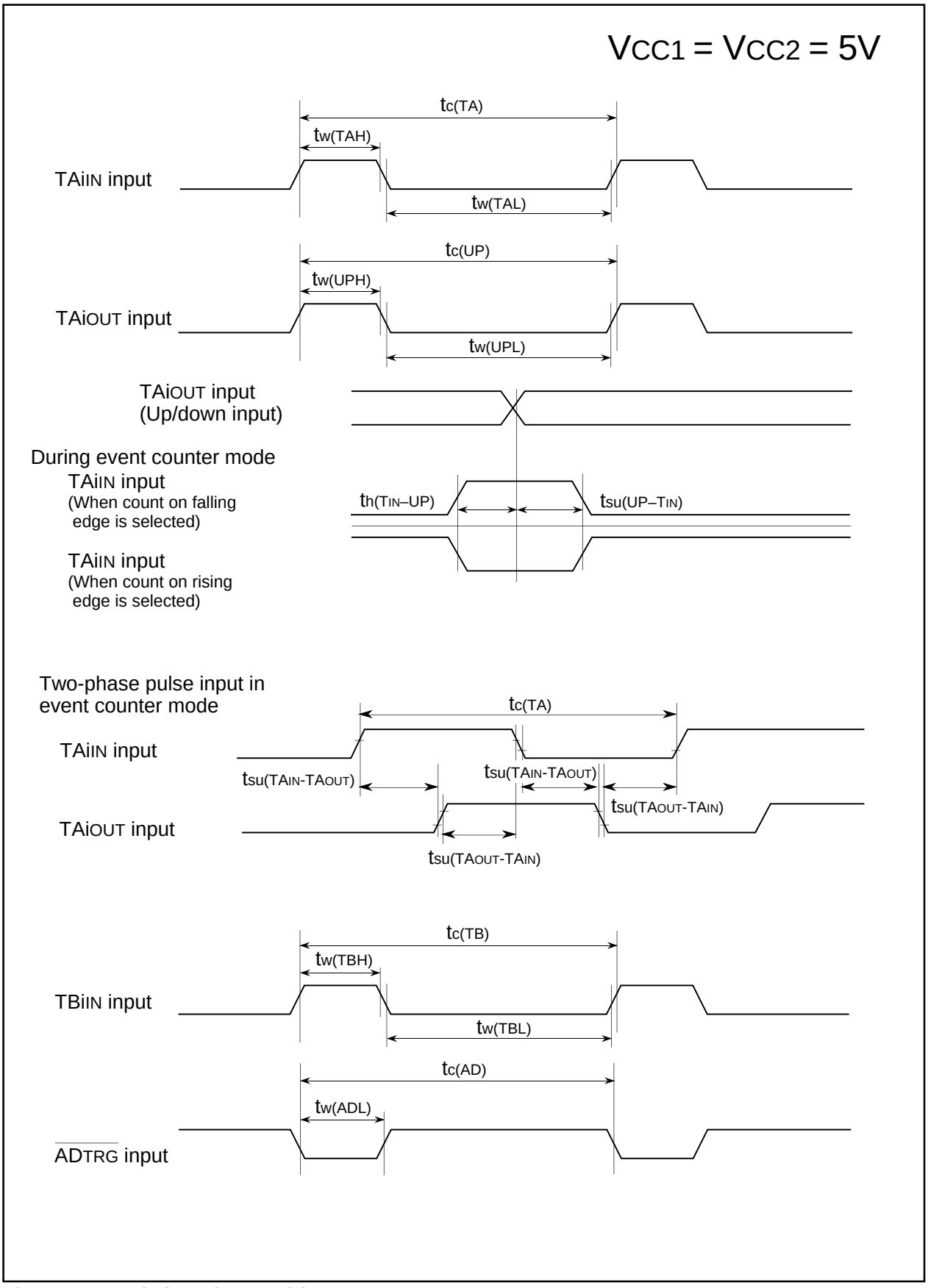


Figure 1.5.2. Timing Diagram (1)

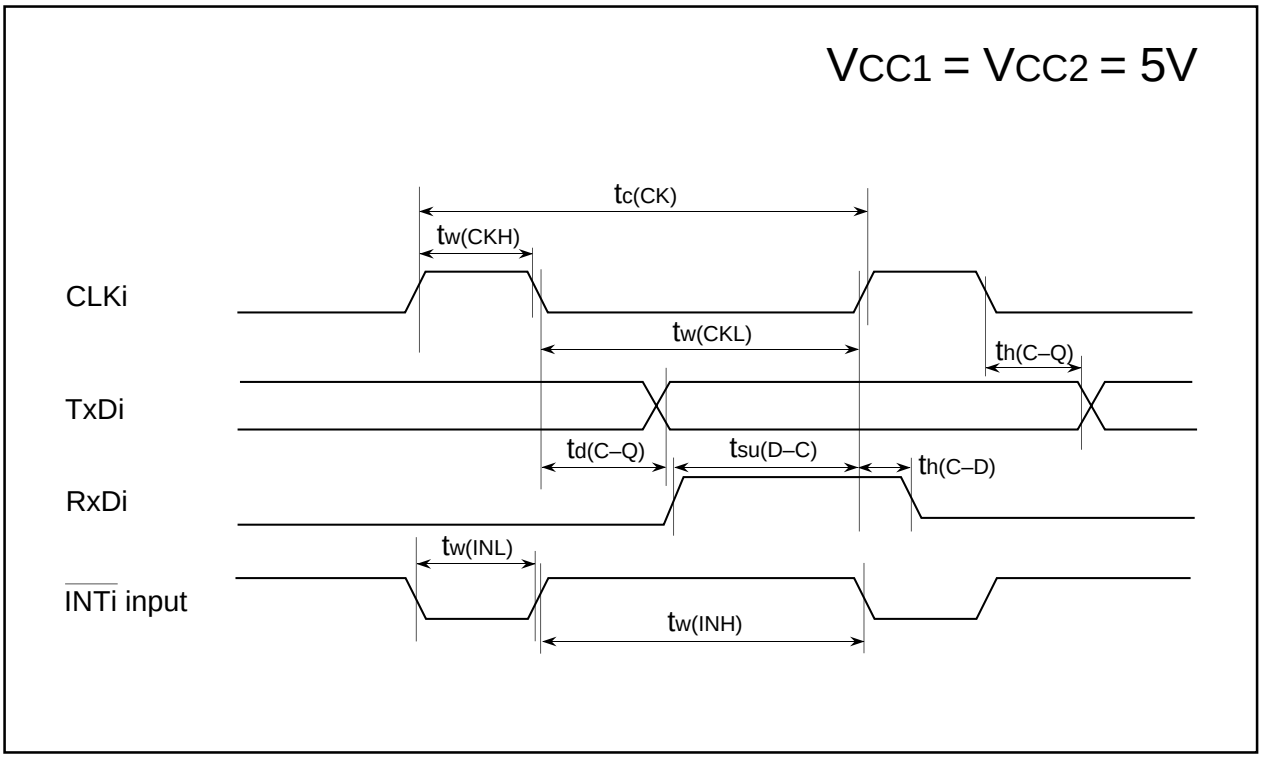
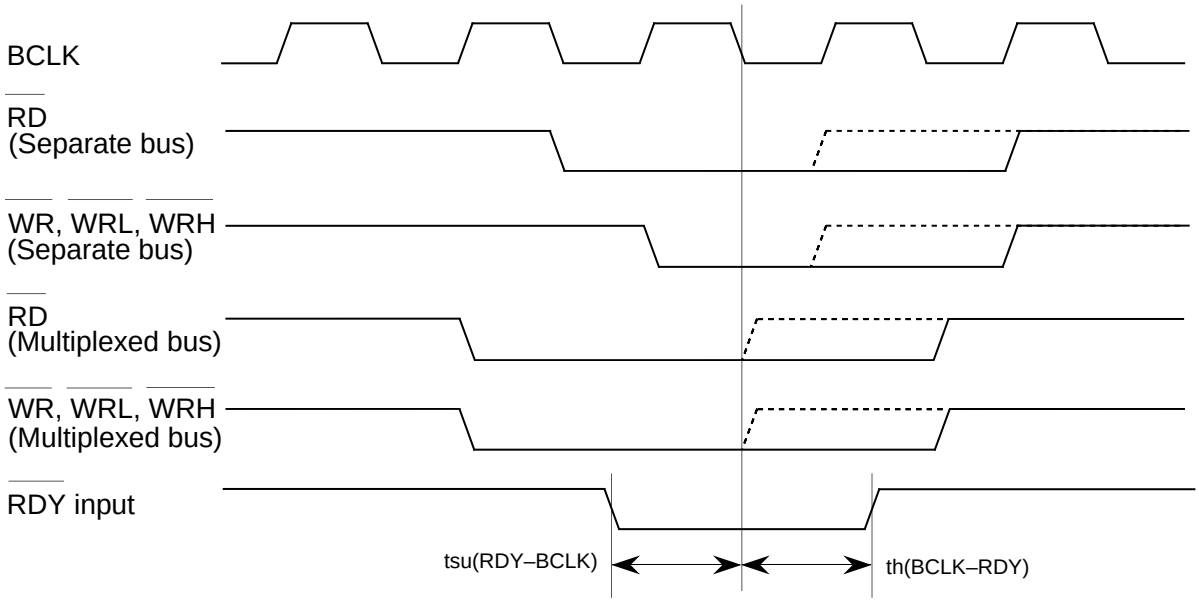


Figure 1.5.3. Timing Diagram (2)

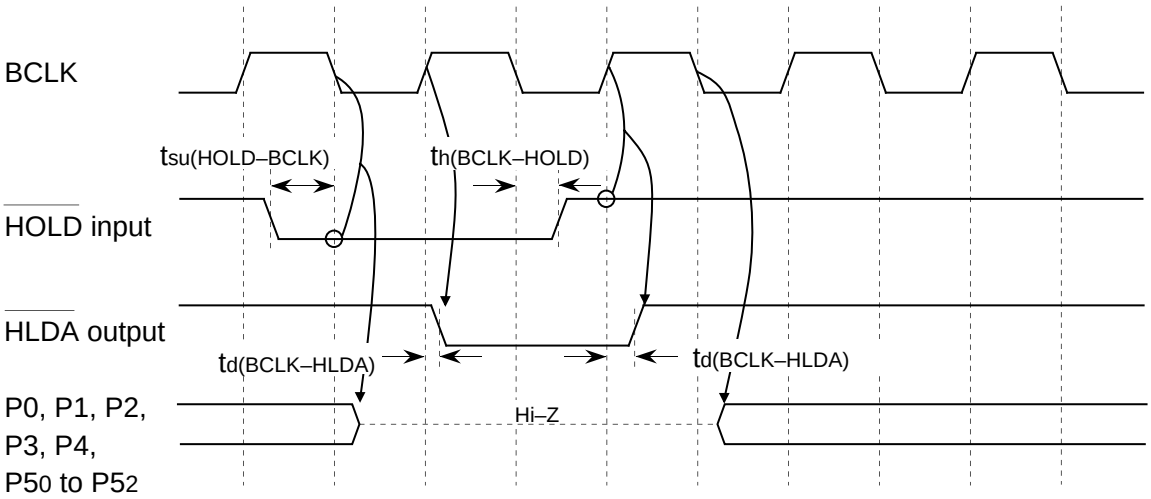
V_{CC1} = V_{CC2} = 5V

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait**)**



(Common to setting with wait and setting without wait**)**



Note: The above pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit in PM0 register and PM11 bit in PM1 register.

Measuring conditions :

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : Determined with V_{IL}=1.0V, V_{IH}=4.0V
- Output timing voltage : Determined with V_{OL}=2.5V, V_{OH}=2.5V

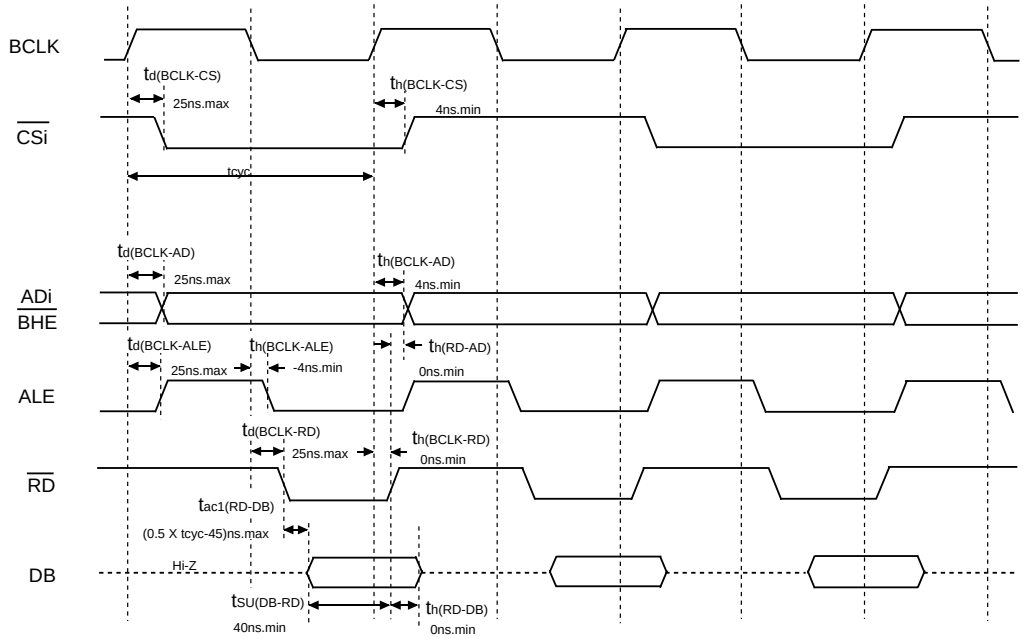
Figure 1.5.4. Timing Diagram (3)

V_{CC1} = V_{CC2} = 5V

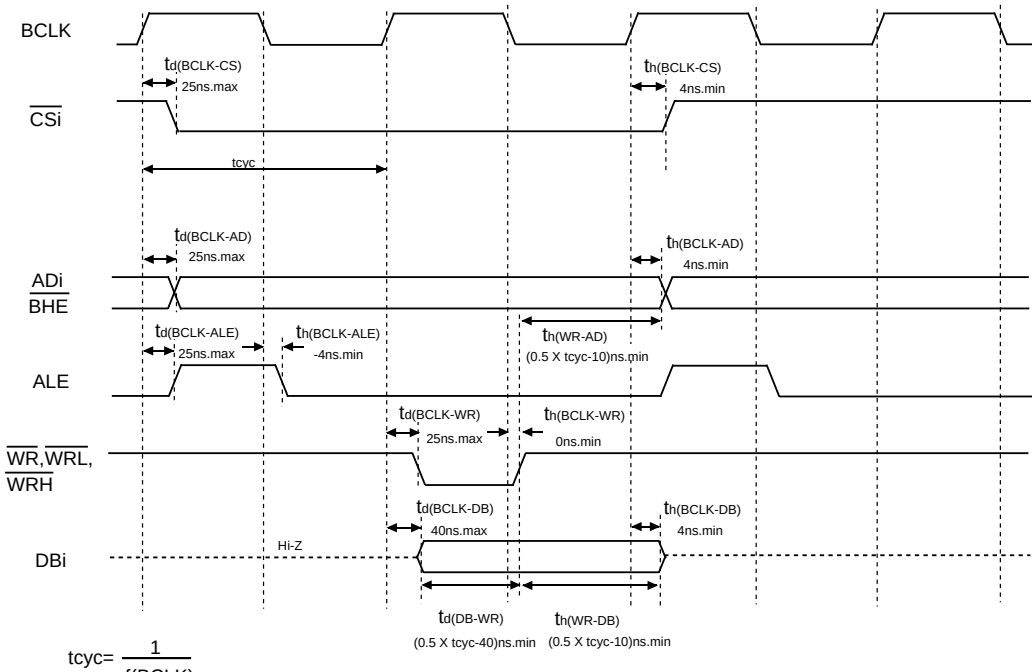
Memory Expansion Mode, Microprocessor Mode

(For setting with no wait**)**

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

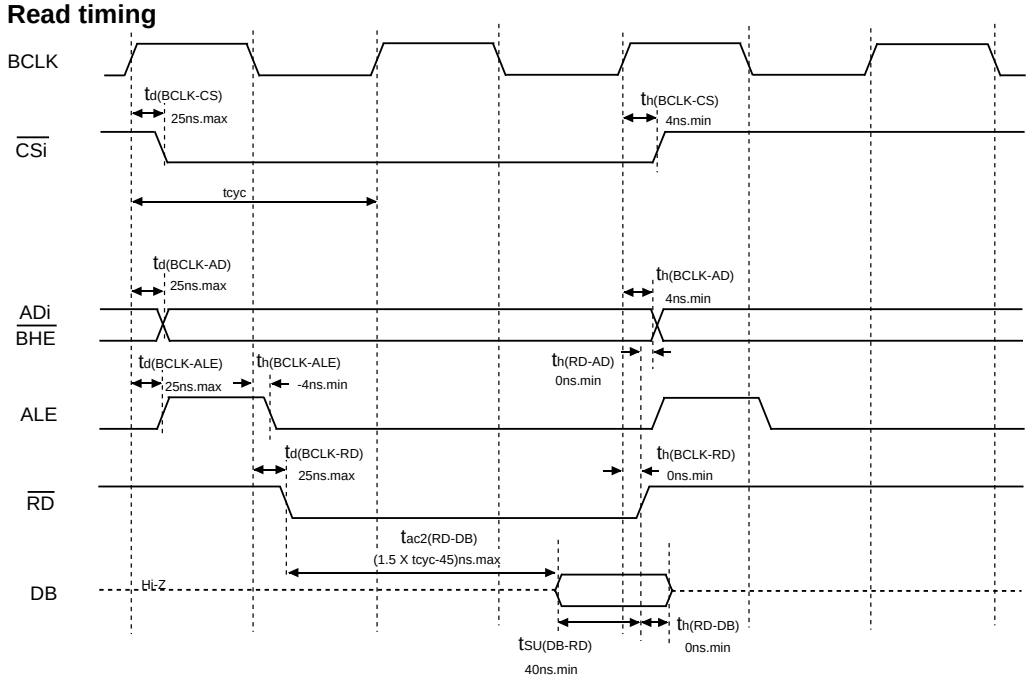
Figure 1.5.5. Timing Diagram (4)

V_{CC1} = V_{CC2} = 5V

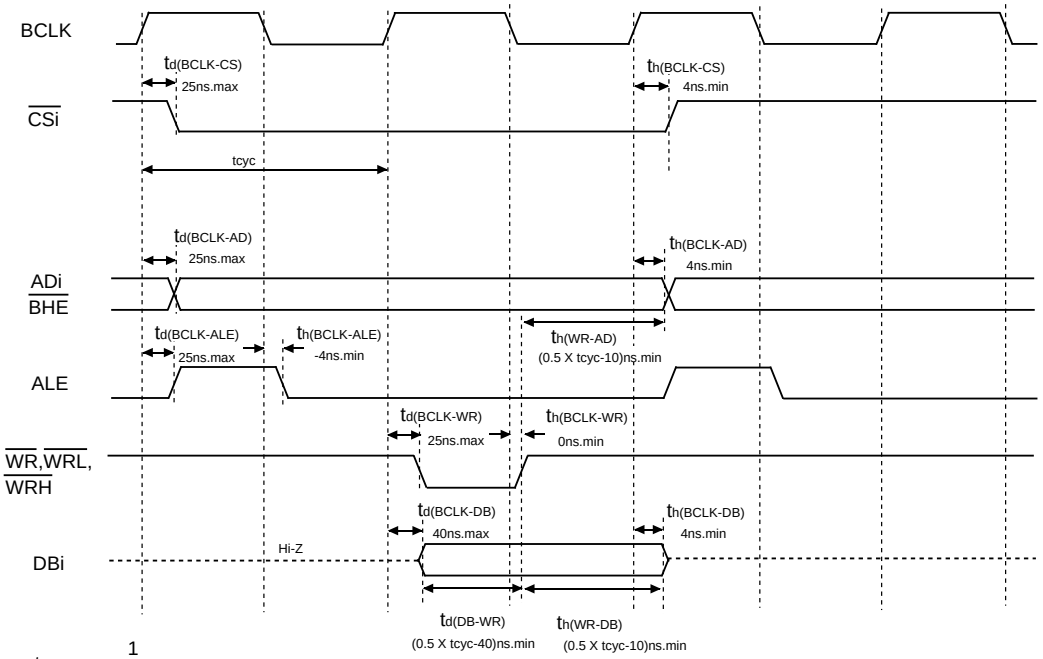
Memory Expansion Mode, Microprocessor Mode

(for 1-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

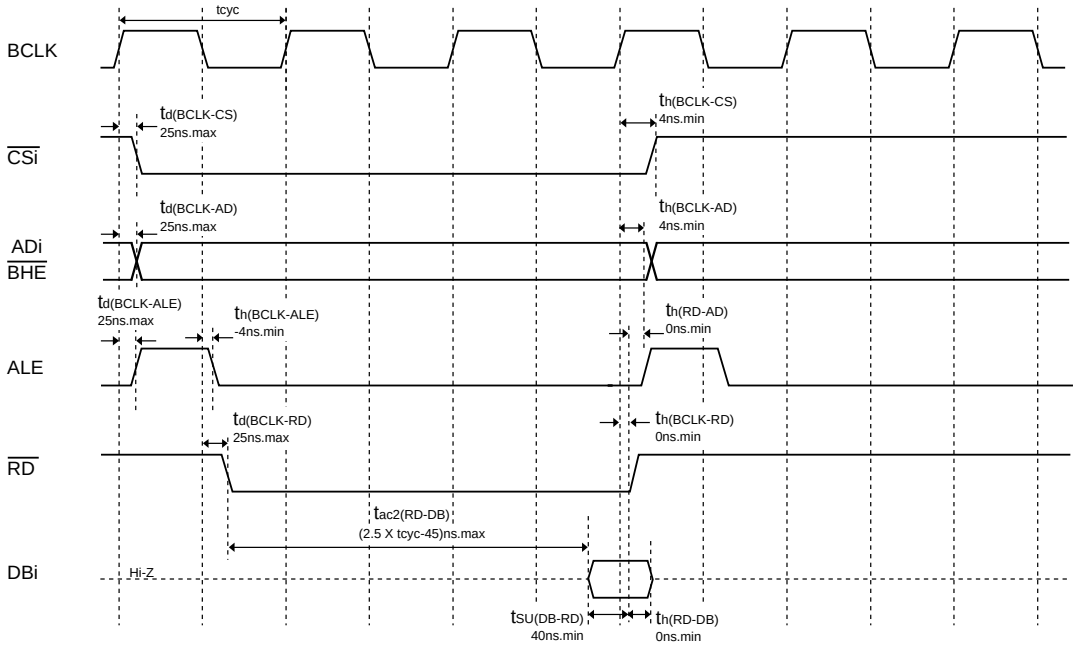
Figure 1.5.6. Timing Diagram (5)

V_{CC1} = V_{CC2} = 5V

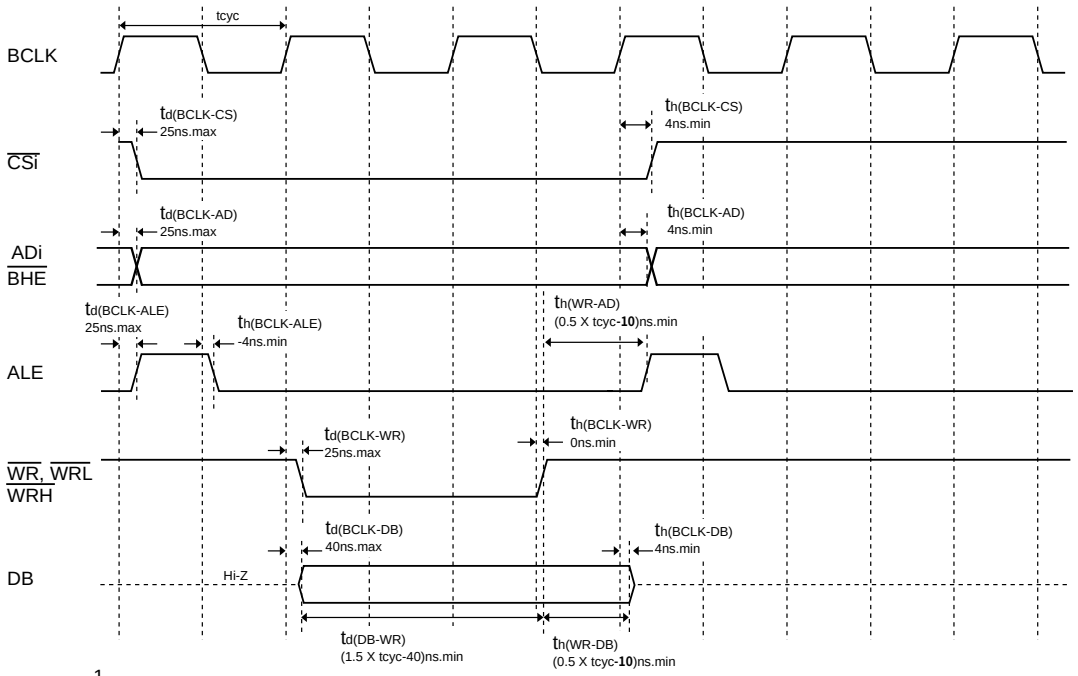
Memory Expansion Mode, Microprocessor Mode

(for 2-wait setting and external area access **)**

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V

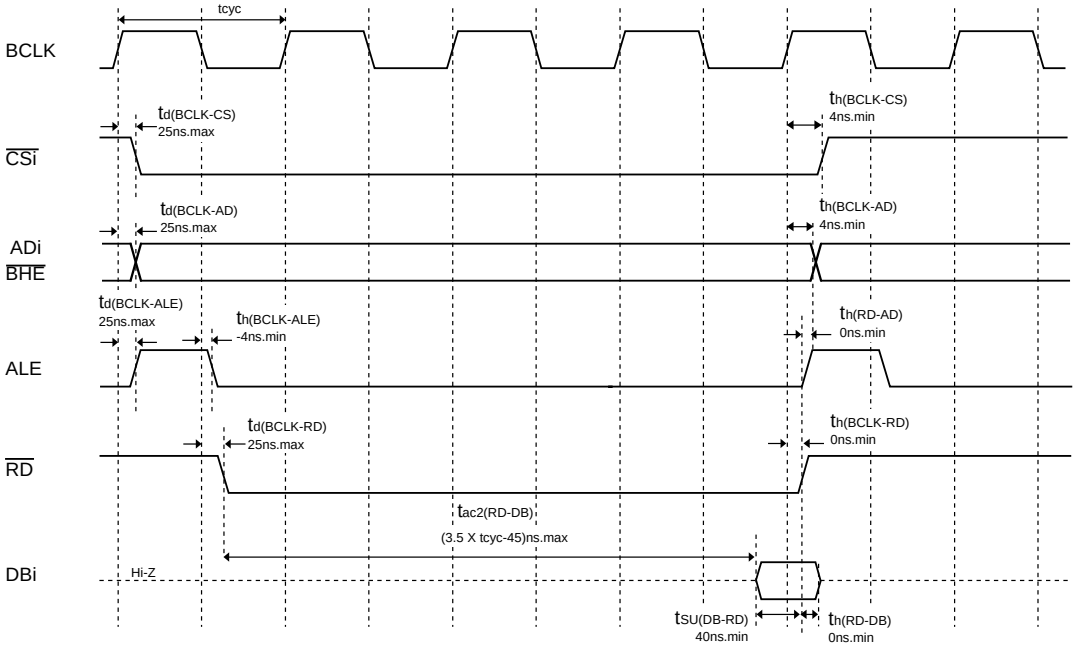
Figure 1.5.7. Timing Diagram (6)

V_{CC1} = V_{CC2} = 5V

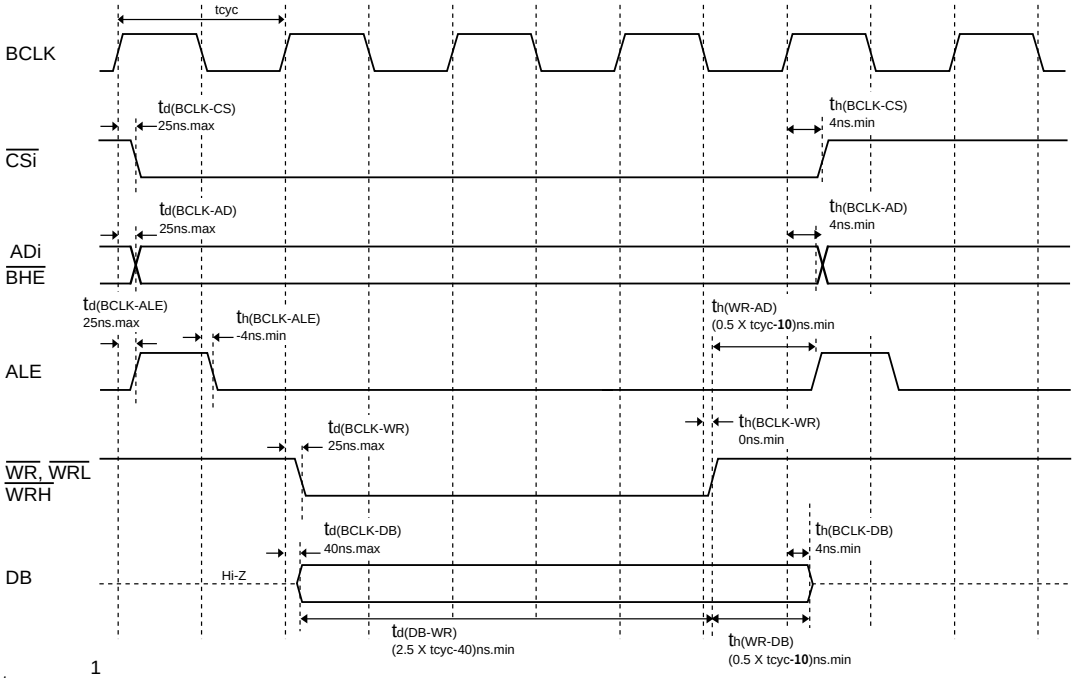
Memory Expansion Mode, Microprocessor Mode

(for 3-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

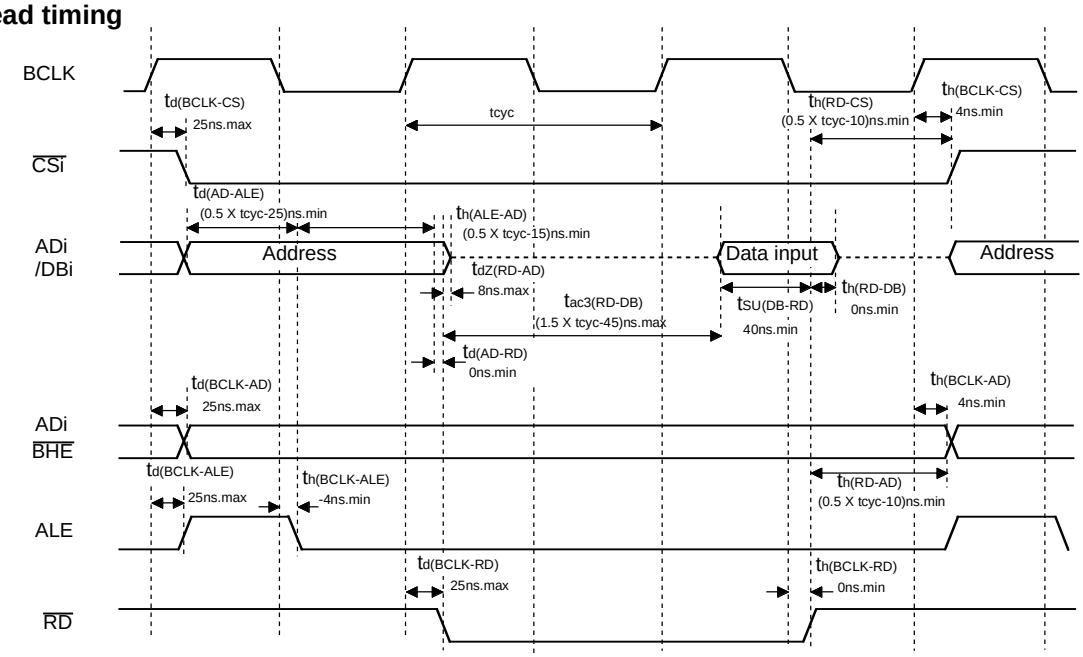
Figure 1.5.8. Timing Diagram (7)

V_{CC1} = V_{CC2} = 5V

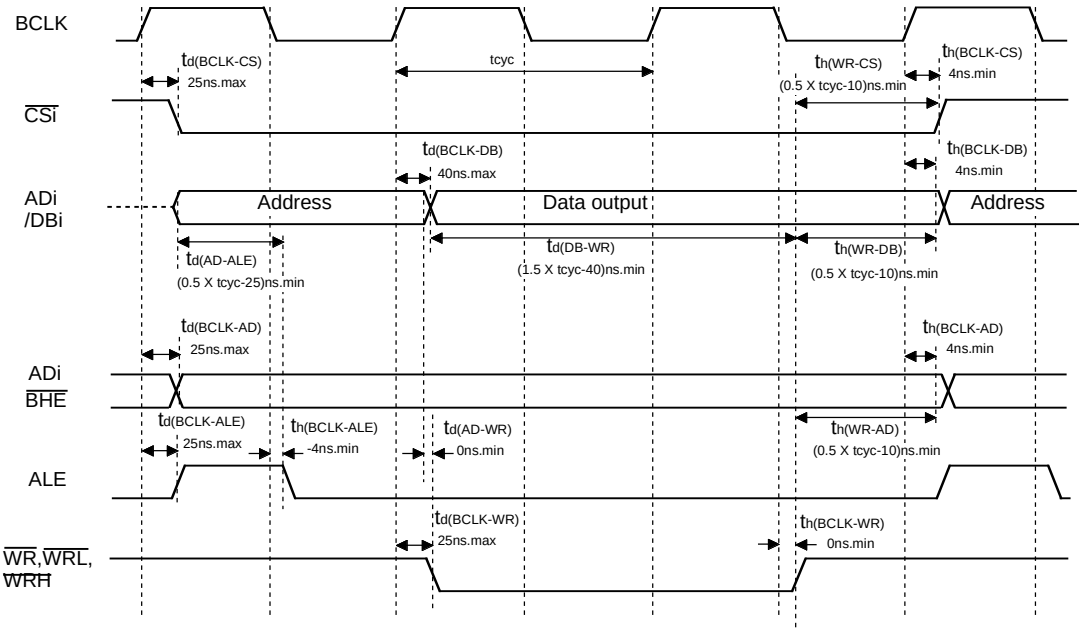
Memory Expansion Mode, Microprocessor Mode

(For 1- or 2-wait setting, external area access and multiplex bus selection**)**

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

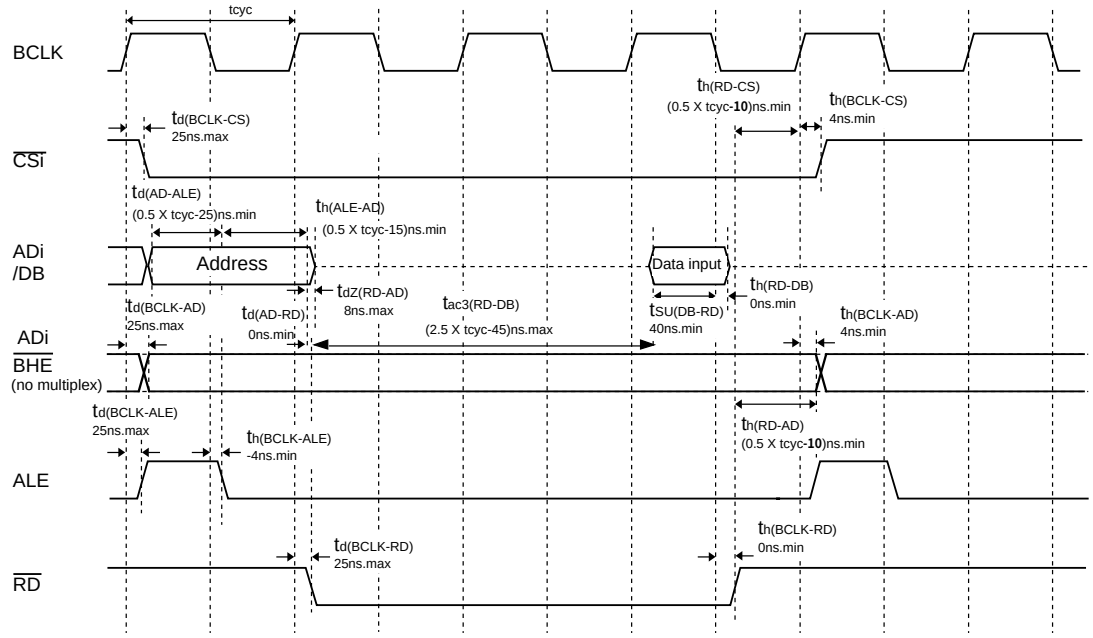
Figure 1.5.9. Timing Diagram (8)

V_{CC1} = V_{CC2} = 5V

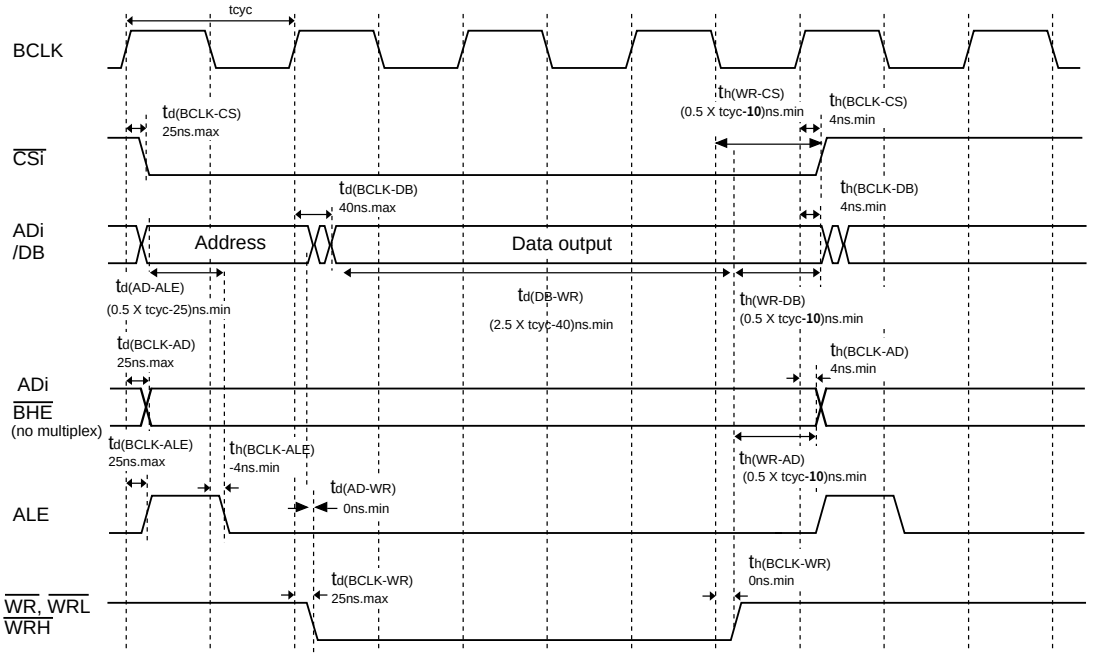
Memory Expansion Mode, Microprocessor Mode

(For 3-wait setting, external area access and multiplex bus selection **)**

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=5V
- Input timing voltage : V_{IL}=0.8V, V_{IH}=2.0V
- Output timing voltage : V_{OL}=0.4V, V_{OH}=2.4V

Figure 1.5.10. Timing Diagram (9)

V_{CC1} = V_{CC2} = 3V

Table 1.5.29. Electrical Characteristics (Note)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_2$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$	I_{OH}=-1mA	V_{CC}-0.5		V_{CC}	V
V_{OH}	HIGH output voltage X_{OUT}	HIGHPOWER	I_{OH}=-0.1mA	V_{CC}-0.5		V_{CC}	V
		LOWPOWER	I_{OH}=-50µA	V_{CC}-0.5		V_{CC}	
	HIGH output voltage X_{COUT}	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
V_{OL}	LOW output voltage	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_0$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$	I_{OL}=1mA			0.5	V
V_{OL}	LOW output voltage X_{OUT}	HIGHPOWER	I_{OL}=0.1mA			0.5	V
		LOWPOWER	I_{OL}=50µA			0.5	
	LOW output voltage X_{COUT}	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$ to $TA4_{IN}$, $TB0_{IN}$ to $TB5_{IN}$, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS2}$, SCL, SDA, $CLK0$ to $CLK4$, $TA2_{OUT}$ to $TA4_{OUT}$, $\overline{KI0}$ to $\overline{KI3}$, $RxD0$ to $RxD2$, $SIN3$,$SIN4$		0.2		0.8	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2	(0.7)	1.8	V
I_{IH}	HIGH input current	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_0$ to $P7_7$, $P8_0$ to $P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$,$P11_0$ to $P11_7$, $P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I=3V			4.0	µA
I_{IL}	LOW input current	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_0$ to $P7_7$, $P8_0$ to $P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$,$P11_0$ to $P11_7$, $P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$, X_{IN}, $\overline{RESET}$, CNVss, BYTE	V_I=0V			-4.0	µA
R_{PULLUP}	Pull-up resistance	$P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_7$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_7$,$P6_0$ to $P6_7$,$P7_2$ to $P7_7$, $P8_0$ to $P8_4$,$P8_6$,$P8_7$,$P9_0$ to $P9_7$,$P10_0$ to $P10_7$, $P11_0$ to $P11_7$,$P12_0$ to $P12_7$,$P13_0$ to $P13_7$,$P14_0$,$P14_1$	V_I=0V	50	100	500	kΩ
R_{fXIN}	Feedback resistance X_{IN}				3.0		MΩ
R_{fXCIN}	Feedback resistance X_{CIN}				25		MΩ
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

Note 1 : Referenced to V_{CC}=V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.
Note 2 : V_{CC1} for the port P6 to P11 and P14, and V_{CC2} for the port P0 to P5 and P12 to P13.

V_{CC1} = V_{CC2} = 3V

Table 1.5.30. Electrical Characteristics (2) (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC1}=2.7 to 3.6V)	In single-chip mode, the output pins are open and other pins are V_{SS}	Mask ROM	f(BCLK)=10MHz, No division		8	11	mA
				No division, Ring oscillation		1		mA
			Flash memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, Ring oscillation		1.8		mA
			Flash memory Program	f(BCLK)=10MHz, V_{CC1}=3.0V		12		mA
			Flash memory Erase	f(BCLK)=10MHz, V_{CC1}=3.0V		22		mA
			Mask ROM	f(X_{CIN})=32kHz, Low power dissipation mode, ROM(Note 3)		25		µA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		µA
				f(BCLK)=32kHz, Low power dissipation mode, Flash memory(Note 3)		420		µA
				Ring oscillation, Wait mode		45		µA
			Mask ROM Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		6.0		µA
				f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity Low		1.8		µA
				Stop mode, T_{opr}=25°C		0.7	3.0	µA
Idet4	Voltage down detection dissipation current (Note 4)					0.6	4	µA
Idet3	Reset level detection dissipation current (Note 4)					0.4	2	µA
Idet2	RAM retention limit detection dissipation current (Note 4)					0.9	4	µA

Note 1: Referenced to V_{CC}=V_{CC1}=V_{CC2}=2.7 to 3.3V, V_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.
Note 2: With one timer operated using f_{C32}.
Note 3: This indicates the memory in which the program to be executed exists.
Note 4: Idet is dissipation current when the following bit is set to "1" (detection circuit enabled).
Idet4: VC27 bit of VCR2 register
Idet3: VC26 bit of VCR2 register
Idet2: VC25 bit of VCR2 register

V_{CC1} = V_{CC2} = 3V

Timing Requirements

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.31. External Clock Input (X_{IN} input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

Table 1.5.32. Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data input access time (for setting with no wait)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data input access time (for setting with wait)		(Note 2)	ns
$t_{ac3(RD-DB)}$	Data input access time (when accessing multiplex bus area)		(Note 3)	ns
$t_{su(DB-RD)}$	Data input setup time	50		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ input setup time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ input setup time	50		ns
$t_{h(RD-DB)}$	Data input hold time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ output delay time		40	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 60 \quad [ns]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \quad [ns]$$

n is “2” for 1-wait setting, “3” for 2-wait setting and “4” for 3-wait setting.

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 60 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

V_{CC1} = V_{CC2} = 3V

Timing Requirements

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.33. Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	150		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	60		ns

Table 1.5.34. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	600		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	300		ns

Table 1.5.35. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	300		ns
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	150		ns

Table 1.5.36. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAi_{IN} input LOW pulse width	150		ns

Table 1.5.37. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	3000		ns
$t_{w(UPH)}$	TAi_{OUT} input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAi_{OUT} input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	600		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	600		ns

Table 1.5.38. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAi_{OUT} input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAi_{IN} input setup time	500		ns

V_{CC1} = V_{CC2} = 3V

Timing Requirements

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.39. Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width (counted on both edges)	120		ns

Table 1.5.40. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	600		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	300		ns

Table 1.5.41. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time	600		ns
$t_{w(TBH)}$	TBi_{IN} input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBi_{IN} input LOW pulse width	300		ns

Table 1.5.42. A-D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	200		ns

Table 1.5.43. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TxDi output delay time		160	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	50		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 1.5.44. External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

$V_{CC1} \geq V_{CC2}$ = 3V

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.45. Memory Expansion, Microprocessor Modes (for setting with no wait)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.5.11		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			30	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

f(BCLK) is 12.5MHz or less.

Note 2: Calculated according to the BCLK frequency as follows:

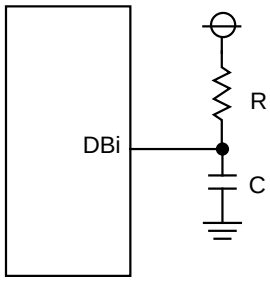
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$t = -CR \times \ln (1 - V_{OL} / V_{CC2})$

by a circuit of the right figure.
For example, when $V_{OL} = 0.2V_{CC2}$, C = 30pF, R = 1kΩ, hold time of output "L" level is

$t = -30pF \times 1k\Omega \times \ln (1 - 0.2V_{CC2} / V_{CC2})$
$= 6.7ns.$



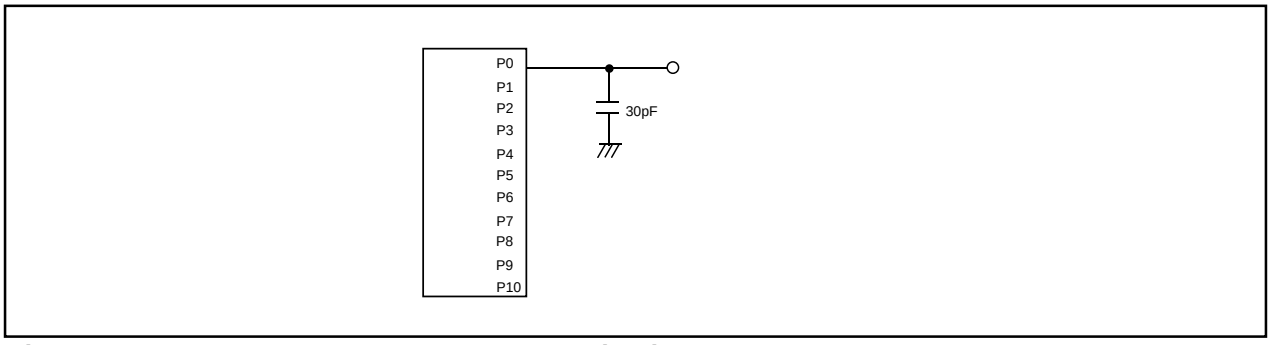


Figure 1.5.11. Ports P0 to P10 Measurement Circuit

$V_{CC1} \geq V_{CC2}$ = 3V

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 1.5.46. Memory expansion and Microprocessor Modes
(for 1- to 3-wait setting and external area access)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.5.11		30	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		0		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 2)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			30	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time			30	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time		–4		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			30	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			30	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)(Note 3)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 1)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)(Note 3)		(Note 2)		ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

n is “1” for 1-wait setting, “2” for 2-wait setting and “3” for 3-wait setting.
When n=1, f(BCLK) is 12.5MHz or less.

Note 2: Calculated according to the BCLK frequency as follows:

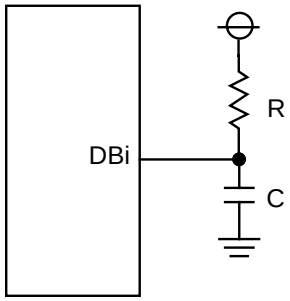
$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

Note 3: This standard value shows the timing when the output is off, and does not show hold time of data bus.
Hold time of data bus varies with capacitor volume and pull-up (pull-down) resistance value.
Hold time of data bus is expressed in

$t = -CR \times \ln (1 - V_{OL} / V_{CC2})$

by a circuit of the right figure.
For example, when V_{OL} = 0.2V_{CC2}, C = 30pF, R = 1kΩ, hold time of output “L” level is

$t = -30pF \times 1k\Omega \times \ln (1 - 0.2V_{CC2} / V_{CC2})$
$= 6.7ns.$



$V_{CC1} \geq V_{CC2}$ = 3V

Switching Characteristics

(V_{CC1} = V_{CC2} = 3V, V_{SS} = 0V, at Topr = – 20 to 85°C / – 40 to 85°C, unless otherwise specified)

Table 1.5.47. Memory expansion and Microprocessor Modes
(for 2- to 3-wait setting, external area access and multiplex bus selection)

Symbol	Parameter	Measuring condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address output delay time	Figure 1.5.11		50	ns
$t_{h(BCLK-AD)}$	Address output hold time (refers to BCLK)		4		ns
$t_{h(RD-AD)}$	Address output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-AD)}$	Address output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip select output delay time			50	ns
$t_{h(BCLK-CS)}$	Chip select output hold time (refers to BCLK)		4		ns
$t_{h(RD-CS)}$	Chip select output hold time (refers to RD)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip select output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD signal output delay time			40	ns
$t_{h(BCLK-RD)}$	RD signal output hold time		0		ns
$t_{d(BCLK-WR)}$	WR signal output delay time			40	ns
$t_{h(BCLK-WR)}$	WR signal output hold time		0		ns
$t_{d(BCLK-DB)}$	Data output delay time (refers to BCLK)			50	ns
$t_{h(BCLK-DB)}$	Data output hold time (refers to BCLK)		4		ns
$t_{d(DB-WR)}$	Data output delay time (refers to WR)		(Note 2)		ns
$t_{h(WR-DB)}$	Data output hold time (refers to WR)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE signal output delay time (refers to BCLK)			40	ns
$t_{h(BCLK-ALE)}$	ALE signal output hold time (refers to BCLK)		– 4		ns
$t_{d(AD-ALE)}$	ALE signal output delay time (refers to Address)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE signal output hold time (refers to Adderss)		(Note 4)		ns
$t_{d(AD-RD)}$	RD signal output delay from the end of Address		0		ns
$t_{d(AD-WR)}$	WR signal output delay from the end of Address		0		ns
$t_{dZ(RD-AD)}$	Address output floating start time			8	ns

Note 1: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 10 \quad [ns]$$

Note 2: Calculated according to the BCLK frequency as follows:

$$\frac{(n-0.5) \times 10^9}{f(BCLK)} - 50 \quad [ns]$$

n is “2” for 2-wait setting, “3” for 3-wait setting.

Note 3: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 40 \quad [ns]$$

Note 4: Calculated according to the BCLK frequency as follows:

$$\frac{0.5 \times 10^9}{f(BCLK)} - 15 \quad [ns]$$

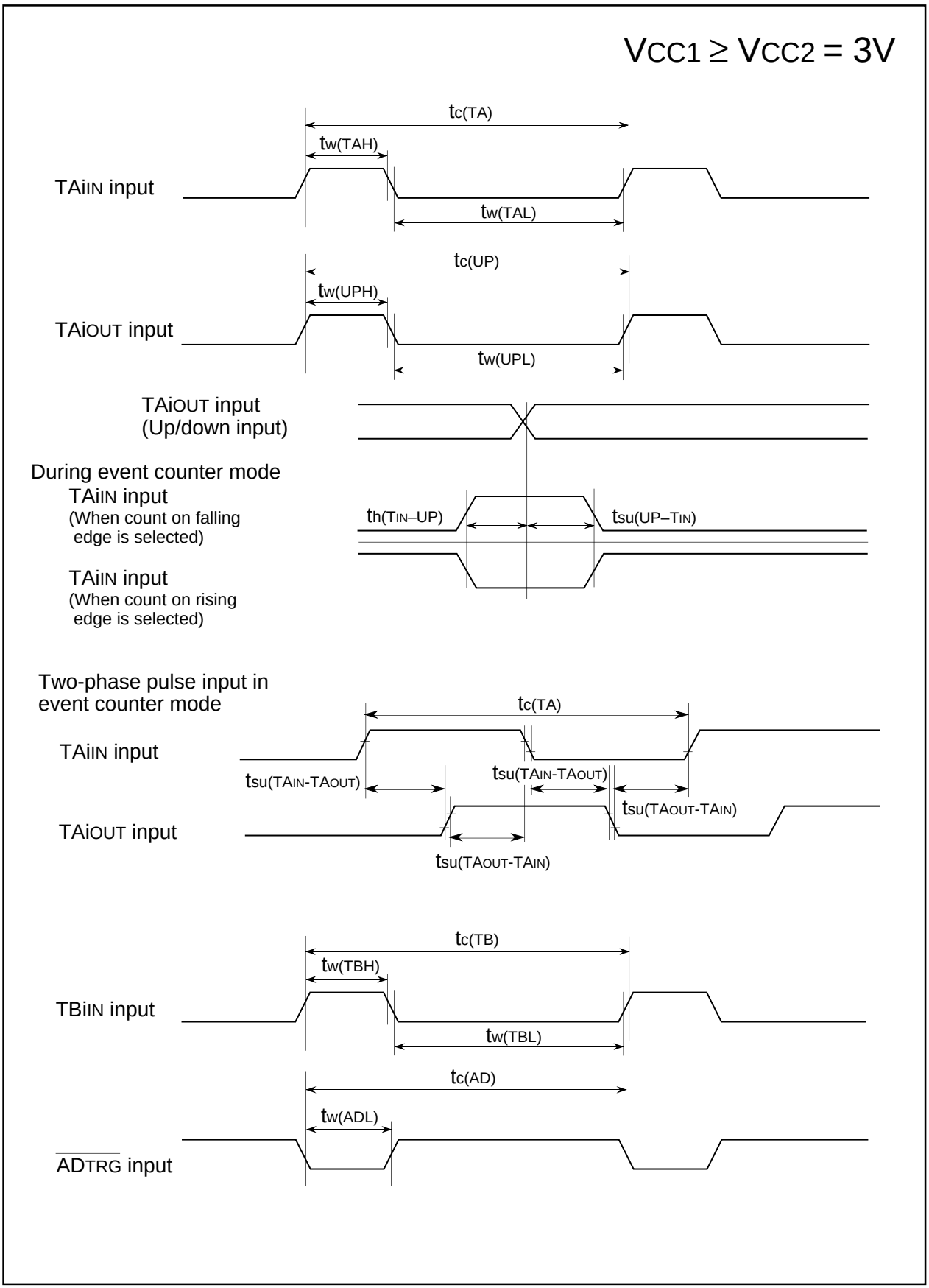


Figure 1.5.12. Timing Diagram (1)

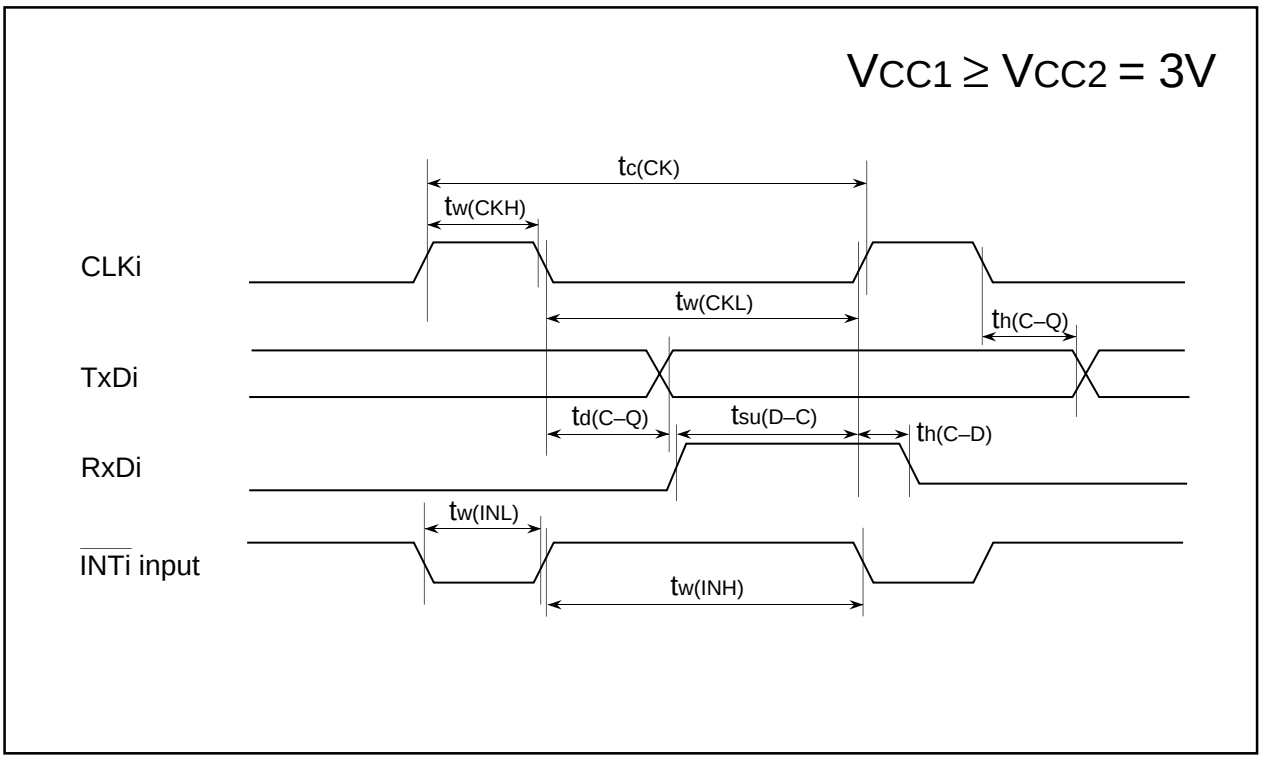
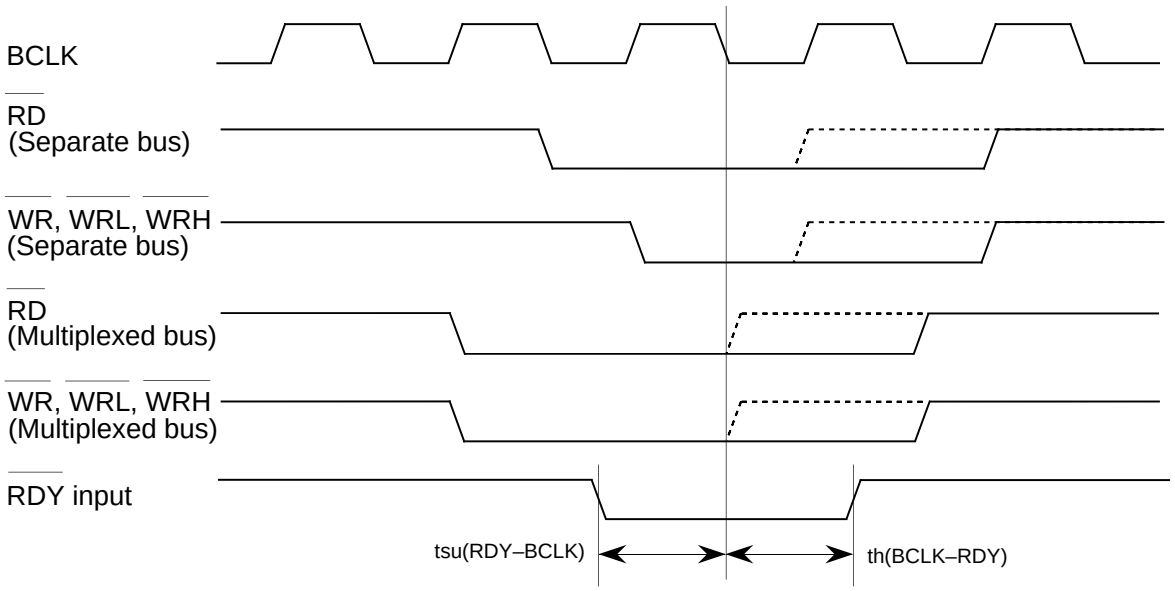


Figure 1.5.13. Timing Diagram (2)

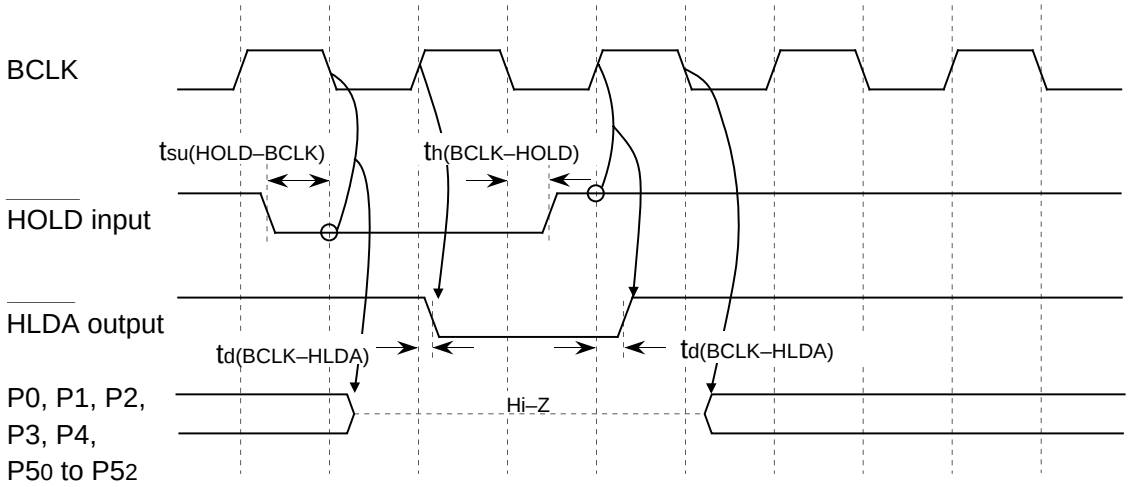
$V_{CC1} \geq V_{CC2}$ = 3V

Memory Expansion Mode, Microprocessor Mode

(Effective for setting with wait**)**



(Common to setting with wait and setting without wait**)**



Note: The above pins are set to high-impedance regardless of the input level of the BYTE pin, PM06 bit of PM0 register and PM11 bit of PM1 register.

Measuring conditions :

- V_{CC1}=V_{CC2}=3V
- Input timing voltage : Determined with V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : Determined with V_{OL}=1.5V, V_{OH}=1.5V

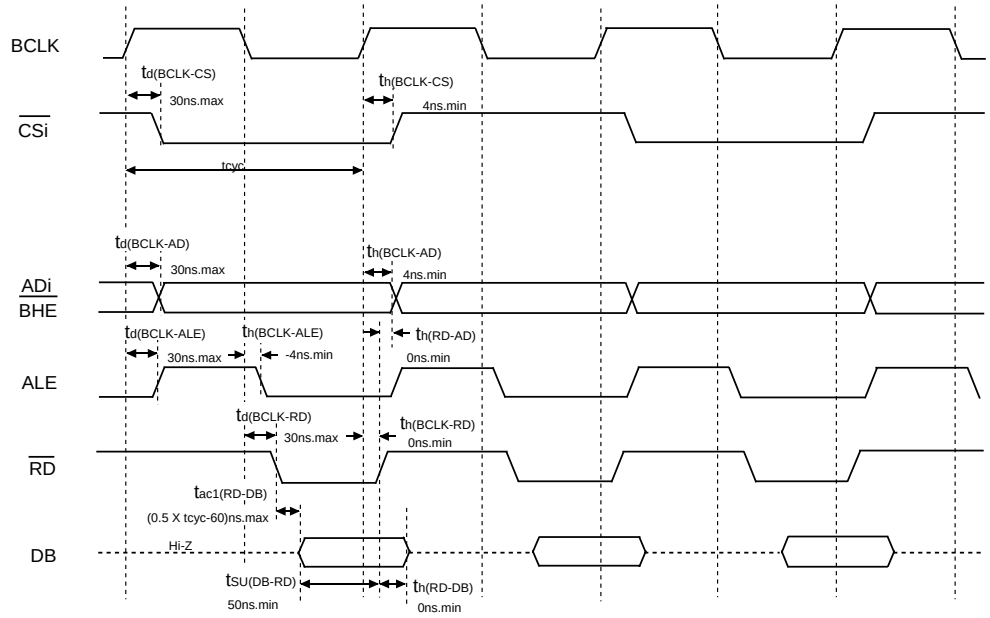
Figure 1.5.14. Timing Diagram (3)

$V_{CC1} \geq V_{CC2}$ = 3V

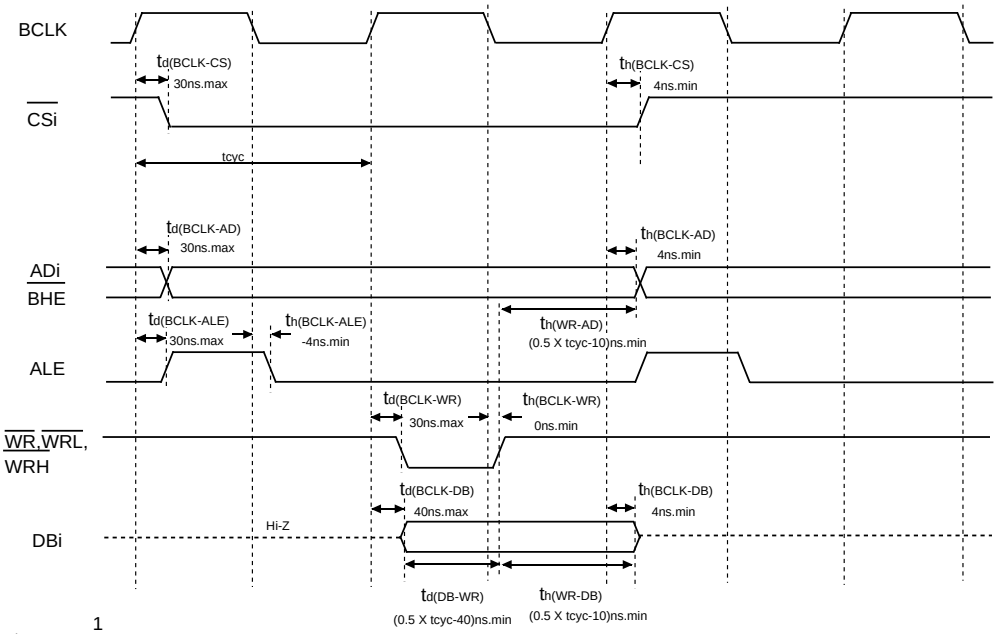
Memory Expansion Mode, Microprocessor Mode

(For setting with no wait**)**

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

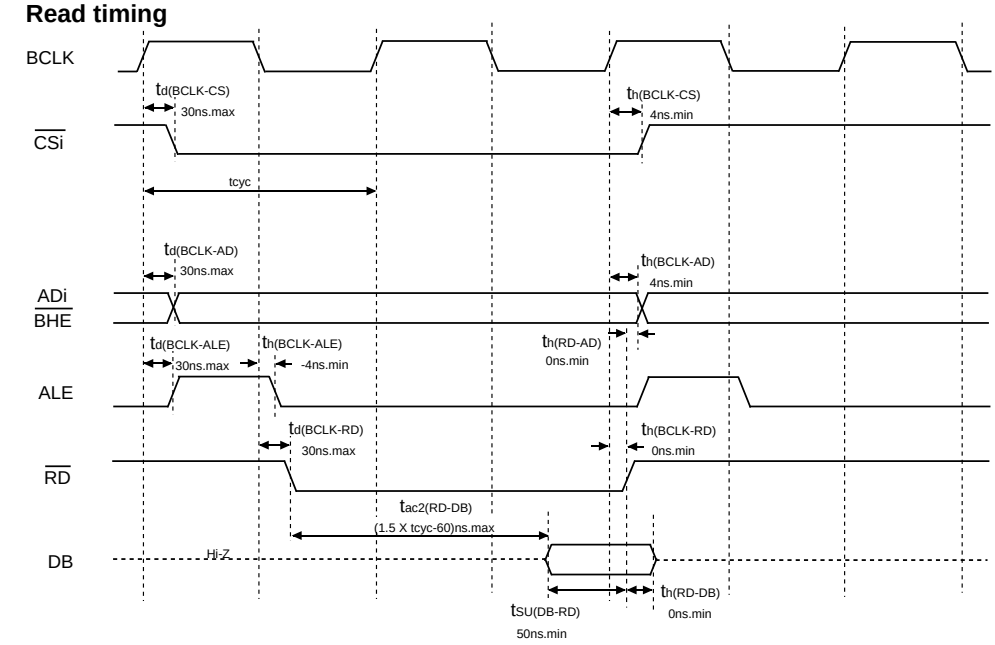
Figure 1.5.15. Timing Diagram (4)

$V_{CC1} \geq V_{CC2}$ = 3V

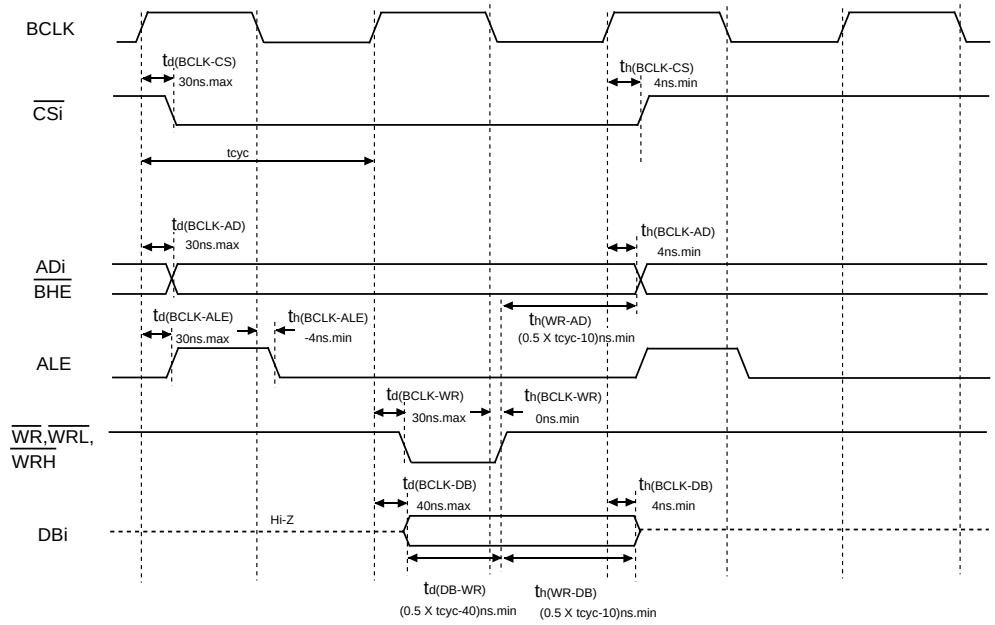
Memory Expansion Mode, Microprocessor Mode

(for 1-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

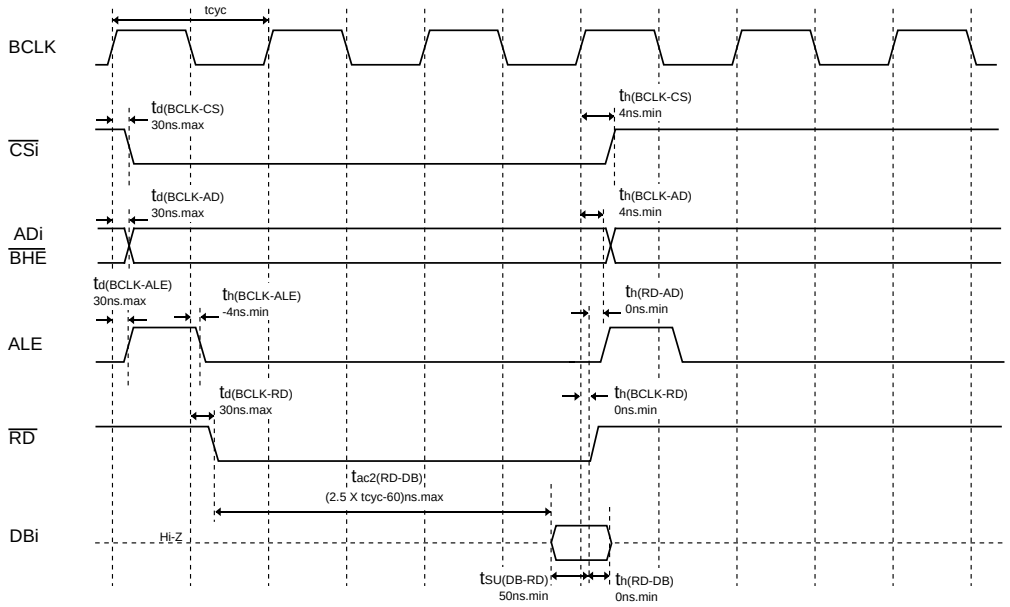
Figure 1.5.16. Timing Diagram (5)

$V_{CC1} \geq V_{CC2} = 3V$

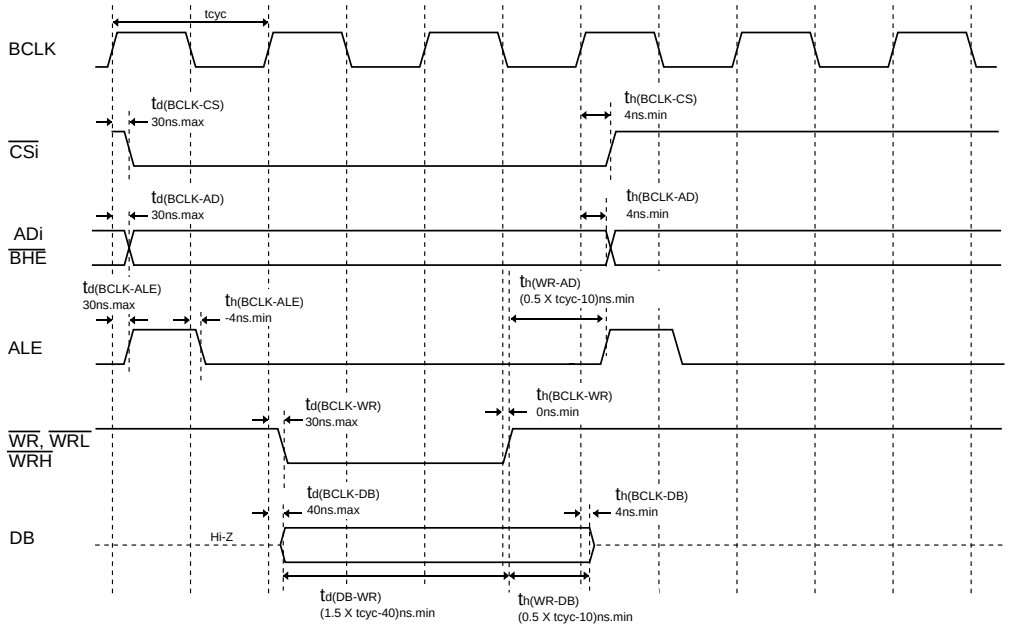
Memory Expansion Mode, Microprocessor Mode

(for 2-wait setting and external area access**)**

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions

- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

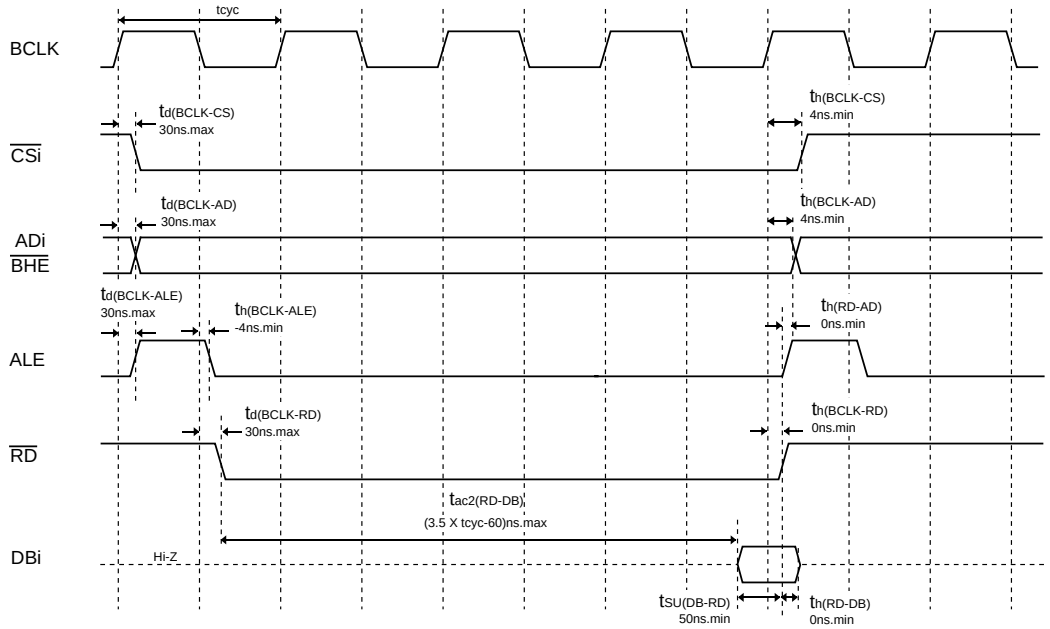
Figure 1.5.17. Timing Diagram (6)

$V_{CC1} \geq V_{CC2}$ = 3V

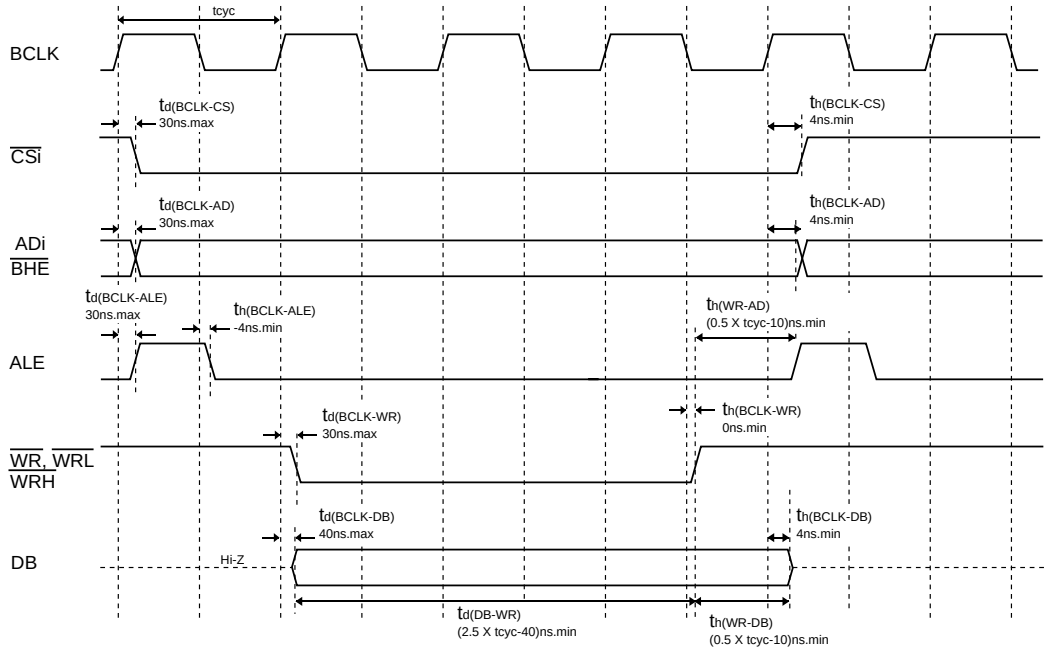
Memory Expansion Mode, Microprocessor Mode

(for 3-wait setting and external area access)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

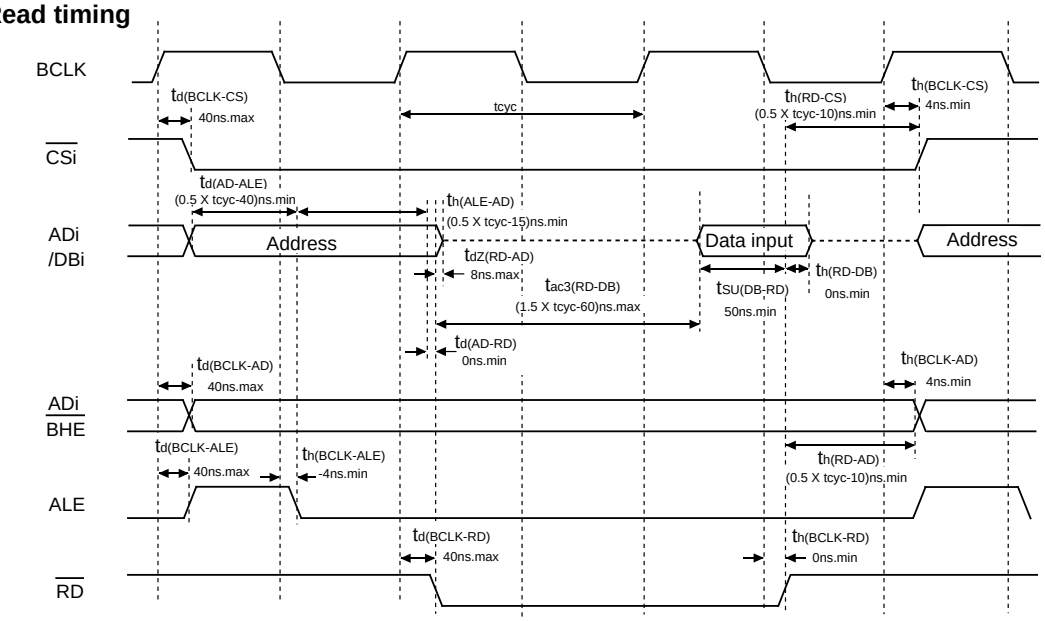
Figure 1.5.18. Timing Diagram (7)

$V_{CC1} \geq V_{CC2} = 3V$

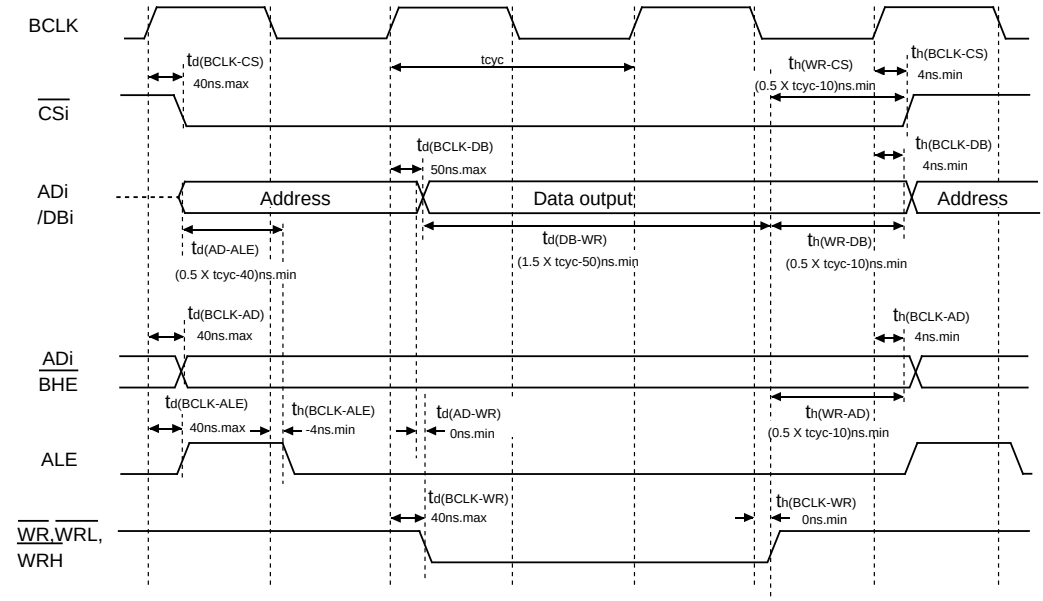
Memory Expansion Mode, Microprocessor Mode

(For 2-wait setting, external area access and multiplex bus selection)

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

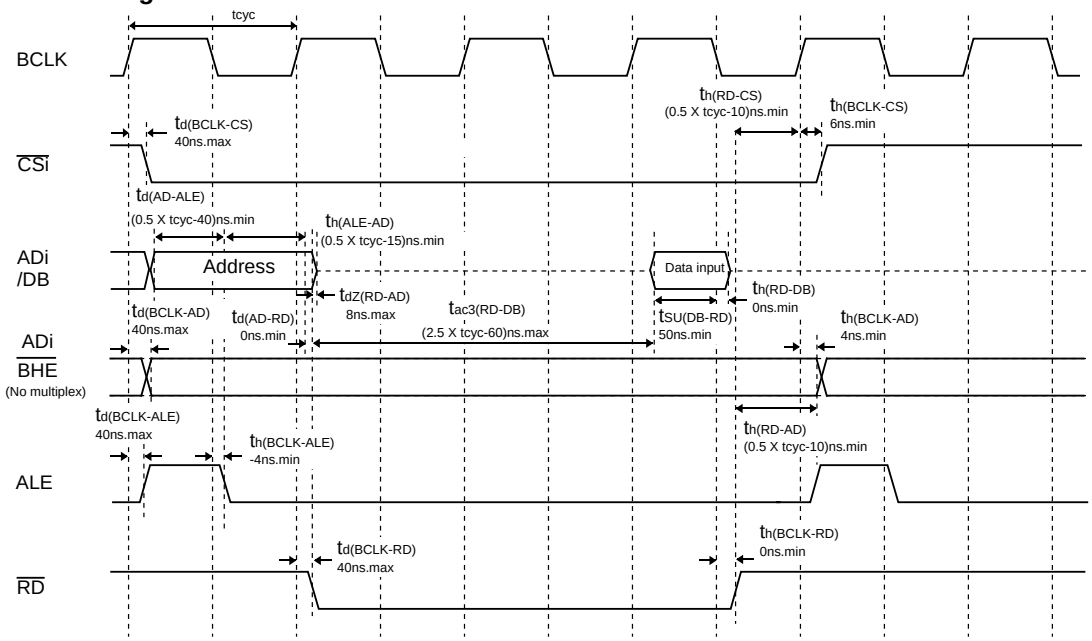
Figure 1.5.19. Timing Diagram (8)

$V_{CC1} \geq V_{CC2} = 3V$

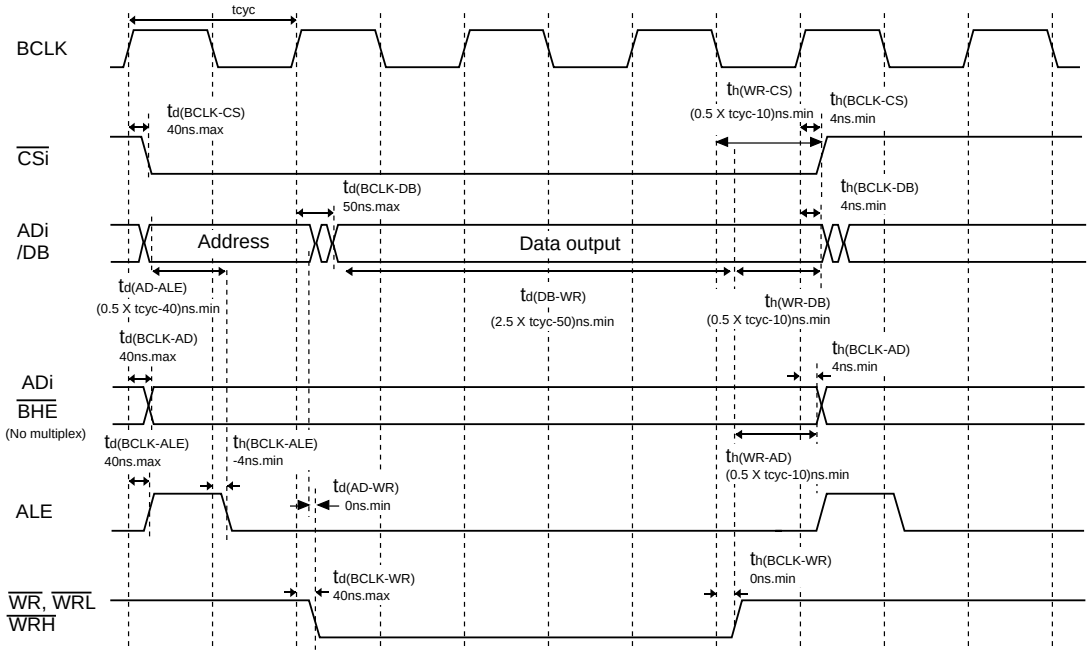
Memory Expansion Mode, Microprocessor Mode

(For 3-wait setting, external area access and multiplex bus selection**)**

Read timing



Write timing



$$tcyc = \frac{1}{f(BCLK)}$$

Measuring conditions
- V_{CC1}=V_{CC2}=3V
- Input timing voltage : V_{IL}=0.6V, V_{IH}=2.4V
- Output timing voltage : V_{OL}=1.5V, V_{OH}=1.5V

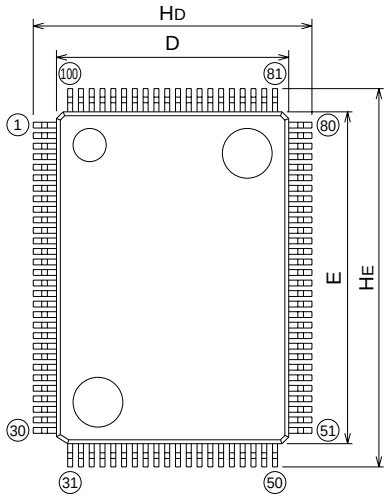
Figure 1.5.20. Timing Diagram (9)

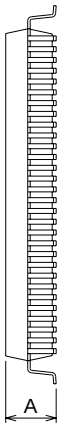
Package Dimensions

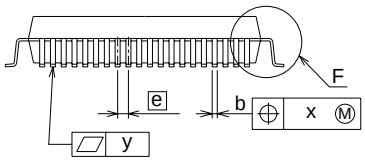
100P6S-A (MMP)

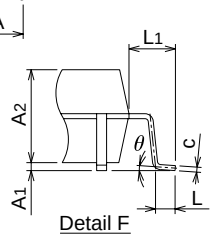
Plastic 100pin 14×20mm body QFP

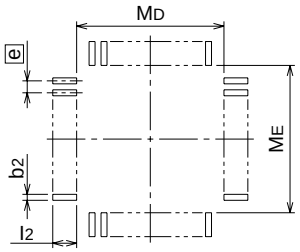
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42











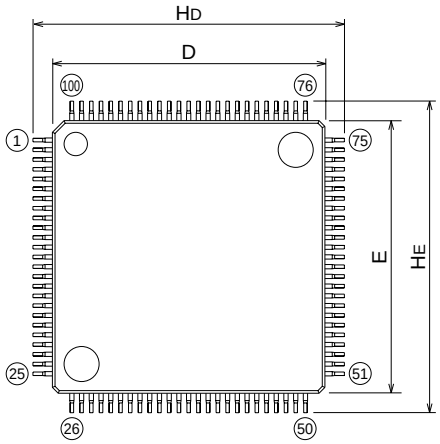
Recommended Mount Pad

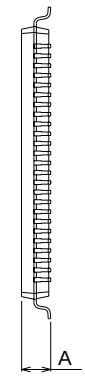
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

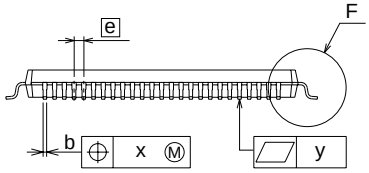
100P6Q-A (MMP)

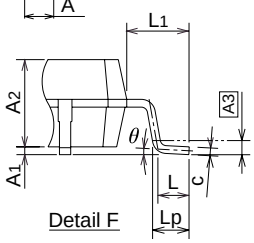
Plastic 100pin 14×14mm body LQFP

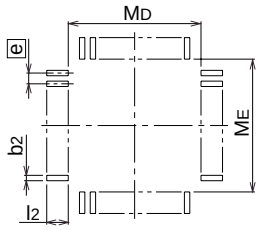
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–	0.63	Cu Alloy











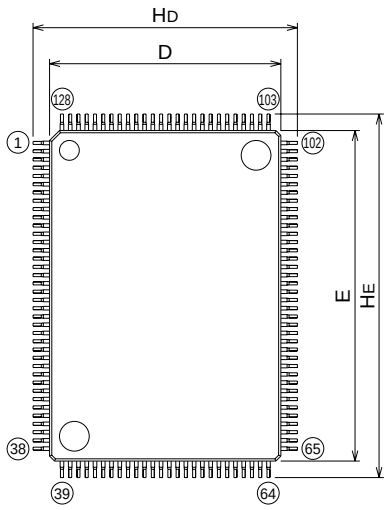
Recommended Mount Pad

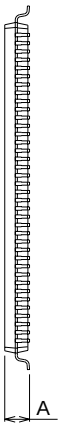
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	14.4	–
ME	–	14.4	–

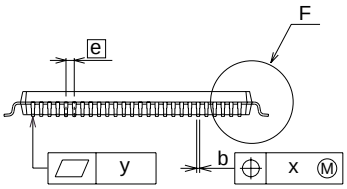
128P6Q-A (MMP)

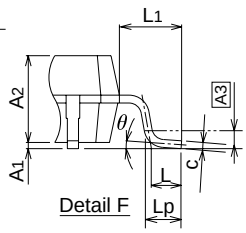
Plastic 128pin 14×20mm body LQFP

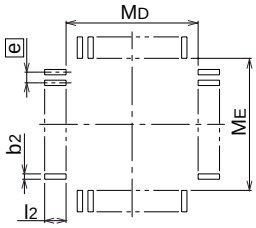
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	–	–	Cu Alloy











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.4	1.5	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	–	1.0	–
MD	–	14.4	–
ME	–	20.4	–

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Rev.	Date	Description	
		Page	Summary
1.10	Apr/XX/Y03 (Continued)	2	Table 1.1.1 is partly revised.
		4-5	Table 1.1.2 and 1.1.3 is partly revised.
		14-19	SFR is partly revised.
			“Note 1” is partly revised.
		22	Table 1.5.3 is partly revised.
		23	Table 1.5.5 is partly revised.
			Table 1.5.6 is added.
		24	Table 1.5.9 is partly revised.
		30	Notes 1 and 2 in Table 1.5.26 is partly revised.
		31	Notes 1 in Table 1.5.27 is partly revised.
		30-31	Note 3 is added to “Data output hold time(refers to BCLK)” in Table 1.5.26 and 1.5.27.
		32	Note 4 is added to “th(ALE-AD)” in Table 1.5.28.
		30-32	Switching Characteristics is partly revised.
		36-39	th(WR-AD) and th(WR-DB) in Figure 1.5.5 to 1.5.8 is partly revised.
		40-41	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.9 to 1.5.10 is partly revised.
		42	Note 2 is added to Table 1.5.29.
		47	Notes 1 and 2 in Table 1.5.45 is partly revised.
		48	Notes 1 in Table 1.5.46 is partly revised.
		47-48	Note 3 is added to “Data output hold time(refers to BCLK)” in Table 1.5.45 and 1.5.46.
		49	Note 4 is added to “th(ALE-AD)” in Table 1.5.47.
		47-49	Switching Characteristics is partly revised.
		53-56	th(WR-AD) and th(WR-DB) in Figure 1.5.15 to 1.5.18 is partly revised.
		57-58	th(ALE-AD), th(WR-CS), th(WR-DB) and th(WR-AD) in Figure 1.5.19 to 1.5.20 is partly revised.