M5M411664AJ,TP1-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1048576-BIT (65536-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 65536-word by 16-bit dynamic RAMs, fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation,and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is small enough for battery back-up application.

This device has 2$\overline{W}$ and 1$\overline{CAS}$ terminals with a refresh cycle of 256 cycles every 4ms.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M411664AXX-5,-5S	50	13	25	13	90	625
M5M411664AXX-6,-6S	60	15	30	15	110	550
M5M411664AXX-7,-7S	70	20	35	20	130	475

XX=J, TP1

- AJ:40pin SOJ/400mil, ATP1: 42 pin TSOP(II)/300mil
- Single 5V±10% supply
- Low stand-by power dissipation
  - CMOS Input level ..... 5.5 mW(Max)
  - CMOS Input level ..... 550 μW(Max) *
- Operating power dissipation
  - M5M411664Axx -5,-5S ..... 688 mW(Max)
  - M5M411664Axx -6,-6S ..... 605 mW(Max)
  - M5M411664Axx -7,-7S ..... 523 mW(Max)
- Self refresh capability *
  - Self refresh current ..... 150 μA(max)
- Extended refresh capability
  - Extended refresh current ..... 150 μA(max)
- Fast-page mode (256-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- 256 refresh cycles every 4ms (A_0~A_7)
- 256 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles every 32ms (A_0~A_7) * for extended refresh
- Byte control for Read / Write operation(2$\overline{W}$,1$\overline{CAS}$ type)

*:Applicable to self refresh version (M5M411664AXX-5S,-6S,-7S :option) only

APPLICATION

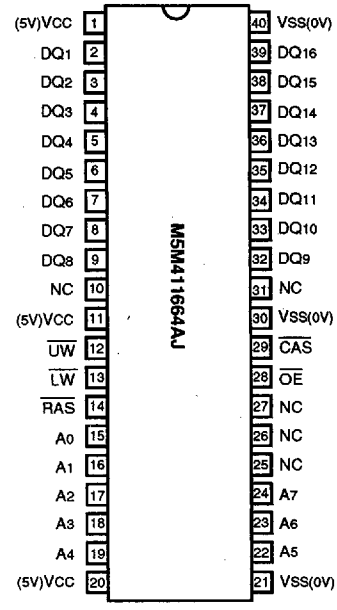
Microcomputer memory, Refresh memory for CRT, Frame Buffer memory for CRT.

PIN DESCRIPTION

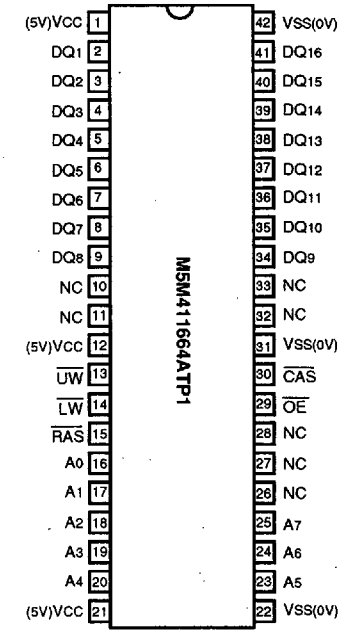
Pin Name	Function
A_0~A_7	Address Inputs
DQ_1~DQ_{16}	Data Inputs/Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
$\overline{LW}$	Lower Byte Control Write Control Input
$\overline{UW}$	Upper Byte Control Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

M5M411664AJ,TP1-5,-5S:Under development

PIN CONFIGURATION (TOP VIEW)



Outline 40P0K (40pin 400mil SOJ)



Outline 42P3U-E (42pin 300mil TSOP)

NC : NO CONNECTION

FUNCTION

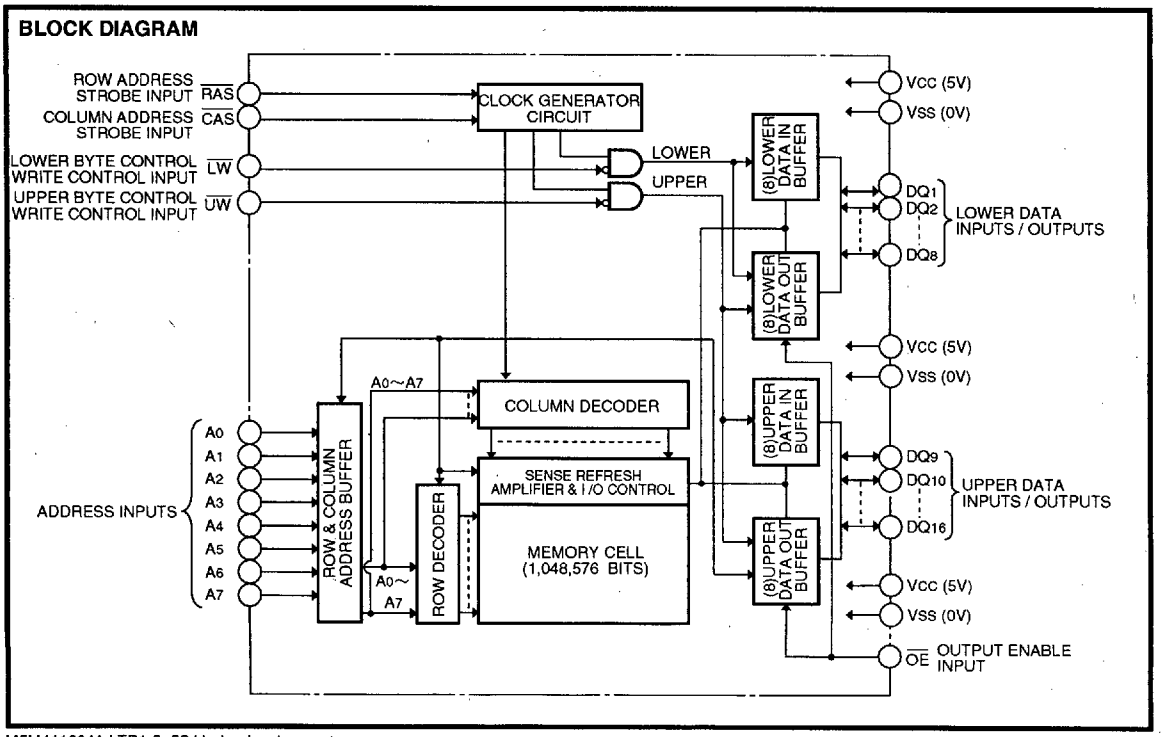
In addition to normal read,write, and read-modify-write operations the M5M411664ATP1,AJ provides a number of other functions,e.g., Fast page mode, $\overline{RAS}$-only refresh,and delayed-write.
The input conditions for each are shown in Table 1.

Table 1. Input conditions for each mode

Operation	Inputs							Input / Output				Refresh	Remark
								Lower		Upper			
	$\overline{RAS}$	$\overline{LW}$	$\overline{UW}$	$\overline{CAS}$	$\overline{OE}$	Row address	Column address	D	Q	D	Q		
Read	ACT	NAC	NAC	ACT	ACT	APD	APD	OPN	VLD	OPN	VLD	YES	Fast-page mode identical
Early write	ACT	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper early	ACT	NAC	ACT	ACT	DNC	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower early	ACT	ACT	NAC	ACT	DNC	APD	APD	VLD	OPN	DNC	OPN	YES	
Delayed write	ACT	ACT	ACT	ACT	ACT	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper delayed	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower delayed	ACT	ACT	NAC	ACT	ACT	APD	APD	VLD	OPN	DNC	OPN	YES	
Read-modify-W	ACT	ACT	ACT	ACT	ACT	APD	APD	VLD	OPN	VLD	OPN	YES	
Upper RMW	ACT	NAC	ACT	ACT	ACT	APD	APD	DNC	OPN	VLD	OPN	YES	
Lower RMW	ACT	ACT	NAC	ACT	ACT	APD	APD	VLD	OPN	DNC	OPN	YES	
$\overline{RAS}$ only-R	ACT	DNC	DNC	NAC	DNC	APD	DNC	DNC	OPN	DNC	OPN	YES	
Hidden refresh	ACT	NAC	NAC	ACT	ACT	DNC	DNC	OPN	VLD	OPN	VLD	YES	
CBR refresh (Extended)	ACT	DNC	DNC	ACT	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Self Refresh*	ACT	DNC	DNC	ACT	DNC	DNC	DNC	DNC	OPN	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	DNC	OPN	NO	

Note : ACT; active , DNC ; don't care, VLD ; valid, IVD ; invalid, APD ; applied, OPN ; open, NAC; nonactive

BLOCK DIAGRAM



M5M411664AJ,TP1-5,-5S:Under development

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1~7	V
V_I	Input voltage		-1~7	V
V_O	Output voltage		-1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0 ~70	℃
T_{stg}	Storage temperature		-65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-0.5 **		0.8	V

Note 1 : All voltage values are with respect to Vss.
** : V_{IL}(min) is -2.0V when pulse width is less than 25ns. (pulse width is with respect to Vss.)

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditons	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} =-2.5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} =2.1mA	0		0.4	V
I_{OZ}	Off-state output voltage		Q floating, 0V≦V_{OUT}≦5.5V	-10		10	μA
I_I	Input current		0V≦V_{IH}≦6.0V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc operating (Note 3,4,5)	M5M411664A-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} =min. output open			125	mA
		M5M411664A-6,-6S				110	
		M5M411664A-7,-7S				95	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc-0.5V output open			1.0	
						0.1*	
$I_{CC3(AV)}$	Average supply current from Vcc,$\overline{RAS}$ only refresh mode (Note 3,5)	M5M411664A-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			125	mA
		M5M411664A-6,-6S				110	
		M5M411664A-7,-7S				95	
$I_{CC4(AV)}$	Average supply current from Vcc Fast Page Mode (Note 3,4,5)	M5M411664A-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			125	mA
		M5M411664A-6,-6S				110	
		M5M411664A-7,-7S				95	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M411664A-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			115	mA
		M5M411664A-6,-6S				100	
		M5M411664A-7,-7S				85	
$I_{CC8(AV)}$ *	Average supply current from Vcc Extended-Refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V Ao~A7≦0.2V or ≧Vcc-0.2V DQ = open t_{RC} =125 μs, t_{RAS}=$t_{RAS\ min}$ ~1 μs			150	μA
$I_{CC9(AV)}$ *	Average supply current from Vcc Self-Refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			150	μA

Note 2 : Current flowing into an IC is positive, out is negative.
3 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$, and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate. Address transient between $\overline{RAS}$ and $\overline{CAS}$ happens once or less. Address transient during $\overline{CAS}$ cycle happens once or less.
4 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5 : Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.
M5M411664AJ,TP1-5,-5S:Under development

CAPACITANCE (Ta=0~70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditons	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I =Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ low	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low	(Note 7,9)		50		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$ low	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		13		15		20	ns

Note 6 : An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 4ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 1TTL loads and 50pF.

8 : Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$.

9 : Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10 : Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11 : Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12 : $t_{OEZ(max)}$ and $t_{OFF(max)}$ defines the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq \pm 10\ \mu A$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

M5M411664AJ,TP1-5,-5S:Under development

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0~70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 13,14)

Symbol	Parameter		Limits						Unit
			M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			4		4		4	ms
tREF	Refresh cycle time*			32		32		32	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		20		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13 : The timing requirements are assumed tT=5ns.
14 : VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15 : tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
16 : tRAD(max) is specified as a reference point only. If tRAD≥tRAD(max) and tASC≤tASC(max), access time is controlled exclusively by tAA.
17 : tASC(max) is specified as a reference point only. If tRCD≥tRCD(max) and tASC≥tASC(max), access time is controlled exclusively by tCAC.
18 : Either tDZC or tDZO must be satisfied.
19 : Either tCDD or tODD must be satisfied.
20 : tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 21)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time	25		30		35		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

M5M411664AJ,TP1-5,-5S:Under development

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	8		10		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		ns
t_{WP}	Write pulse width	8		10		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write / read modify write cycle time (Note 22)	126		150		180		ns
t_{RAS}	$\overline{RAS}$ low pulse width	86	10000	100	10000	120	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	49	10000	55	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	86		100		120		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	49		55		70		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	31		35		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	68		80		95		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 23)	43		50		60		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		ns

Note 22 : t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+5t_T$.

23 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for Fast Page Mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast Page Mode read/write cycle time	35		40		45		ns
t_{PRWC}	Fast Page Mode read write/read modify write cycle time	71		80		95		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	85	100000	100	100000	115	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	48		55		65		ns

Note 24 : All previously specified timing requirements and switching characteristics are applicable to their respective Fast Page Mode cycle.
25 : $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
26 : $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

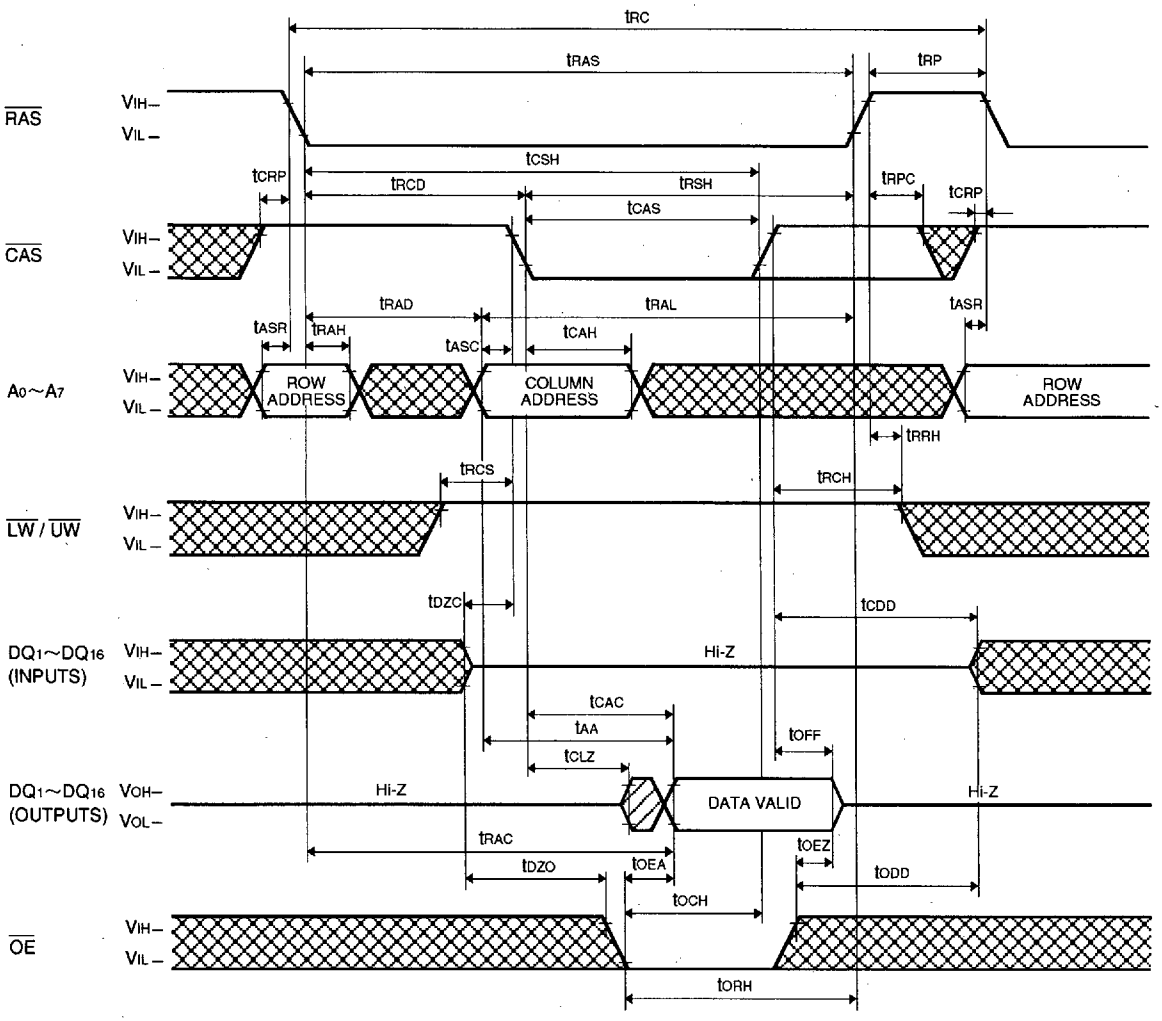
Note 27 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle* (Note 28)

Symbol	Parameter	Limits						Unit
		M5M411664A-5,-5S		M5M411664A-6,-6S		M5M411664A-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	- 50		- 50		- 50		ns

M5M411664AJ,TP1-5,-5S:Under development

Timing Diagrams (Note 29)
Read Cycle



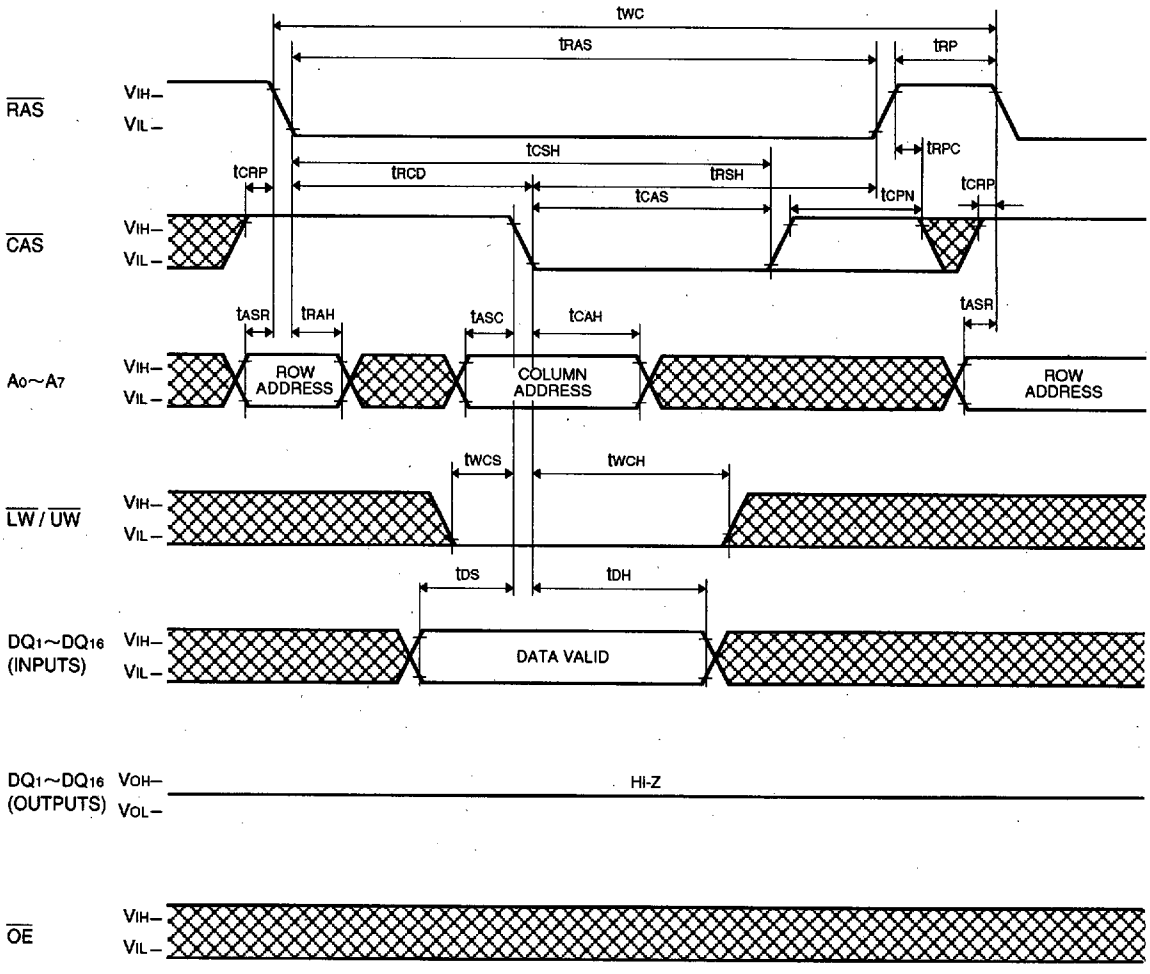
Note 29

Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

Indicates the invalid output.

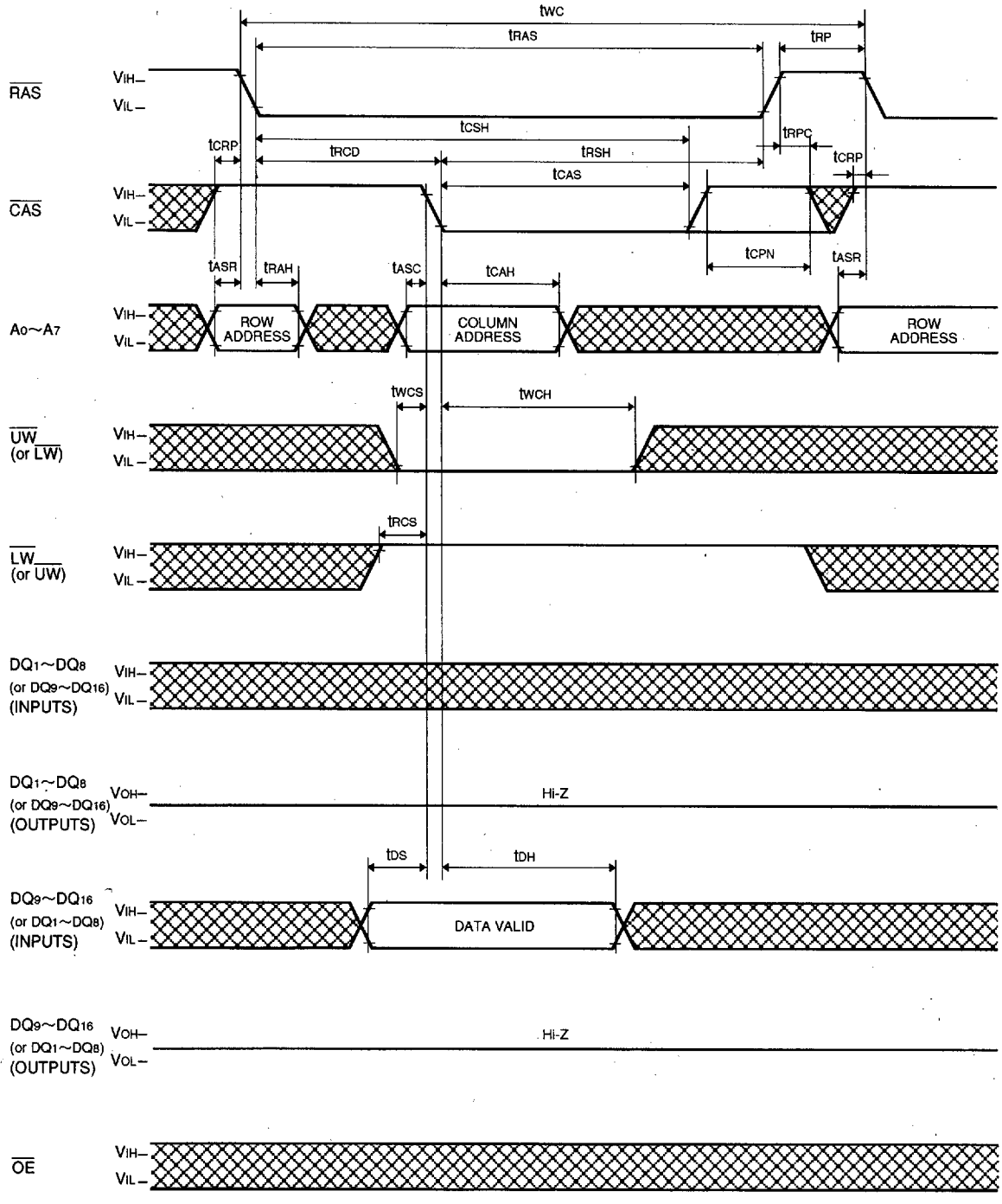
*M5M411664AJ,TP1-5,-5S:Under development

Early Write Cycle



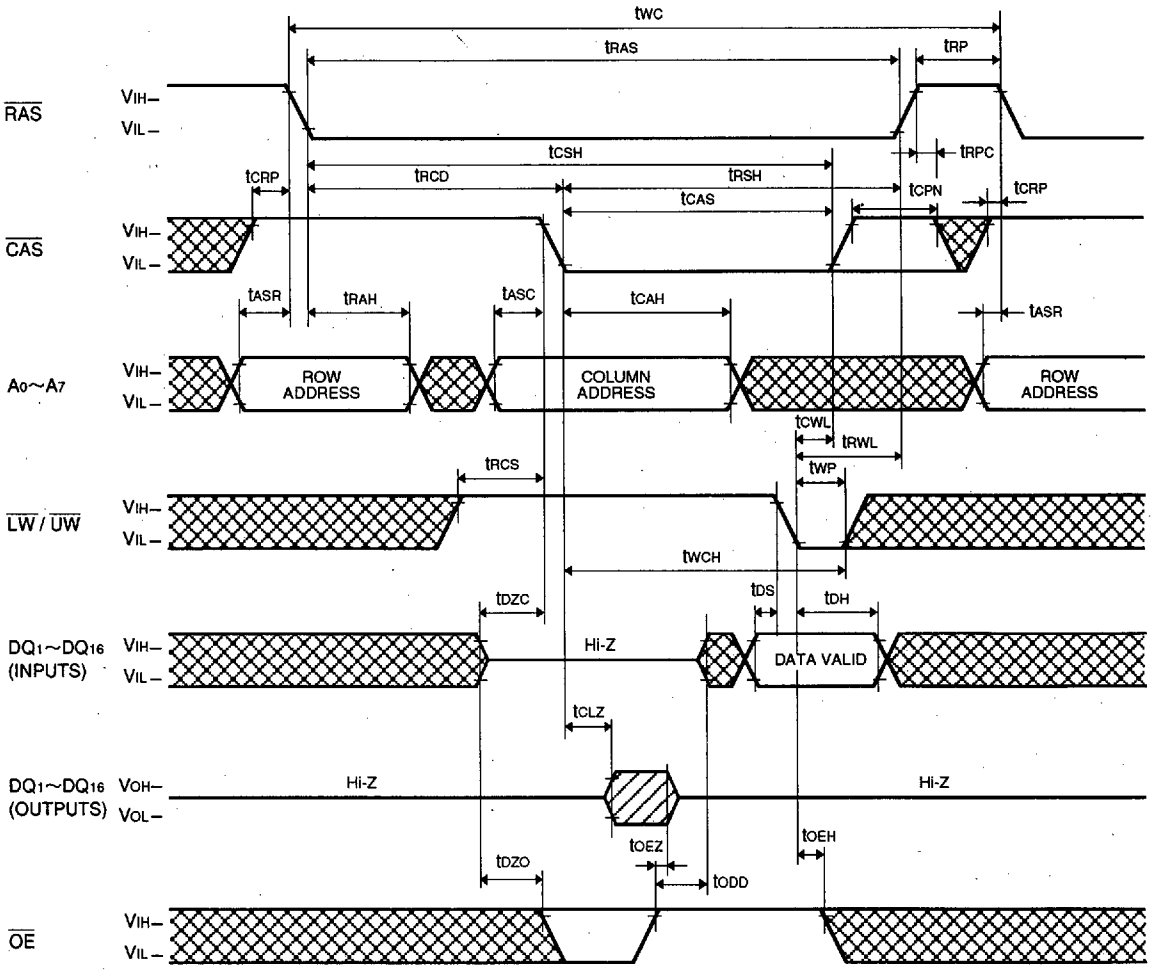
M5M411664AJ,TP1-5,-5S:Under development

Byte Early Write Cycle



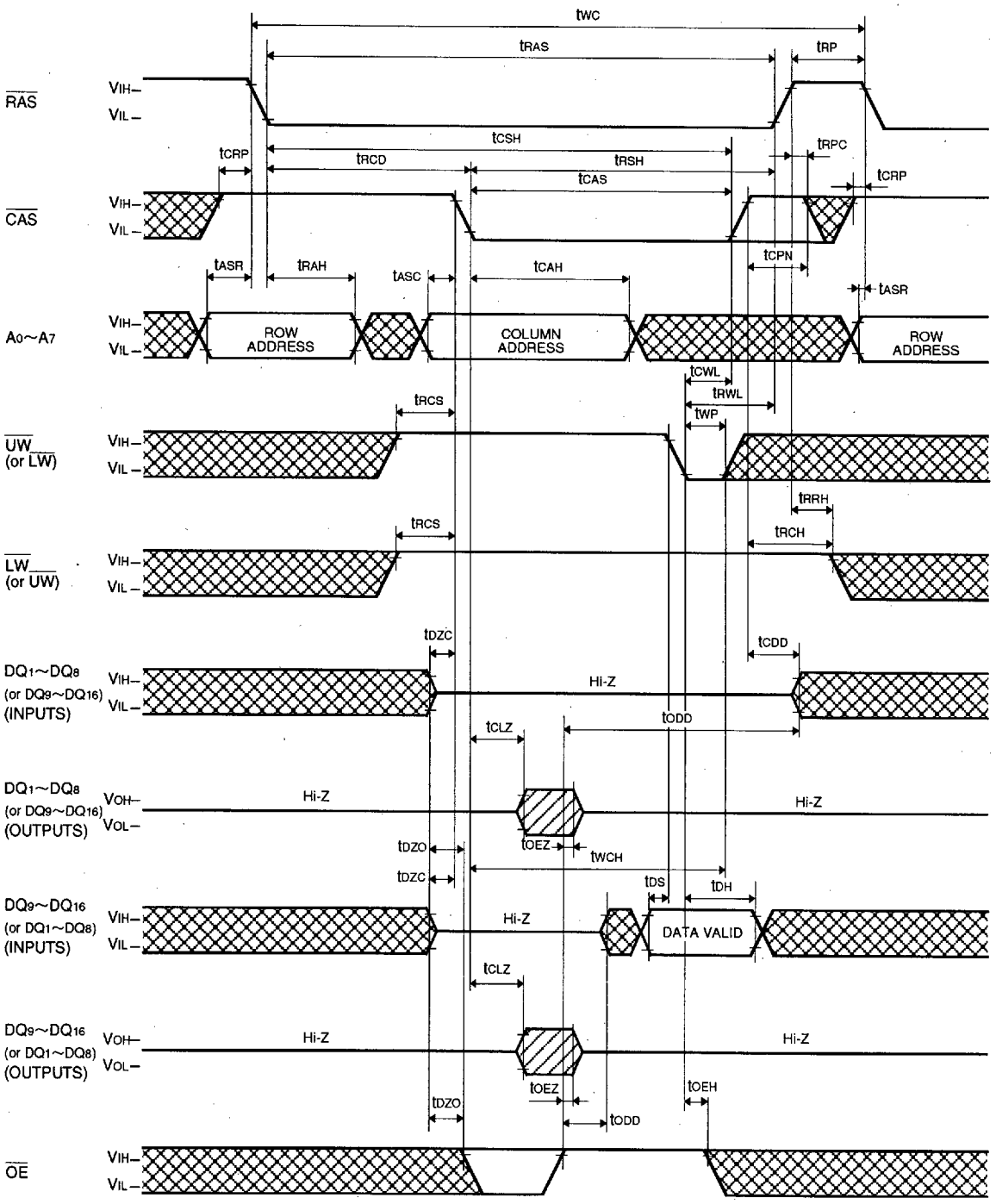
M5M411664AJ,TP1-5,-5S:Under development

Delayed Write Cycle



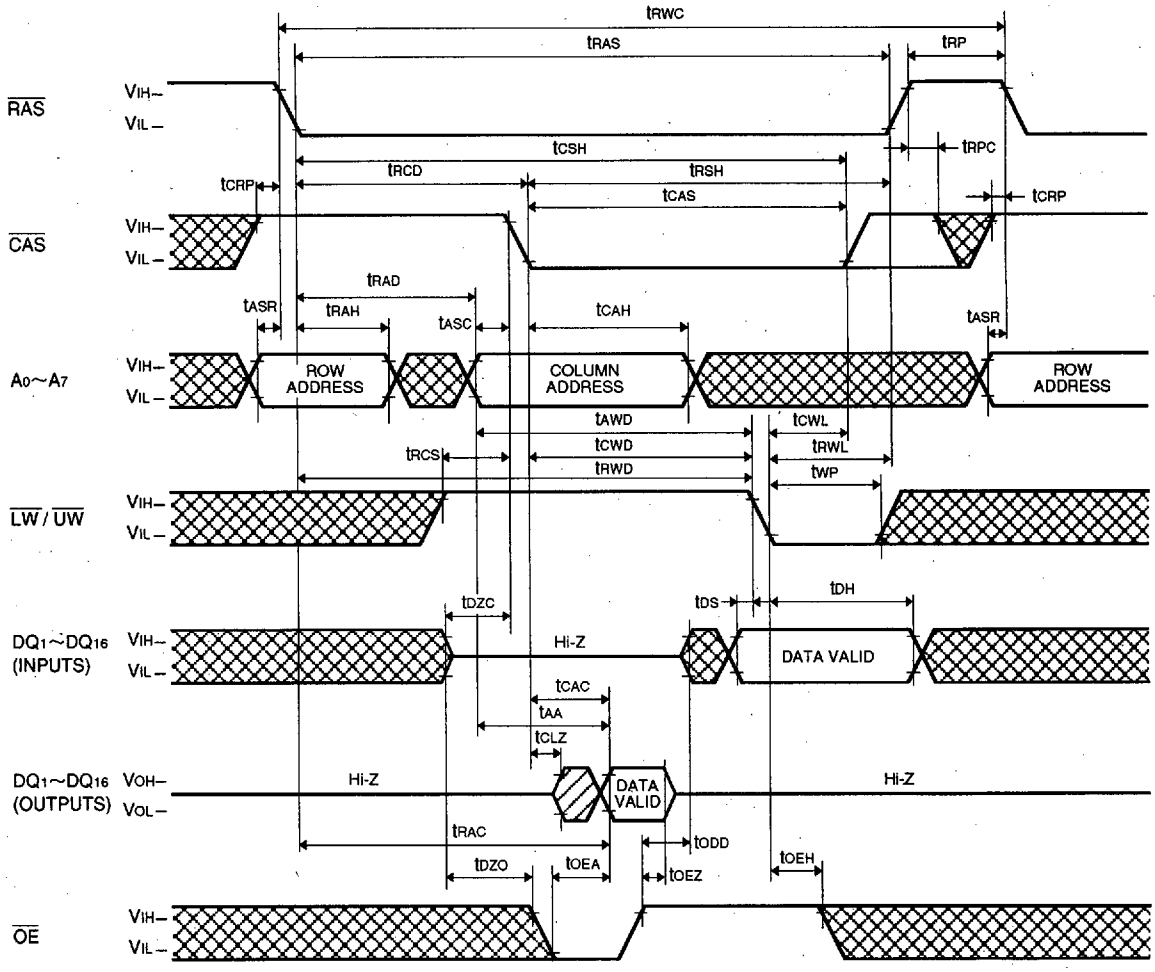
M5M411664AJ,TP1-5,-5S:Under development

Byte Delayed Write Cycle



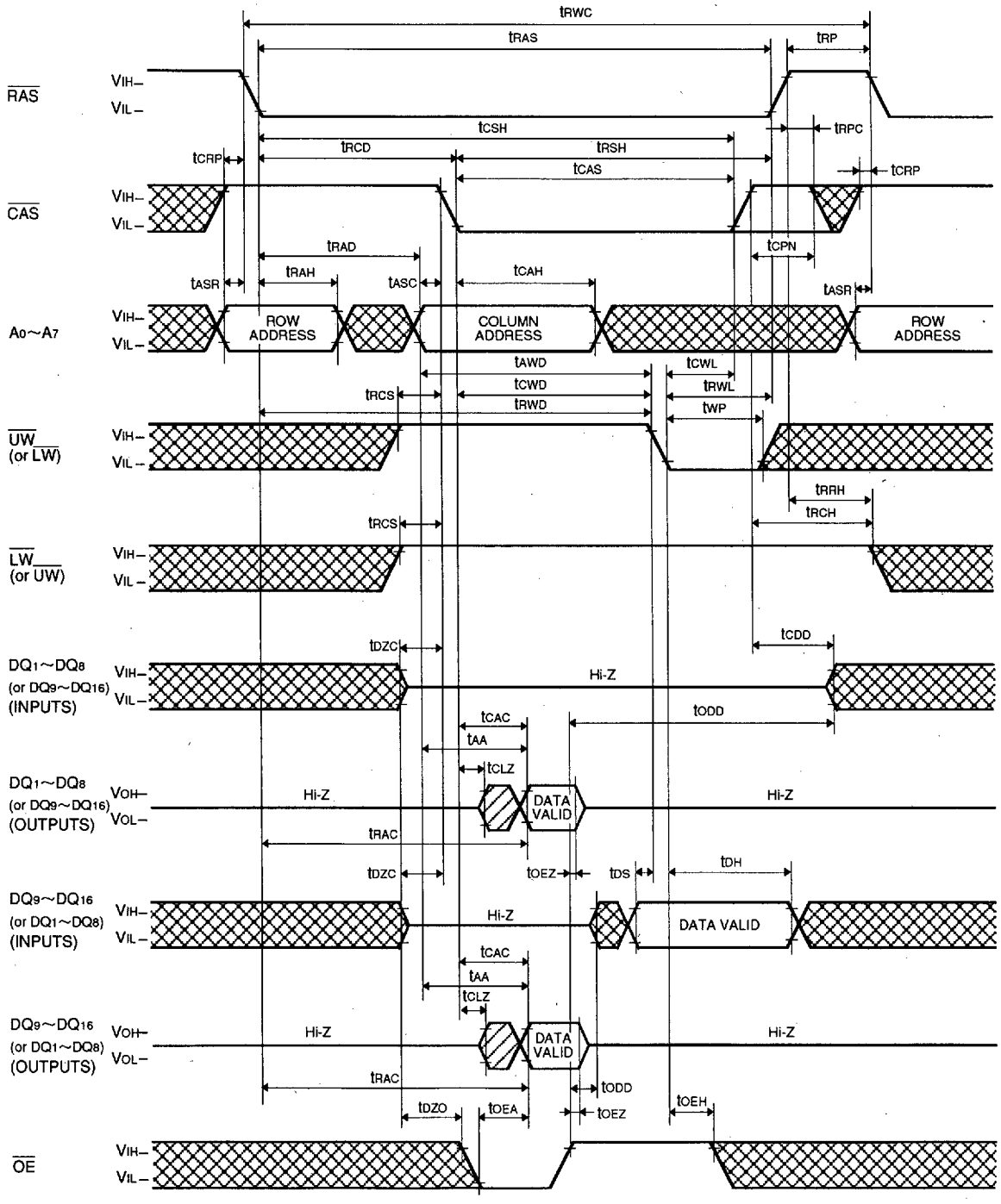
M5M411664AJ,TP1-5,-5S:Under development

Read-Write, Read-Modify-Write Cycle



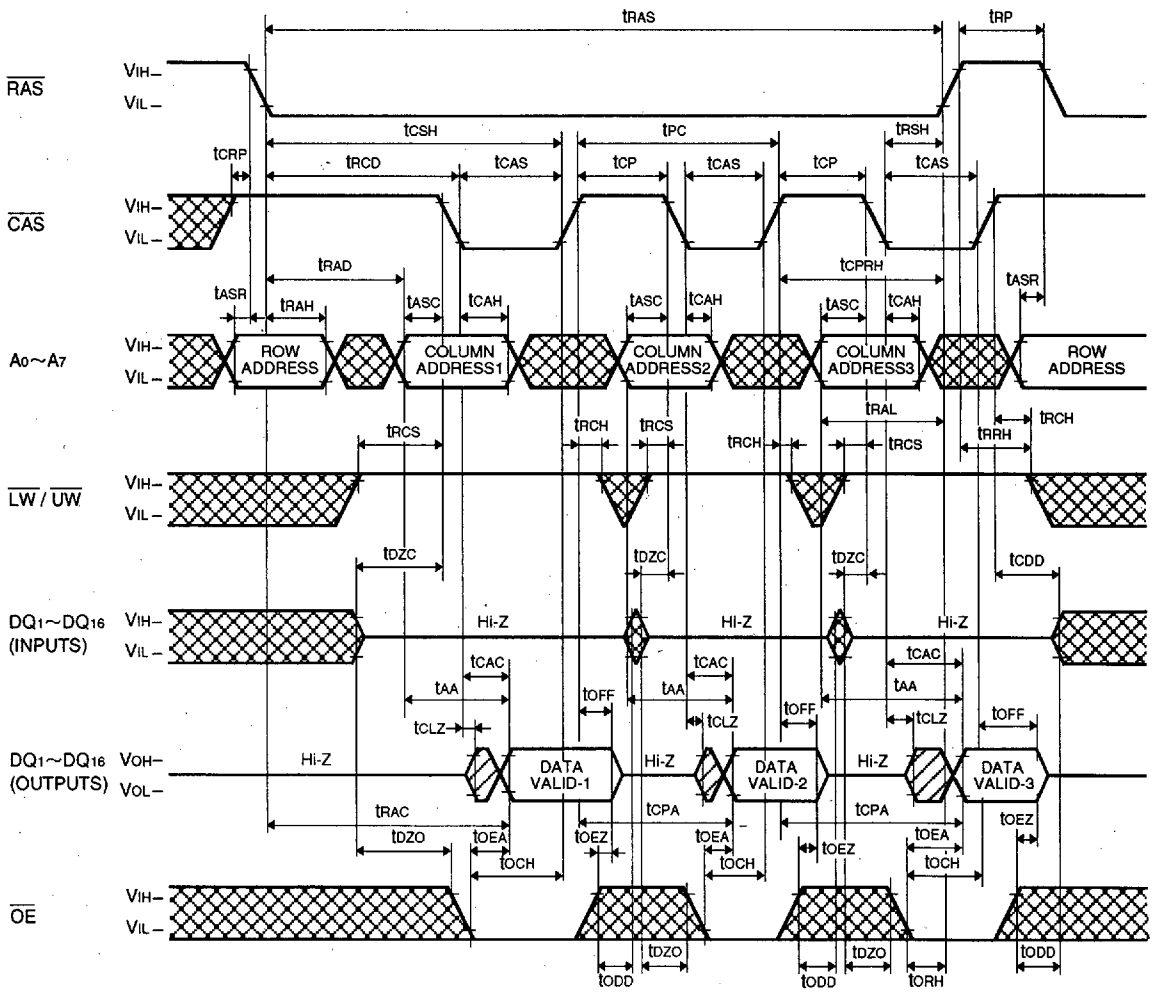
M5M411664AJ,TP1-5,-5S:Under development

Byte Read-Write, Read-Modify-Write Cycle



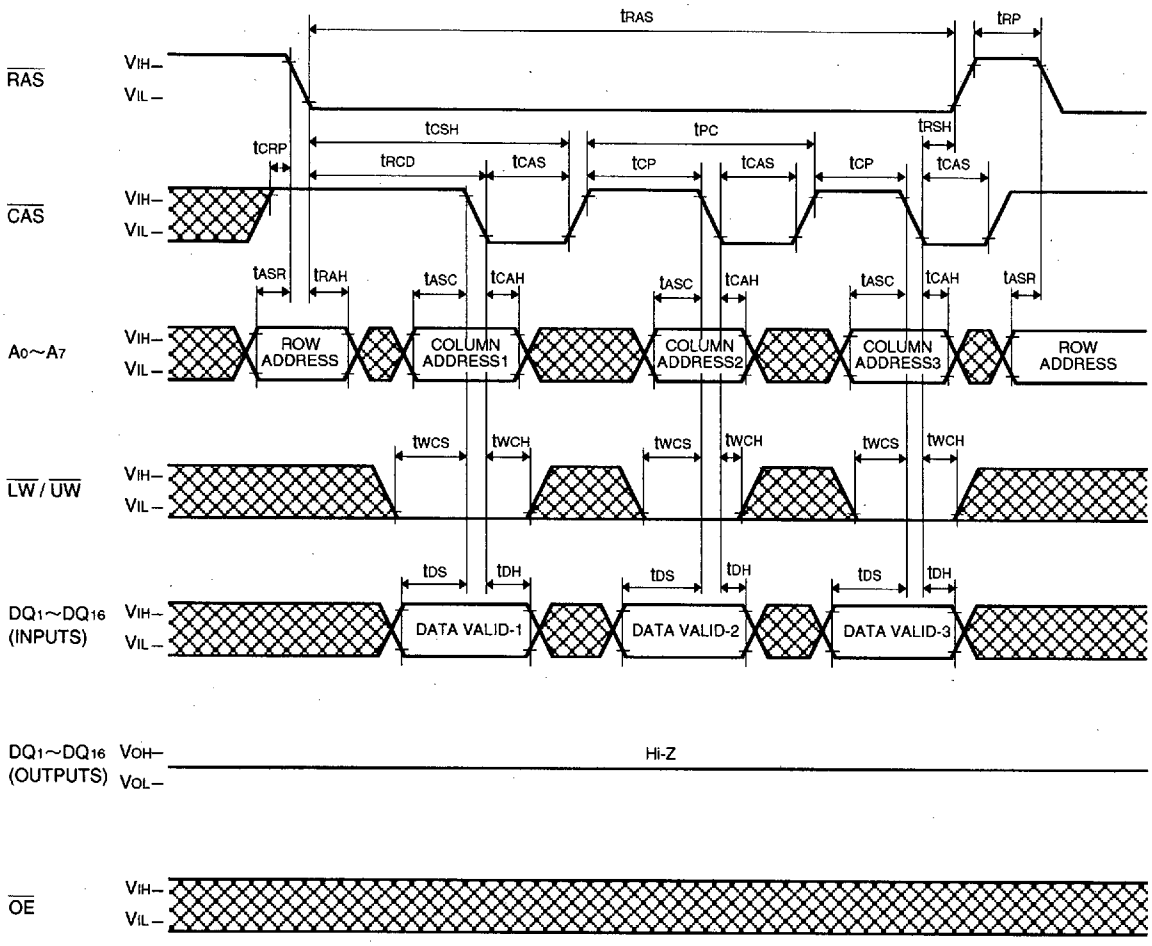
M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Read Cycle



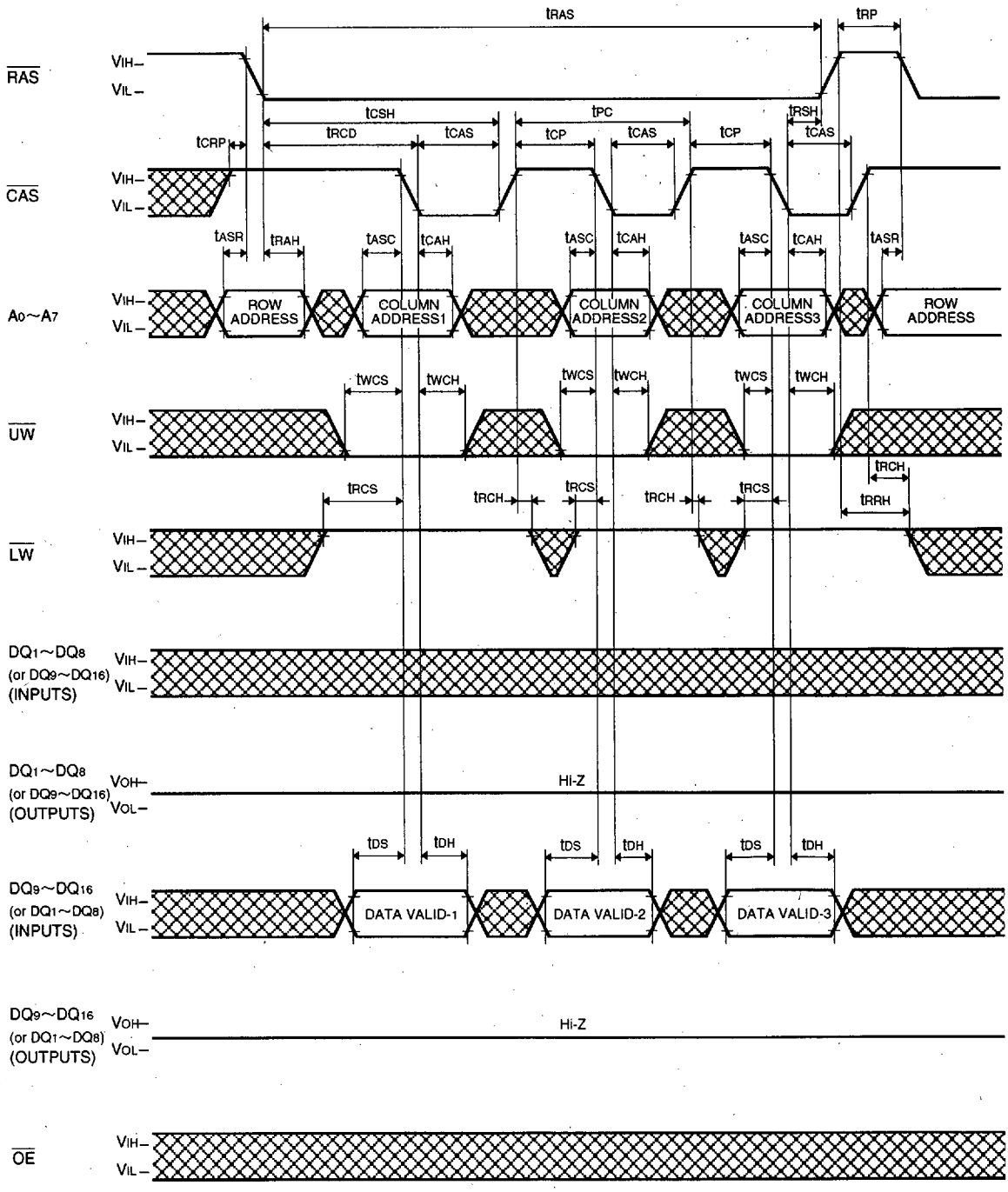
M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Early Write Cycle



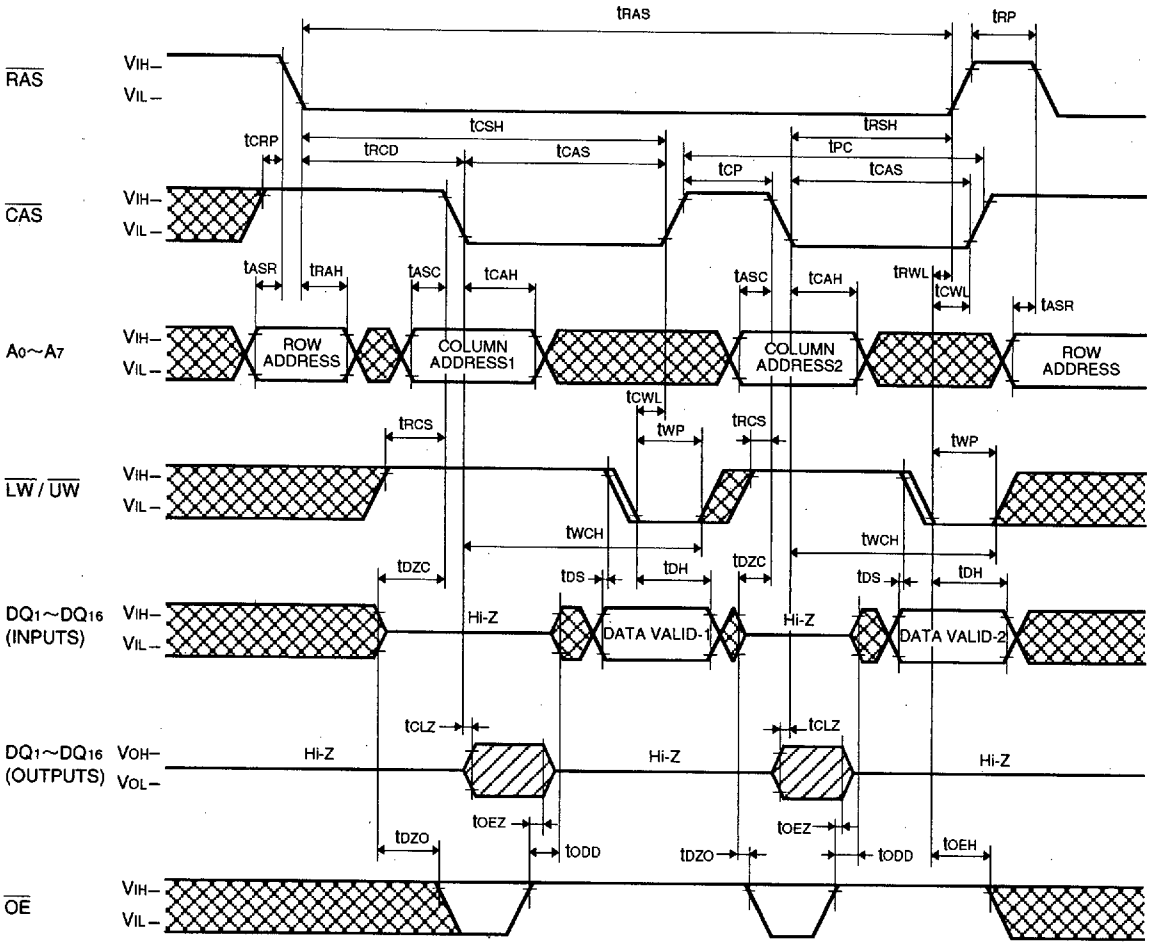
M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Byte Early Write Cycle



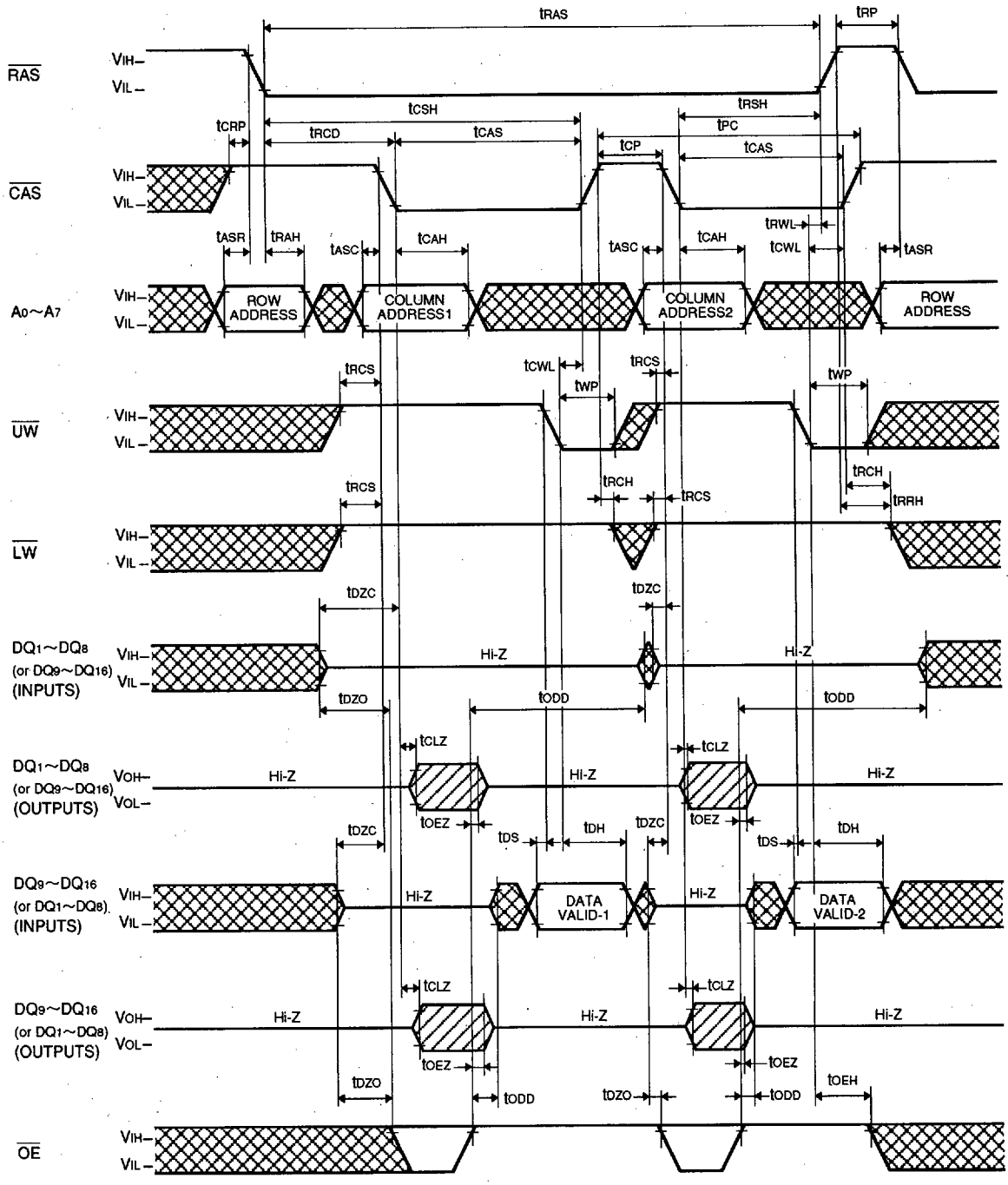
M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Delayed Write Cycle



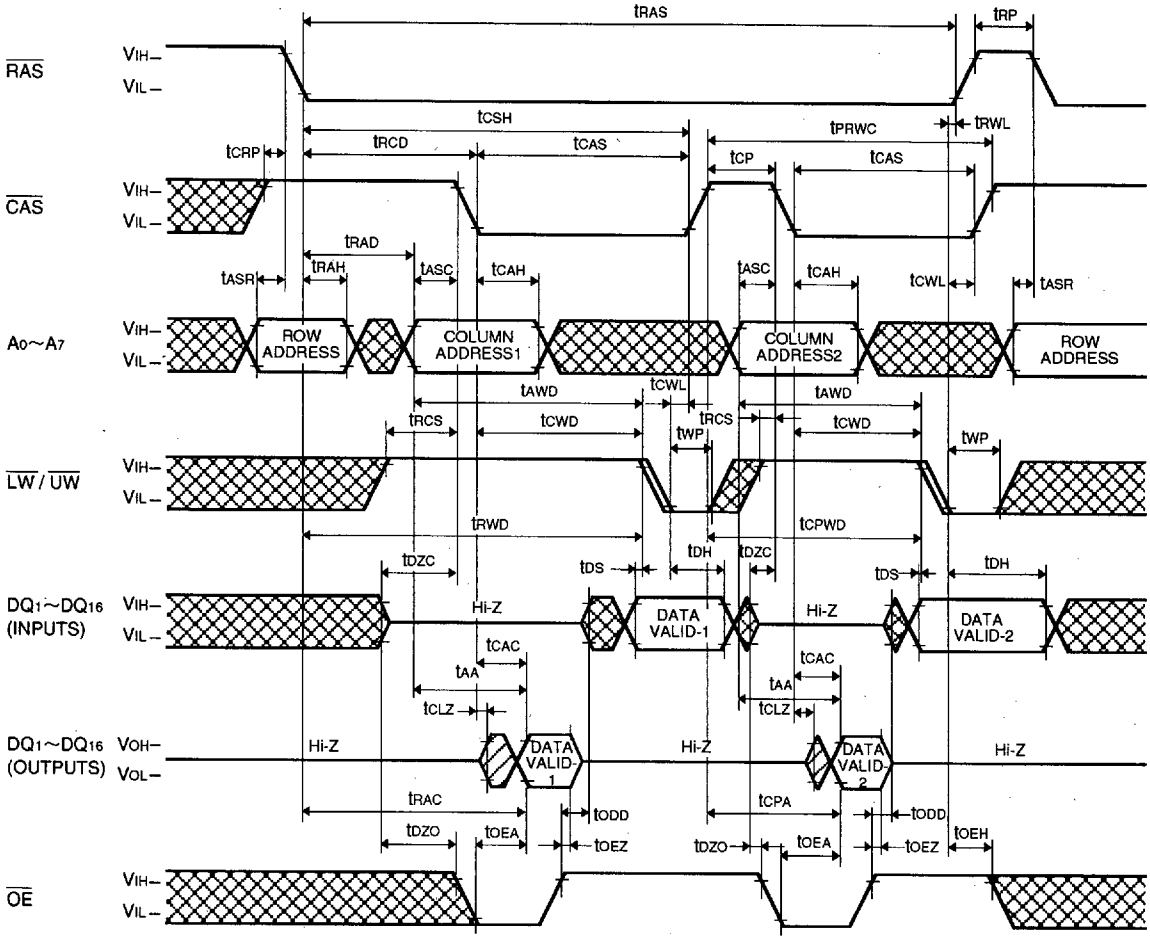
M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Byte Delayed Write Cycle



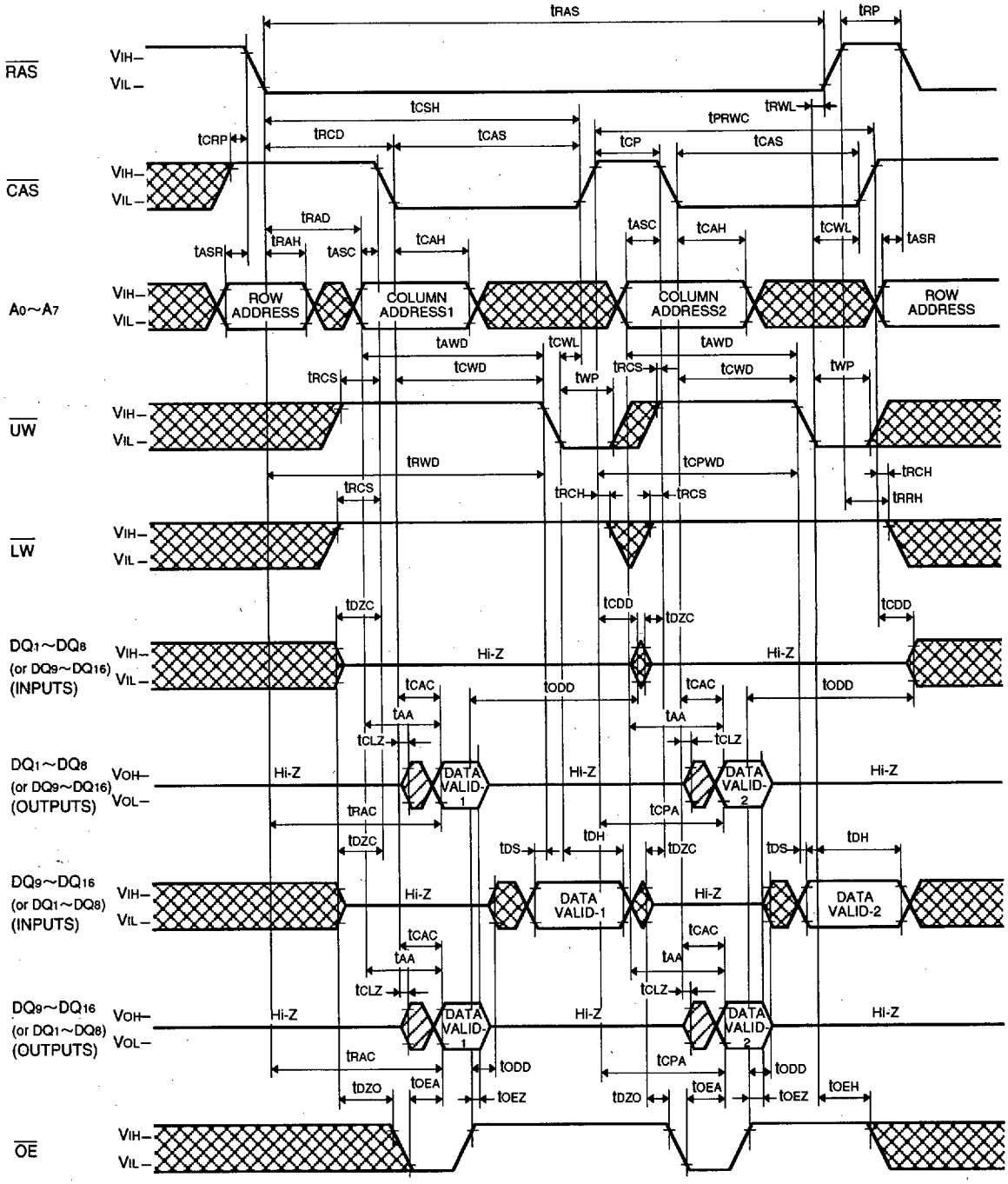
M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Read-Write, Read-Modify-Write Cycle



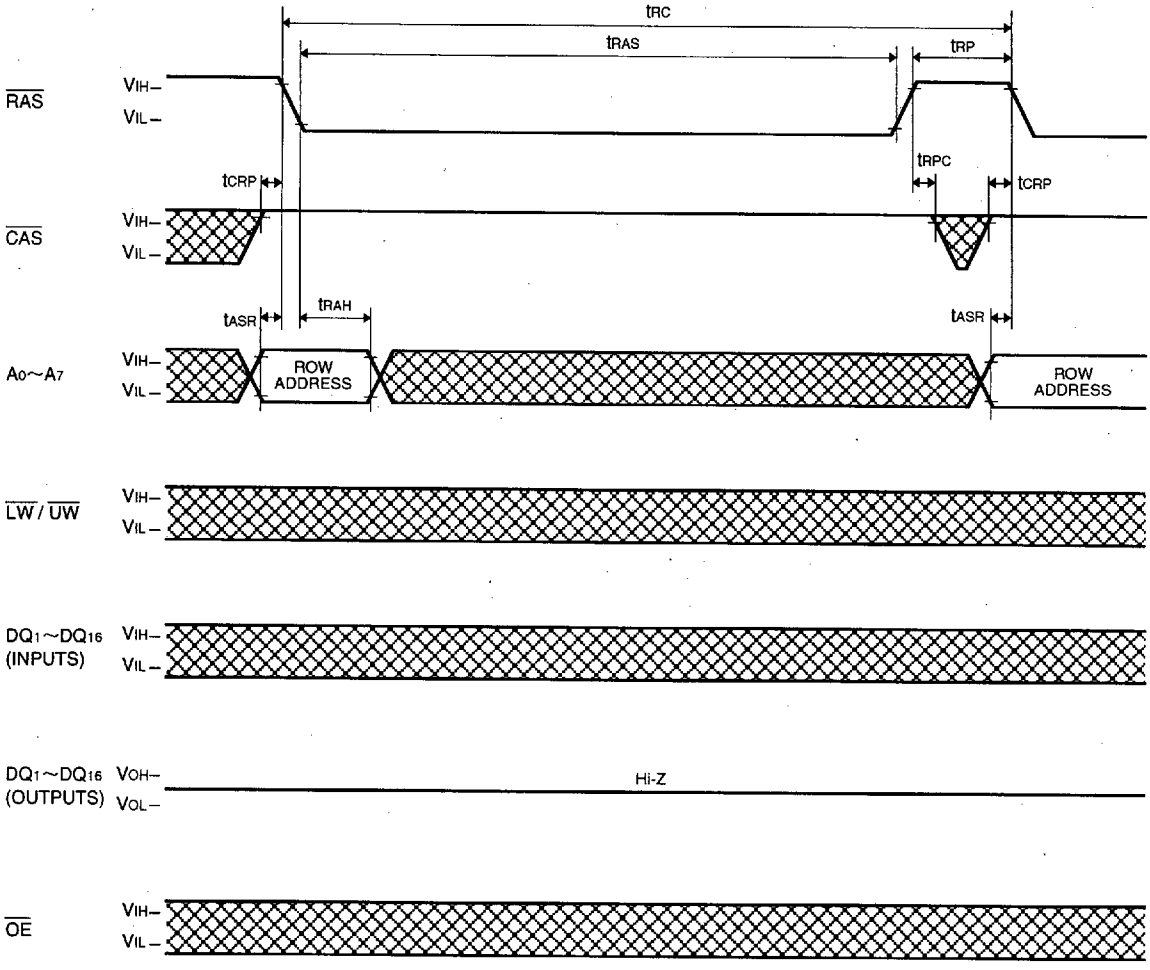
M5M411664AJ,TP1-5,-5S:Under development

Fast Page Mode Byte Read-Write, Read-Modify-Write Cycle



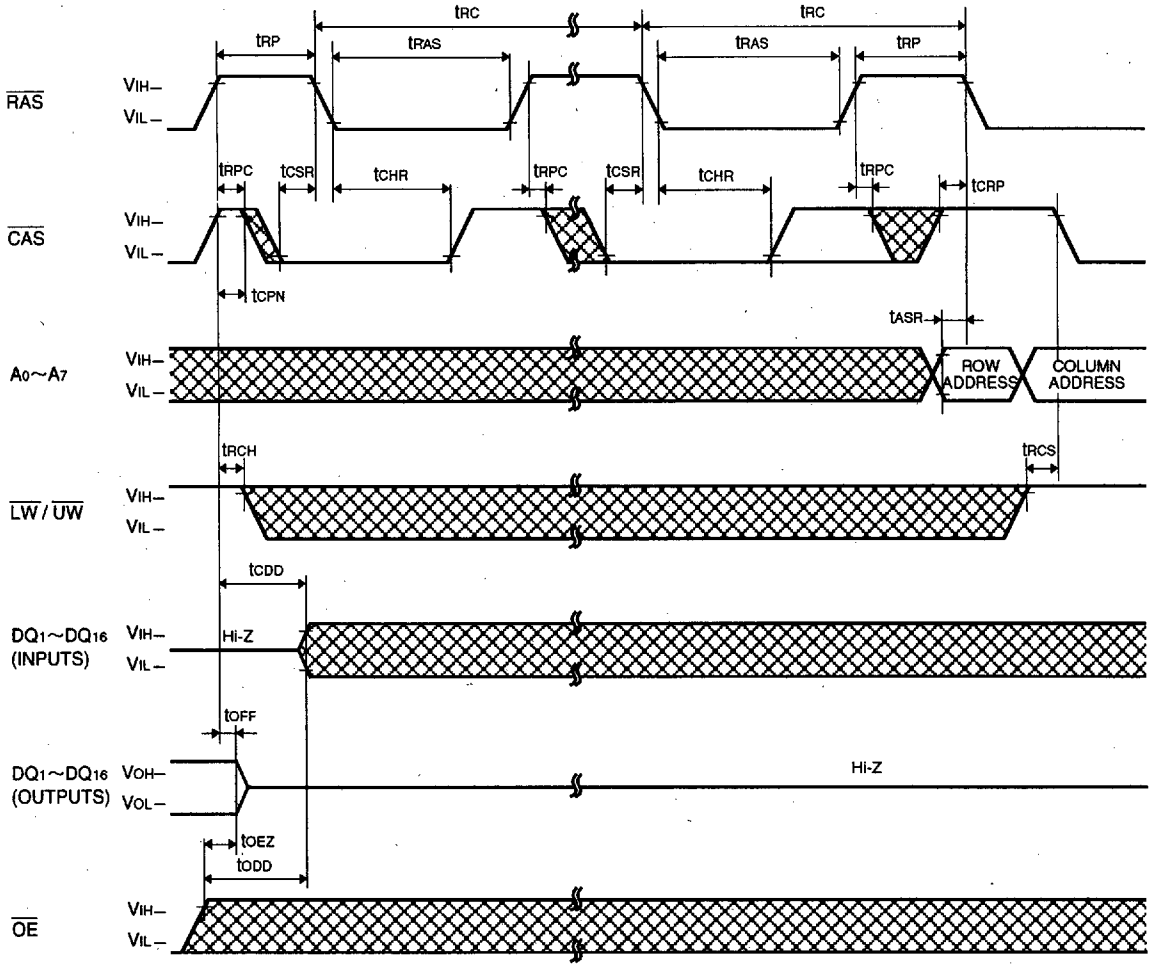
M5M411664AJ,TP1-5,-5S:Under development

RAS-only Refresh Cycle



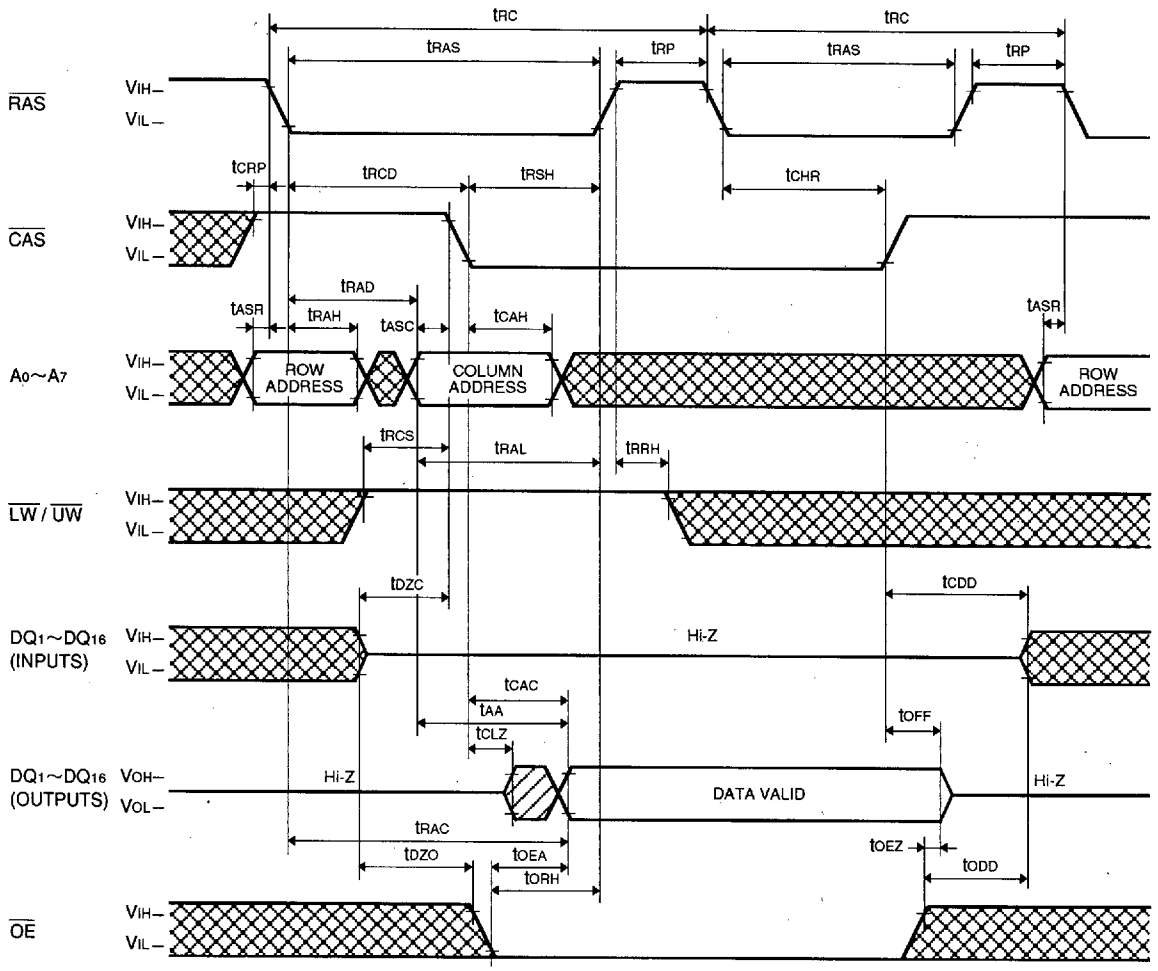
M5M411664AJ,TP1-5,-5S:Under development

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



M5M411664AJ,TP1-5,-5S:Under development

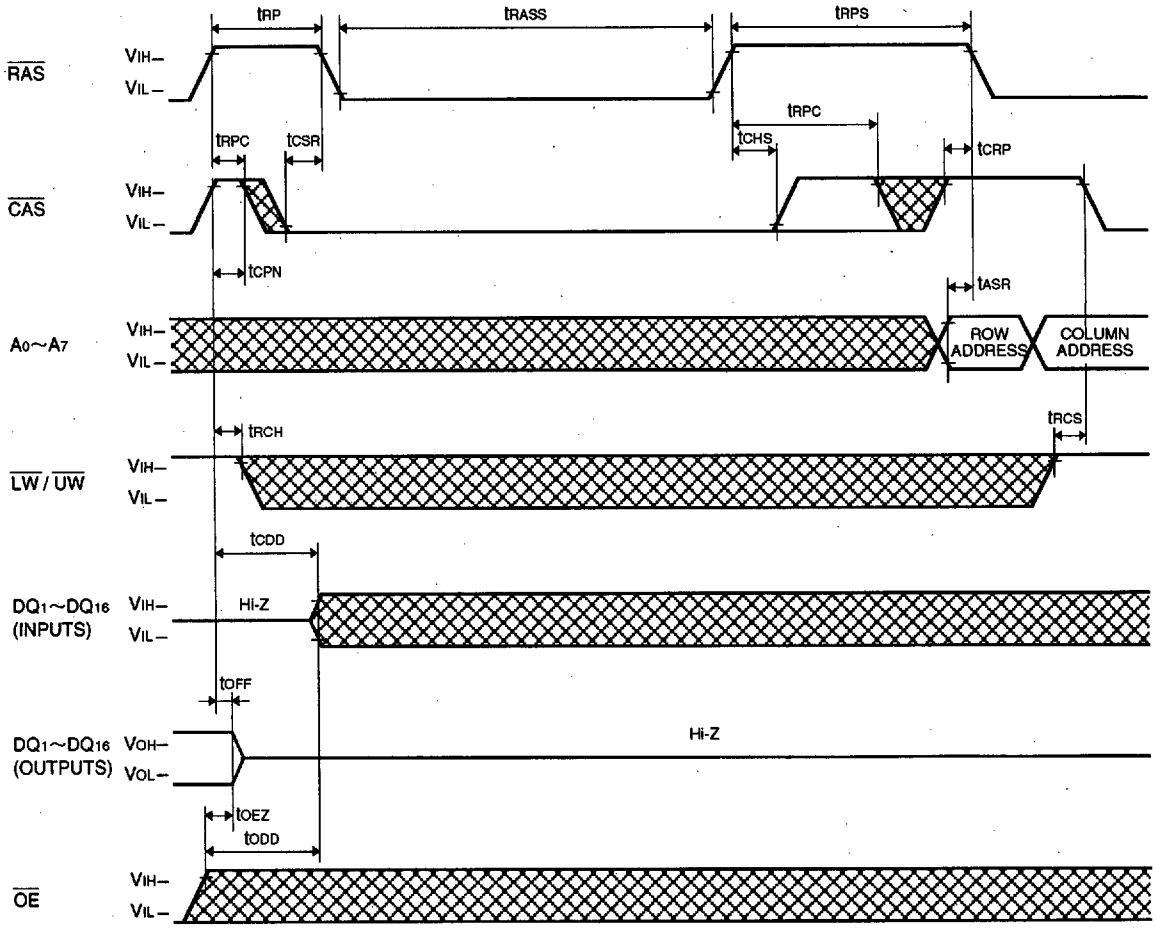
Hidden Refresh Cycle (Read) (Note 30)



Note 30 : Early write, delayed write, read write or read-modefy write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

M5M411664AJ,TP1-5,-5S:Under development

Self Refresh Cycle (Note 28)

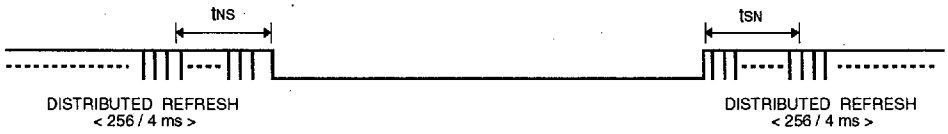


M5M411664AJ,TP1-5,-5S:Under development

Note 28 : SELF REFRESH ENTRY & EXIT CONDITIONS

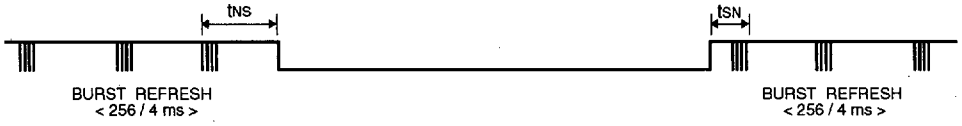
(1) In case of distributed refresh

The last and first full refresh cycles (256) must be done within t_{NS} and t_{SN} before and after self refresh, on the condition of $t_{NS} \leqq 4ms$ and $t_{SN} \leqq 4ms$.



(2) In case of burst refresh

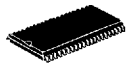
The last and first full refresh cycles (256) must be done within t_{NS} and t_{SN} before and after self refresh, on the condition of $t_{NS} \leqq 4ms$ and $t_{SN} \leqq 4ms$.



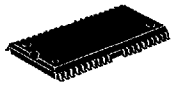
M5M411664AJ,TP1-5,-5S:Under development

PACKAGE OUTWARD

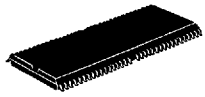
TSOP



42P3U-E

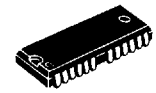


44P3W-R

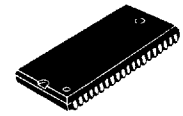


70P3S-L

SOJ



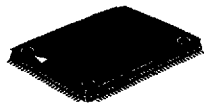
26P0J-B



40P0K

LQFP

128P6D-C



128P6D-D

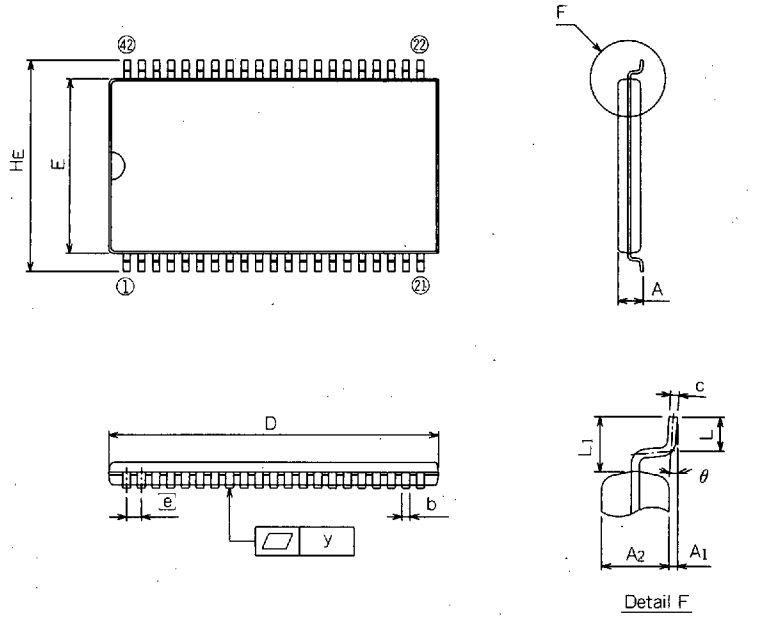
PACKAGE OUTLINES

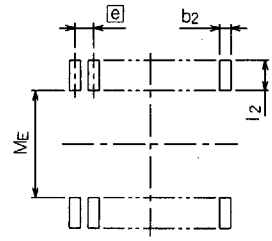
42P3U-E

Plastic 42pin 300mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII42-P-300-0.65	–	0.29	Alloy 42

Scale : 3/1





Recommended Mount Pad

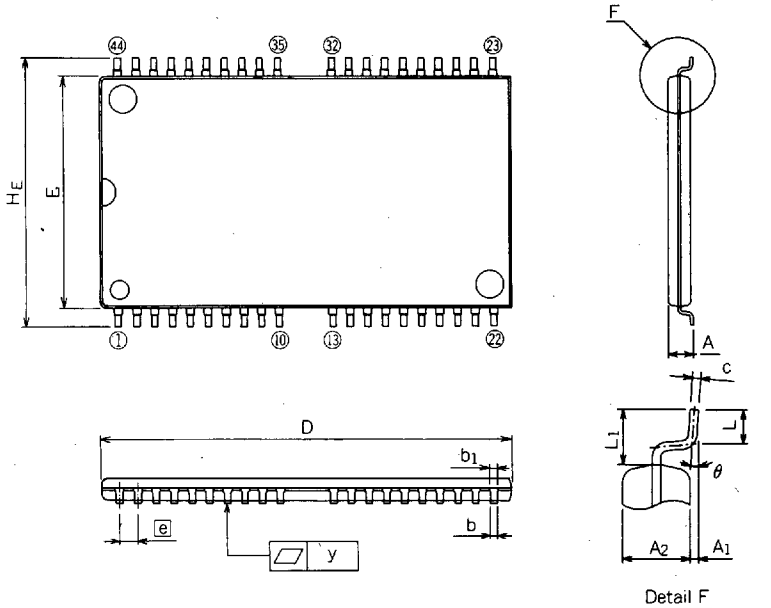
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0.05	0.125	0.2
A_2	–	1.0	–
b	0.25	0.3	0.4
c	0.105	0.125	0.175
D	14.5	14.6	14.7
E	7.52	7.62	7.72
e	–	0.65	–
H_E	9.02	9.22	9.42
L	0.4	0.5	0.6
L_1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
M_E	–	7.82	–
l_2	0.9	–	–
b_2	–	0.35	–

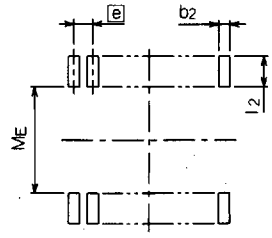
44P3W-R

Plastic 44pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOPII44/40-P-0400-0.80	–	0.47	Alloy 42

Scale : 3/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0.05	0.125	0.20
A_2	–	1.0	–
b	0.25	0.3	0.35
b_1	0.3	0.35	0.45
c	0.105	0.125	0.175
D	18.31	18.41	18.51
E	10.06	10.16	10.26
e	–	0.8	–
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	–	0.8	–
y	–	–	0.1
θ	0°	–	10°
M_E	–	10.36	–
l_2	0.9	–	–
b_2	–	0.5	–

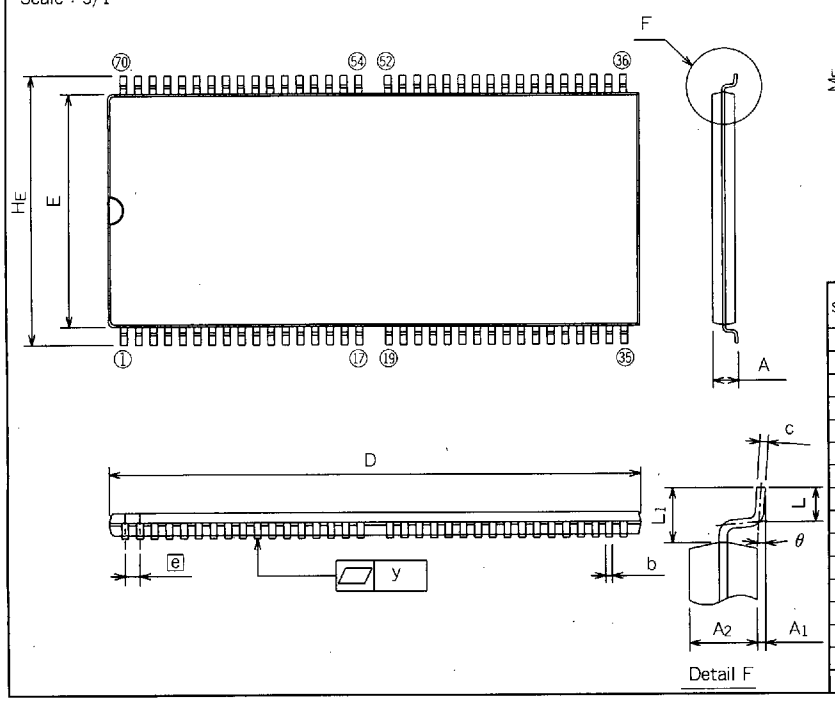
PACKAGE OUTLINES

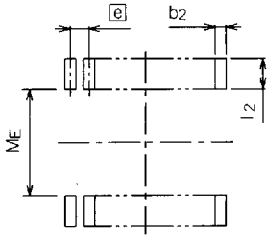
70P3S-L

Plastic 70pin 400mil TSOP(II)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP II 70/68-P-400-0.65	—		Alloy 42

Scale : 3/1





Recommended Mount Pad

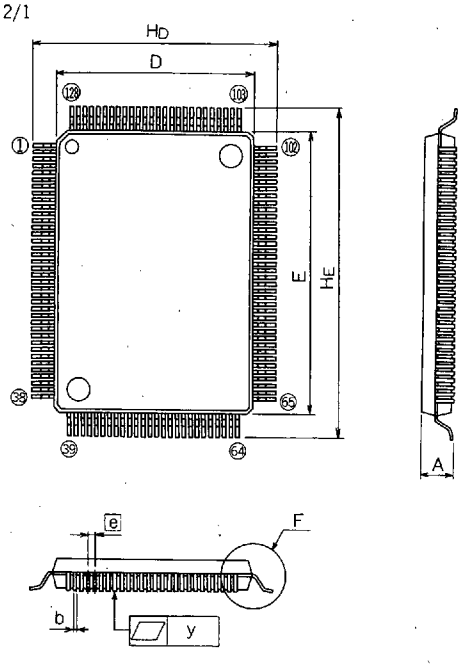
symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A_1	0.05	0.125	0.2
A_2	—	1.0	—
b	0.25	0.3	0.4
c	0.105	0.125	0.175
D	23.39	23.49	23.59
E	10.06	10.16	10.26
e	—	0.65	—
H_E	11.56	11.76	11.96
L	0.4	0.5	0.6
L_1	—	0.8	—
y	—	—	0.1
θ	0°	—	10°
M_E	—	10.36	—
l_2	0.9	—	—
b_2	—	0.35	—

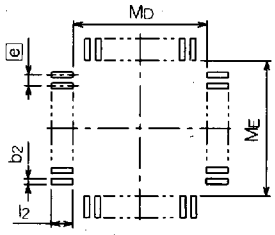
128P6D-C

Plastic 128pin 14×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	–	0.85	Alloy 42

Scale : 2/1





Recommended Mount Pad

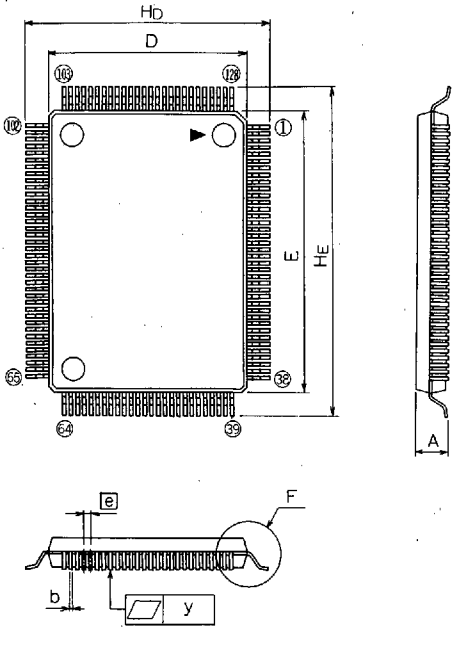
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0.05	0.15	0.25
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	21.8	22.0	22.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	14.4	–
M_E	–	20.4	–

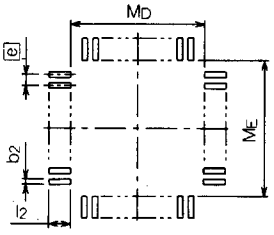
128P6D-D

Plastic 128pin 14×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	–	0.85	Alloy 42

Scale : 2/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A_1	0.05	0.15	0.25
A_2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	19.9	20.0	20.1
e	–	0.5	–
H_D	15.8	16.0	16.2
H_E	21.8	22.0	22.2
L	0.3	0.5	0.7
L_1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.225	–
l_2	1.0	–	–
M_D	–	14.4	–
M_E	–	20.4	–

MITSUBISHI ELECTRIC

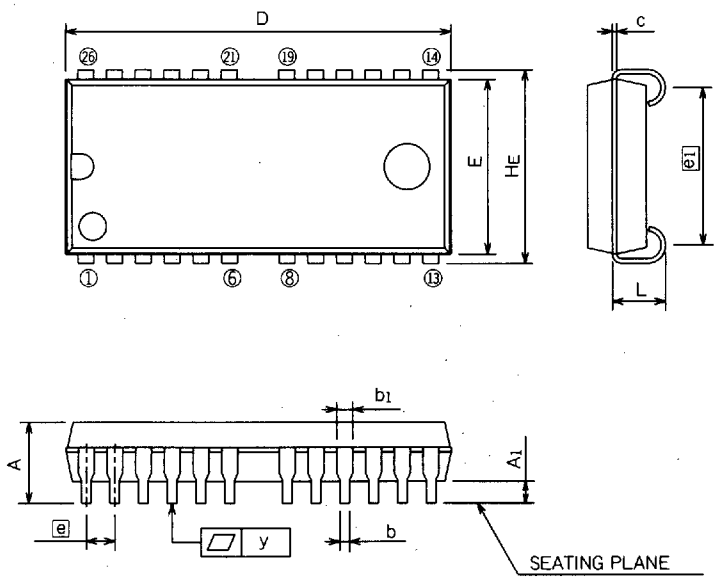
PACKAGE OUTLINES

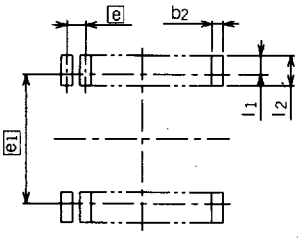
26P0J-B

Plastic 26pin 300mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ26/24-P-300-1.27	–		Alloy 42

Scale : 3/1





Recommended Mount Pad

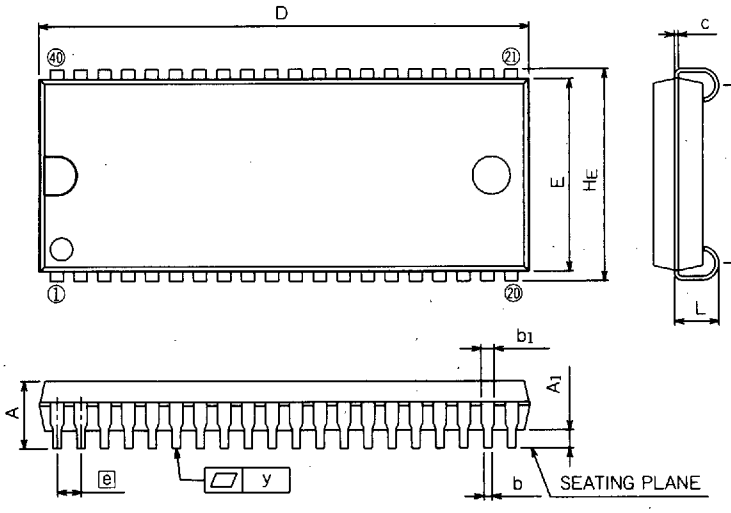
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	–	–
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	17.02	17.15	17.28
E	7.52	7.62	7.72
e	–	1.27	–
ei	6.73	6.86	6.99
HE	8.35	8.45	8.55
L	2.25	2.35	2.45
y	–	–	0.1
b_2	–	0.75	–
l_1	–	1.2	–
l_2	2.0	–	–

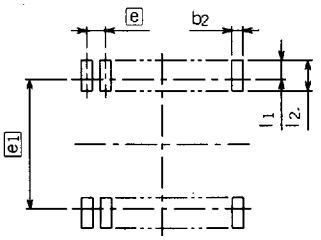
40P0K

Plastic 40pin 400mil SOJ

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOJ40-P-400-1.27	–	1.53	Alloy 42

Scale : 2.5/1





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	3.35	3.45	3.55
A_1	0.8	–	–
b	0.38	0.43	0.5
b_1	0.66	0.7	0.81
c	0.18	0.2	0.25
D	25.91	26.04	26.17
E	10.03	10.16	10.29
e	–	1.27	–
ei	9.27	9.4	9.53
HE	11.05	11.18	11.31
L	2.25	2.35	2.45
y	–	–	0.1
b_2	–	0.75	–
l_1	–	1.2	–
l_2	2.0	–	–