# M5M411665AJ,TP2,TP3-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 1048576-BIT(65536-WORD BY 16-BIT) DYNAMIC RAM

## DESCRIPTION

This is a family of 65536-word by 16-bit dynamic RAMs, fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation,and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is small enough for battery back-up application.

This device has 2$\overline{W}$ and 1$\overline{CAS}$ terminals with a refresh cycle of 256 cycles every 4ms.

## FEATURES

| Type name | $\overline{RAS}$ access time (max.ns) | $\overline{CAS}$ access time (max.ns) | Address access time (max.ns) | $\overline{OE}$ access time (max.ns) | Cycle time (min.ns) | Power dissipation (typ.mW) |
|---|---|---|---|---|---|---|
| M5M411665AXX-5,-5S | 50 | 13 | 25 | 13 | 90 | 625 |
| M5M411665AXX-6,-6S | 60 | 15 | 30 | 15 | 110 | 550 |
| M5M411665AXX-7,-7S | 70 | 20 | 35 | 20 | 130 | 475 |

XX=J,TP2,TP3

- AJ: 40 pin SOJ/400mil,ATP2: 44 pin TSOP(Ⅱ)/400mil,ATP3: 44 pin TSOP(Ⅱ)/400mil
- Single 5V ±10% supply ..... 5.5 mW(Max)
- Low stand-by power dissipation ..... 550 µW(Max)*
  CMOS Input level
  CMOS Input level ..... 688 mW(Max)
- Operating power dissipation ..... 605 mW(Max)
  M5M411665Axx- 5,-5S ..... 523 mW(Max)
  M5M411665Axx- 6,-6S
  M5M411665Axx- 7,-7S ..... 150 µA(max)
- Self refresh capability *
  Self refresh current ..... 150 µA(max)
- Extended refresh capability
  Extended refresh current
- Hyper-page mode (256-column random access), Read-modify-write, $\overline{RAS}$-only refresh,$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- 256 refresh cycles every 4ms ($A_0$ ~$A_7$)
- 256 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles every 32ms ($A_0$ ~$A_7$)* for extended refresh
- Byte control for Read / Write operation(2$\overline{W}$,1$\overline{CAS}$ type)

* :Applicable to self refresh version(M5M411665AXX-5S,-6S,-7S :option) only

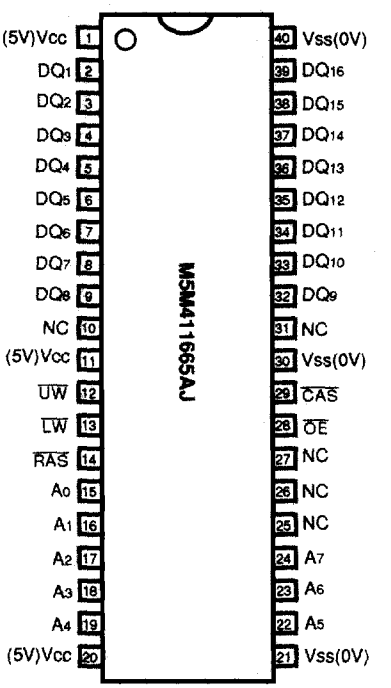
## APPLICATION

Microcomputer memory, Refresh memory for CRT, Frame Buffer memory for CRT.

## PIN DESCRIPTION

| Pin name | Function |
|---|---|
| $A_0$~$A_7$ | Address Inputs |
| DQ1~DQ16 | Data Inputs / Outputs |
| $\overline{RAS}$ | Row Address Strobe Input |
| $\overline{CAS}$ | Column Address Strobe Input |
| $\overline{LW}$ | Lower Byte Control Write Control Input |
| $\overline{UW}$ | Upper Byte Control Write Control Input |
| $\overline{OE}$ | Output Enable Input |
| Vcc | Power Supply (+5V) |
| Vss | Ground (0V) |

## PIN CONFIGURATION (TOP VIEW)

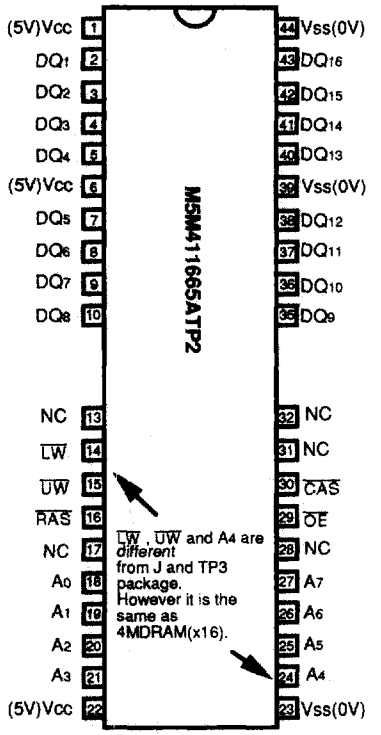



Outline 40P0K(400mil 40 pin SOJ)

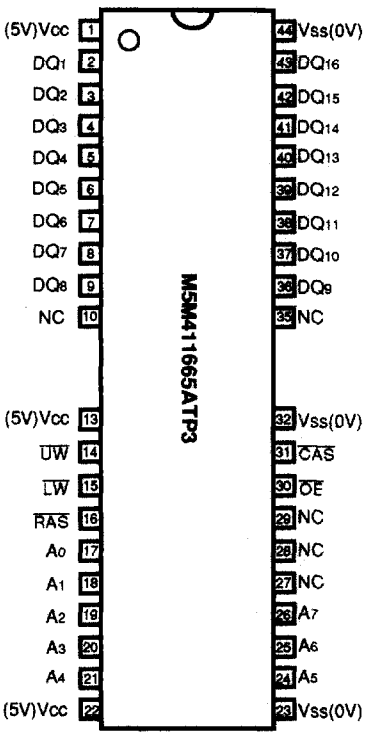
NC: NO CONNECTION

M5M411665AJ,TP2,TP3 -5,-5S : Under development

## PIN CONFIGURATION (TOP VIEW)



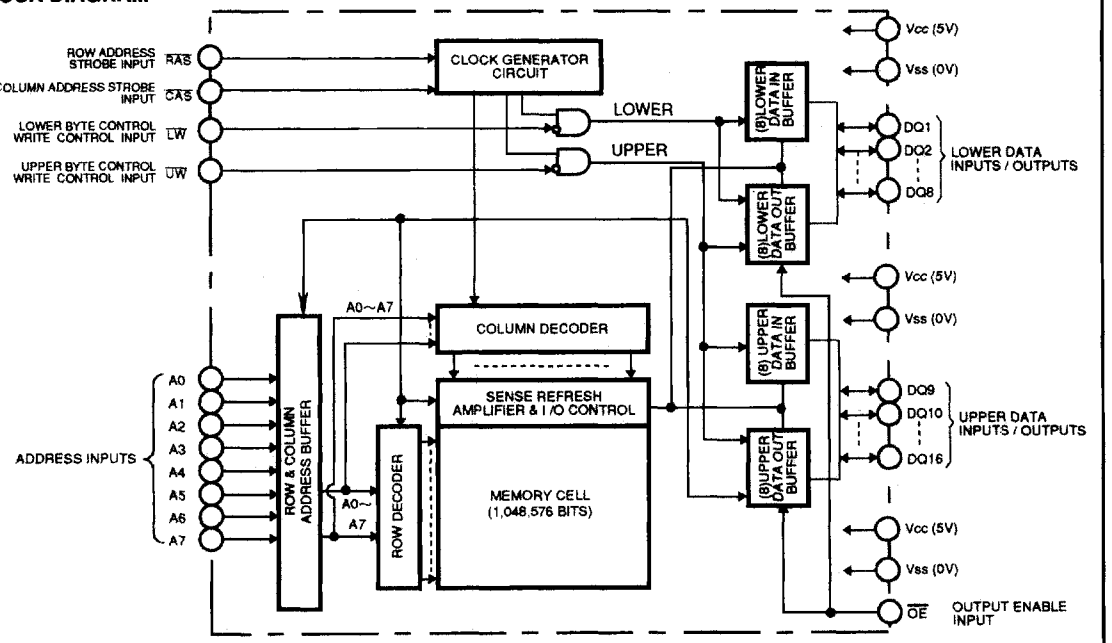

Outline 44P3W-R(400mil 44 pin TSOP)




Outline 44P3W-R(400mil 44 pin TSOP)

NC : NO CONNECTION

## BLOCK DIAGRAM

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## FUNCTION

In addition to normal read,write, and read-modify-write operations the M5M411665 ATP3,ATP2, AJ provides a number of other functions,e.g., Hyper Page Mode, $\overline{RAS}$-only refresh,and delayed-write.
The input conditions for each are shown in Table 1.

**Table 1. Input conditions for each mode**

| Operation | inputs | | | | | | | input / output | | | | Refresh | Remark |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Lower | | Upper | | | |
| | $\overline{RAS}$ | $\overline{LW}$ | $\overline{UW}$ | $\overline{CAS}$ | $\overline{OE}$ | Row address | Column address | D | Q | D | Q | | |
| Read | ACT | NAC | NAC | ACT | ACT | APD | APD | OPN | VLD | OPN | VLD | YES | Hyper page mode identical |
| Early write | ACT | ACT | ACT | ACT | DNC | APD | APD | VLD | OPN | VLD | OPN | YES | |
| Upper early | ACT | NAC | ACT | ACT | DNC | APD | APD | DNC | OPN | VLD | OPN | YES | |
| Lower early | ACT | ACT | NAC | ACT | DNC | APD | APD | VLD | OPN | DNC | OPN | YES | |
| Delayed write | ACT | ACT | ACT | ACT | ACT | APD | APD | VLD | OPN | VLD | OPN | YES | |
| Upper delayed | ACT | NAC | ACT | ACT | ACT | APD | APD | DNC | OPN | VLD | OPN | YES | |
| Lower delayed | ACT | ACT | NAC | ACT | ACT | APD | APD | VLD | OPN | DNC | OPN | YES | |
| Read-modify-W | ACT | ACT | ACT | ACT | ACT | APD | APD | VLD | OPN | VLD | OPN | YES | |
| Upper RMW | ACT | NAC | ACT | ACT | ACT | APD | APD | DNC | OPN | VLD | OPN | YES | |
| Lower RMW | ACT | ACT | NAC | ACT | ACT | APD | APD | VLD | OPN | DNC | OPN | YES | |
| $\overline{RAS}$ only-R | ACT | DNC | DNC | NAC | DNC | APD | DNC | DNC | OPN | DNC | OPN | YES | |
| Hidden refresh | ACT | NAC | NAC | ACT | ACT | DNC | DNC | OPN | VLD | OPN | VLD | YES | |
| CBRrefresh (Extended) | ACT | DNC | DNC | ACT | DNC | DNC | DNC | DNC | OPN | DNC | OPN | YES | |
| Self Refresh* | ACT | DNC | DNC | ACT | DNC | DNC | DNC | DNC | OPN | DNC | OPN | YES | |
| Stand-by | NAC | DNC | DNC | DNC | DNC | DNC | DNC | DNC | OPN | DNC | OPN | NO | |

Note :ACT ; active DNC ; don't care VLD ; valid IVD ; invalid APD ; applied OPN ; open NAC; nonactive

## ABSOLUTE MAXIMUN RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to Vss | −1~7 | V |
| $V_I$ | Input voltage | | −1~7 | V |
| $V_O$ | Output voltage | | −1~7 | V |
| $I_O$ | Output current | | 50 | mA |
| $P_d$ | Power dissipation | Ta=25℃ | 1000 | mW |
| $T_{opr}$ | Operating temperature | | 0~70 | ℃ |
| $T_{stg}$ | Storage temperature | | −65~150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | High-level input voltage, all inputs | 2.4 | | 6.0 | V |
| $V_{IL}$ | Low-level input voltage, all inputs | −0.5** | | 0.8 | V |

Note 1 : All voltage values are with respect to Vss.

** : $V_{IL}$(min) is -2 .0V when pulse width is less than 25ns.(pulse width is with respect to Vss.)

## ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = −2mA | 2.4 | | Vcc | V |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 2mA | 0 | | 0.4 | V |
| $I_{OZ}$ | Off-state output voltage | | Q floating,0V ≦ $V_{OUT}$≦5.5V | −10 | | 10 | μA |
| $I_I$ | Input current | | 0V≦$V_{IH}$≦6.0V, Other inputs pins = 0V | −10 | | 10 | μA |
| $I_{CC1}$ (AV) | Average supply current from Vcc operating (Note 3,4,5) | M5M411665A-5,-5S | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}$ = $t_{WC}$ =min. output open | | | 125 | mA |
| | | M5M411665A-6,-6S | | | | 110 | |
| | | M5M411665A-7,-7S | | | | 95 | |
| $I_{CC2}$ | Supply current from Vcc , stand-by (Note 6) | | $\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$, output open | | | 2 | mA |
| | | | $\overline{RAS}$ = $\overline{CAS}$ ≧ Vcc -0.5V output open | | | 1.0 | |
| | | | | | | 0.1* | |
| $I_{CC3}$ (AV) | Average supply current from Vcc,$\overline{RAS}$ only refresh mode (Note 3,5) | M5M411665A-5,-5S | $\overline{RAS}$ cycling, $\overline{CAS}$= $V_{IH}$ $t_{RC}$=min. output open | | | 125 | mA |
| | | M5M411665A-6,-6S | | | | 110 | |
| | | M5M411665A-7,-7S | | | | 95 | |
| $I_{CC4}$(AV) | Average supply current from Vcc Hyper Page Mode (Note 3,4,5) | M5M411665A-5,-5S | $\overline{RAS}$=VIL, $\overline{CAS}$ cycling $t_{PC}$=min. output open | | | 125 | mA |
| | | M5M411665A-6,-6S | | | | 110 | |
| | | M5M411665A-7,-7S | | | | 95 | |
| $I_{CC6}$(AV) | Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5) | M5M411665A-5,-5S | $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{RC}$=min. output open | | | 115 | mA |
| | | M5M411665A-6,-6S | | | | 100 | |
| | | M5M411665A-7,-7S | | | | 85 | |
| $I_{CC8}$(AV) * | Average supply current from Vcc Extended-Refresh mode (Note 6) | | $\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$ ≦ 0.2V or ≧ Vcc-0.2V $\overline{CAS}$≦ 0.2V or ≧ Vcc-0.2V $\overline{W}$ ≦ 0.2V or ≧ Vcc-0.2V $\overline{OE}$ ≦ 0.2V or ≧ Vcc-0.2V $A_0$~$A_7$ ≦ 0.2V or ≧ Vcc-0.2V DQ = open $t_{RC}$ = 125 μs, $t_{RAS}$=$t_{RAS}$ min ~1μ s | | | 150 | μA |
| $I_{CC9}$(AV) * | Average supply current from Vcc Self-Refresh mode (Note 6) | | $\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V output open | | | 150 | μA |

Note 2: Current flowing into an IC is positive, out is negative.

3: $I_{CC1}$ (AV), $I_{CC3}$ (AV) ,$I_{CC4}$ (AV) , and $I_{CC6}$ (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
Address transient between $\overline{RAS}$ and $\overline{CAS}$ happens once or less. Address transient during $\overline{CAS}$ cycle happens once or less.

4: $I_{CC1}$ (AV) and $I_{CC4}$ (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while $\overline{RAS}$=VIL and $\overline{CAS}$=$V_{IH}$.

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**CAPACITANCE** (Ta=0~70℃, Vcc= 5V±10%, VSS=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{I(A)}$ | Input capacitance, address inputs | $V_I$=Vss | | | 5 | pF |
| $C_{I(CLK)}$ | Input capacitance, clock inputs | f=1MHz | | | 7 | pF |
| $C_{I/O}$ | Input/Output capacitance, data ports | $V_I$=25mVrms | | | 7 | pF |

**SWITCHING CHARACTERISTICS** (Ta=0~70℃, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 6,14,15)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{CAC}$ | Access time from $\overline{CAS}$ low | (Note 7,8) | | 13 | | 15 | | 20 | ns |
| $t_{RAC}$ | Access time from $\overline{RAS}$ low | (Note 7,9) | | 50 | | 60 | | 70 | ns |
| $t_{AA}$ | Column address access time | (Note 7,10) | | 25 | | 30 | | 35 | ns |
| $t_{CPA}$ | Access time from $\overline{CAS}$ precharge | (Note 7,11) | | 28 | | 33 | | 38 | ns |
| $t_{OEA}$ | Access time from $\overline{OE}$ low | (Note 7) | | 13 | | 15 | | 20 | ns |
| $t_{OHC}$ | Output hold time from $\overline{CAS}$ | (Note 13) | 5 | | 5 | | 5 | | ns |
| $t_{OHR}$ | Output hold time from $\overline{RAS}$ | (Note 13) | 5 | | 5 | | 5 | | ns |
| $t_{CLZ}$ | Output low impedance time from $\overline{CAS}$ low | (Note 7) | 5 | | 5 | | 5 | | ns |
| $t_{OEZ}$ | Output disable time after $\overline{OE}$ high | (Note 12) | | 13 | | 15 | | 20 | ns |
| $t_{WEZ}$ | Output disable time after $\overline{WE}$ high | (Note 12) | | 13 | | 15 | | 20 | ns |
| $t_{OFF}$ | Output disable time after $\overline{CAS}$ high | (Note 12,13) | | 13 | | 15 | | 20 | ns |
| $t_{REZ}$ | Output disable time after $\overline{RAS}$ high | (Note 12,13) | | 13 | | 15 | | 20 | ns |

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 1TTL loads and 50pF.
The reference levels for measuring of output signals are 2.0V($V_{OH}$) and 0.8V($V_{OL}$).

8: Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by amount that $t_{RCD}$ exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ}$ (max), $t_{WEZ}$(max) , $t_{OFF}$(max) and $t_{REZ}$(max) defines the time at which the output achieves the high impedance state ( $|I_{OUT}| \leqq \pm 10\mu A$ ) and is not reference to $V_{OH}$(min) or $V_{OL}$(max).

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

**TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Hyper-Page Mode Cycles)**
(Ta=0 ~70℃, Vcc = 5V ±10%, Vss=0V, unless otherwise noted) (Note 14,15)

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| tREF | Refresh cycle time | | | 4 | | 4 | | 4 | ms |
| tREF | Refresh cycle time* | | | 32 | | 32 | | 32 | ms |
| tRP | $\overline{RAS}$ high pulse width | | 30 | | 40 | | 50 | | ns |
| tRCD | Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low | (Note 16) | 18 | 32 | 20 | 38 | 20 | 42 | ns |
| tCRP | Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low | | 5 | | 5 | | 5 | | ns |
| tRPC | Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| tCPN | $\overline{CAS}$ high pulse width | | 8 | | 10 | | 13 | | ns |
| tRAD | Column address delay time from $\overline{RAS}$ low | (Note 17) | 13 | 25 | 15 | 30 | 15 | 35 | ns |
| tASR | Row address setup time before $\overline{RAS}$ low | | 0 | | 0 | | 0 | | ns |
| tASC | Column address setup time before $\overline{CAS}$ low | (Note 18) | 0 | 10 | 0 | 13 | 0 | 13 | ns |
| tRAH | Row address hold time after $\overline{RAS}$ low | | 8 | | 10 | | 10 | | ns |
| tCAH | Column address hold time after $\overline{CAS}$ low | | 8 | | 10 | | 10 | | ns |
| tDZC | Delay time, data to $\overline{CAS}$ low | (Note 19) | 0 | | 0 | | 0 | | ns |
| tDZO | Delay time, data to $\overline{OE}$ low | (Note 19) | 0 | | 0 | | 0 | | ns |
| tRDD | Delay time, $\overline{RAS}$ high to data | (Note 20) | 13 | | 15 | | 20 | | ns |
| tCDD | Delay time, $\overline{CAS}$ high to data | (Note 20) | 13 | | 15 | | 20 | | ns |
| tODD | Delay time, $\overline{OE}$ high to data | (Note 20) | 13 | | 15 | | 20 | | ns |
| tT | Transition time | (Note 21) | 1 | 50 | 1 | 50 | 1 | 50 | ns |

Note 14 : The timing requirements are assumed tT = 2ns.
15 : VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
16 : tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
17 : tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.
18 : tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.
19 : Either tDZC or tDZO must be satisfied.
20 : Either tRDD or tCDD or tODD must be satisfied.
21 : tT is measured between VIH(min) and VIL(max).

**Read and Refresh Cycles**

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| tRC | Read cycle time | | 90 | | 110 | | 130 | | ns |
| tRAS | $\overline{RAS}$ low pulse width | | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| tCAS | $\overline{CAS}$ low pulse width | | 8 | 10000 | 10 | 10000 | 13 | 10000 | ns |
| tCSH | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 40 | | 48 | | 55 | | ns |
| tRSH | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 13 | | 15 | | 20 | | ns |
| tRCS | Read Setup time before $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| tRCH | Read hold time after $\overline{CAS}$ high | (Note 22) | 0 | | 0 | | 0 | | ns |
| tRRH | Read hold time after $\overline{RAS}$ high | (Note 22) | 0 | | 0 | | 0 | | ns |
| tRAL | Column address to $\overline{RAS}$ hold time | | 25 | | 30 | | 35 | | ns |
| tCAL | Column address to $\overline{CAS}$ hold time | | 13 | | 18 | | 23 | | ns |
| tORH | $\overline{RAS}$ hold time after $\overline{OE}$ low | | 13 | | 15 | | 20 | | ns |
| tOCH | $\overline{CAS}$ hold time after $\overline{OE}$ low | | 13 | | 15 | | 20 | | ns |

Note 22: Either tRCH or tRRH must be satisfied for a read cycle.

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**Write Cycle (Early Write and Delayed Write)**

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| tWC | Write cycle time | | 90 | | 110 | | 130 | | ns |
| tRAS | $\overline{RAS}$ low pulse width | | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| tCAS | $\overline{CAS}$ low pulse width | | 8 | 10000 | 10 | 10000 | 13 | 10000 | ns |
| tCSH | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 40 | | 48 | | 55 | | ns |
| tRSH | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 13 | | 15 | | 20 | | ns |
| tWCS | Write setup time before $\overline{CAS}$ low | (Note 24) | 0 | | 0 | | 0 | | ns |
| tWCH | Write hold time after $\overline{CAS}$ low | | 8 | | 10 | | 13 | | ns |
| tCWL | $\overline{CAS}$ hold time after $\overline{W}$ low | | 8 | | 10 | | 13 | | ns |
| tRWL | $\overline{RAS}$ hold time after $\overline{W}$ low | | 8 | | 10 | | 13 | | ns |
| tWP | Write pulse width | | 8 | | 10 | | 13 | | ns |
| tDS | Data setup time before $\overline{CAS}$ low or $\overline{W}$ low | | 0 | | 0 | | 0 | | ns |
| tDH | Data hold time after $\overline{CAS}$ low or $\overline{W}$ low | | 8 | | 10 | | 13 | | ns |

**Read-Write and Read-Modify-Write Cycles**

| Symbol | Parameter | | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | | Min | Max | Min | Max | Min | Max | |
| tRWC | Read write / read modify write cycle time | (Note 23) | 109 | | 133 | | 161 | | ns |
| tRAS | $\overline{RAS}$ low pulse width | | 75 | 10000 | 89 | 10000 | 107 | 10000 | ns |
| tCAS | $\overline{CAS}$ low pulse width | | 38 | 10000 | 44 | 10000 | 57 | 10000 | ns |
| tCSH | $\overline{CAS}$ hold time after $\overline{RAS}$ low | | 70 | | 82 | | 99 | | ns |
| tRSH | $\overline{RAS}$ hold time after $\overline{CAS}$ low | | 38 | | 44 | | 57 | | ns |
| tRCS | Read setup time before $\overline{CAS}$ low | | 0 | | 0 | | 0 | | ns |
| tCWD | Delay time, $\overline{CAS}$ low to $\overline{W}$ low | (Note 24) | 28 | | 32 | | 42 | | ns |
| tRWD | Delay time, $\overline{RAS}$ low to $\overline{W}$ low | (Note 24) | 65 | | 77 | | 92 | | ns |
| tAWD | Delay time, address to $\overline{W}$ low | (Note 24) | 40 | | 47 | | 57 | | ns |
| tOEH | $\overline{OE}$ hold time after $\overline{W}$ low | | 13 | | 15 | | 20 | | ns |

Noyr 23 : tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+5tT.

24 : tWCS, tCWD, tRWD and tAWD and, tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD (min), tAWD≧tAWD(min) and tCPWD ≧tCPWD(min) (for Hyper Page Mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH ) is indeterminate.

### Hyper Page Mode Cycle
### (Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{HPC}$ | Hyper Page Mode read / write cycle time (Note26) | 20 | | 25 | | 30 | | ns |
| $t_{HPRWC}$ | Hyper Page Mode read write / read modify write cycle time | 57 | | 66 | | 79 | | ns |
| $t_{DOH}$ | Output hold time from $\overline{CAS}$ low | 5 | | 5 | | 5 | | ns |
| $t_{RAS}$ | $\overline{RAS}$ low pulse width for read write cycle (Note27) | 65 | 100000 | 77 | 100000 | 92 | 100000 | ns |
| $t_{CP}$ | $\overline{CAS}$ high pulse width (Note28) | 8 | 13 | 10 | 16 | 13 | 16 | ns |
| $t_{CPRH}$ | $\overline{RAS}$ hold time after $\overline{CAS}$ precharge | 28 | | 33 | | 38 | | ns |
| $t_{CPWD}$ | Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24) | 43 | | 50 | | 60 | | ns |
| $t_{CHOL}$ | Hold time to maintain the data Hi-Z until $\overline{CAS}$ access | 7 | | 7 | | 7 | | ns |
| $t_{OEPE}$ | $\overline{OE}$ Pulse Width (Hi-Z control) | 7 | | 7 | | 7 | | ns |
| $t_{WPE}$ | $\overline{W}$ Pulse Width (Hi-Z control) | 7 | | 7 | | 7 | | ns |
| $t_{HCWD}$ | Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read | 28 | | 32 | | 42 | | ns |
| $t_{HAWD}$ | Delay time, Address to $\overline{W}$ low after read | 40 | | 47 | | 57 | | ns |
| $t_{HPWD}$ | Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read | 43 | | 50 | | 60 | | ns |
| $t_{HCOD}$ | Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read | 13 | | 15 | | 20 | | ns |
| $t_{HAOD}$ | Delay time, Address to $\overline{OE}$ high after read | 25 | | 30 | | 35 | | ns |
| $t_{HPOD}$ | Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read | 28 | | 33 | | 38 | | ns |

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper Page Mode cycle.
26: $t_{HPC}$(min) is specified in the case of read-only and early write-only in Hyper Page Mode.
27: $t_{RAS}$(min) is specified as two cycles of $\overline{CAS}$ input are performed.
28: $t_{CP}$(max) is specified as a reference point only.

### $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{CSR}$ | $\overline{CAS}$ setup time before $\overline{RAS}$ low | 5 | | 5 | | 5 | | ns |
| $t_{CHR}$ | $\overline{CAS}$ hold time after $\overline{RAS}$ low | 10 | | 10 | | 15 | | ns |

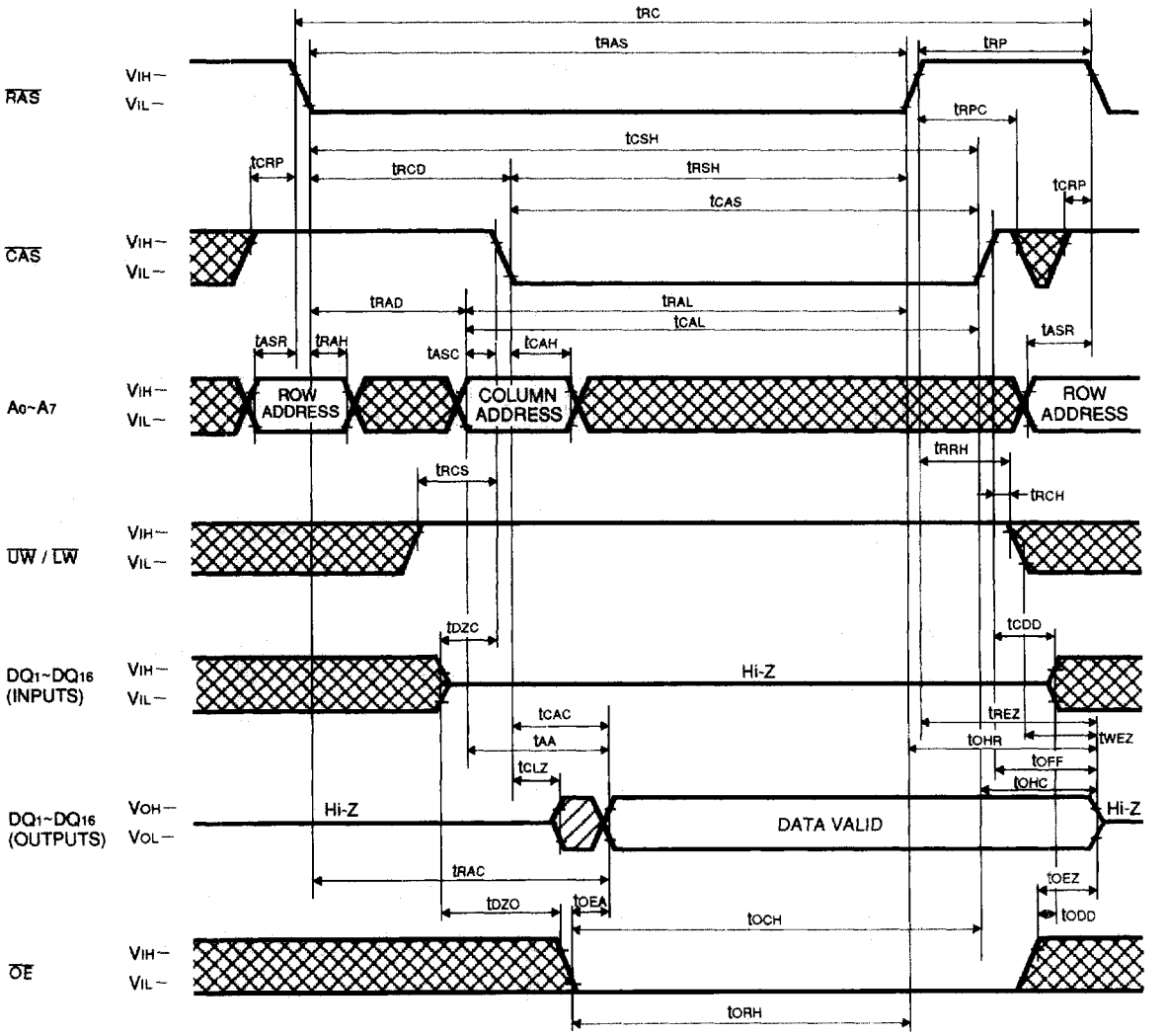
Note 29: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

### Self Refresh Cycle* (Note 32)

| Symbol | Parameter | Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | M5M411665A-5,-5S | | M5M411665A-6,-6S | | M5M411665A-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{RASS}$ | CBR self refresh $\overline{RAS}$ low pulse width | 100 | | 100 | | 100 | | μs |
| $t_{RPS}$ | CBR self refresh $\overline{RAS}$ high precharge time | 90 | | 110 | | 130 | | ns |
| $t_{CHS}$ | CBR self refresh $\overline{CAS}$ hold time | − 50 | | − 50 | | − 50 | | ns |

M5M411665AJ,TP2,TP3 -5,-5S : Under development

**Timing Diagrams** (Note 30)
**Read Cycle**



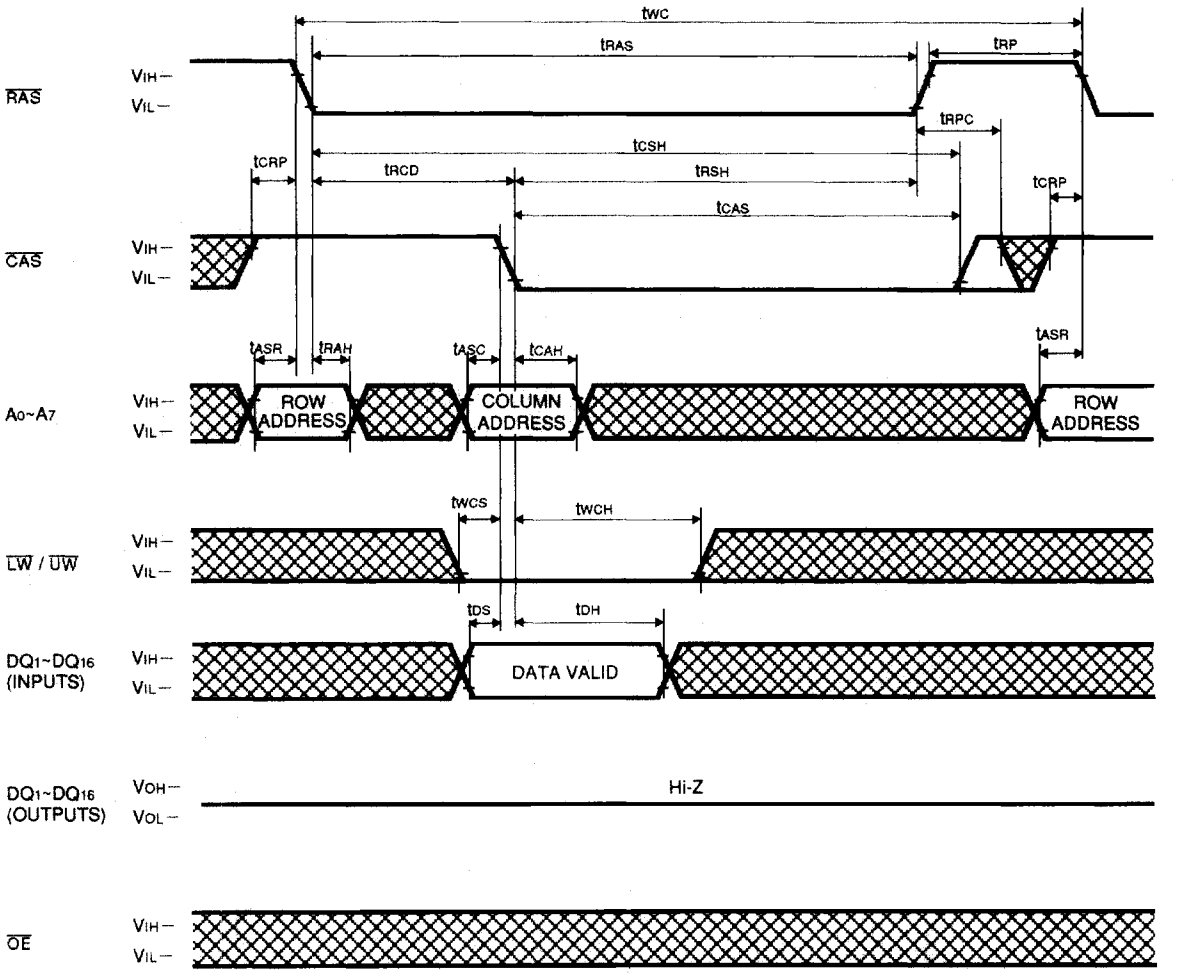

Note 30

Indicates the don't care input.
$V_{IH}(min) \leqq V_{IN} \leqq V_{IH}(max)$ or $V_{IL}(min) \leqq V_{IN} \leqq V_{IL}(max)$

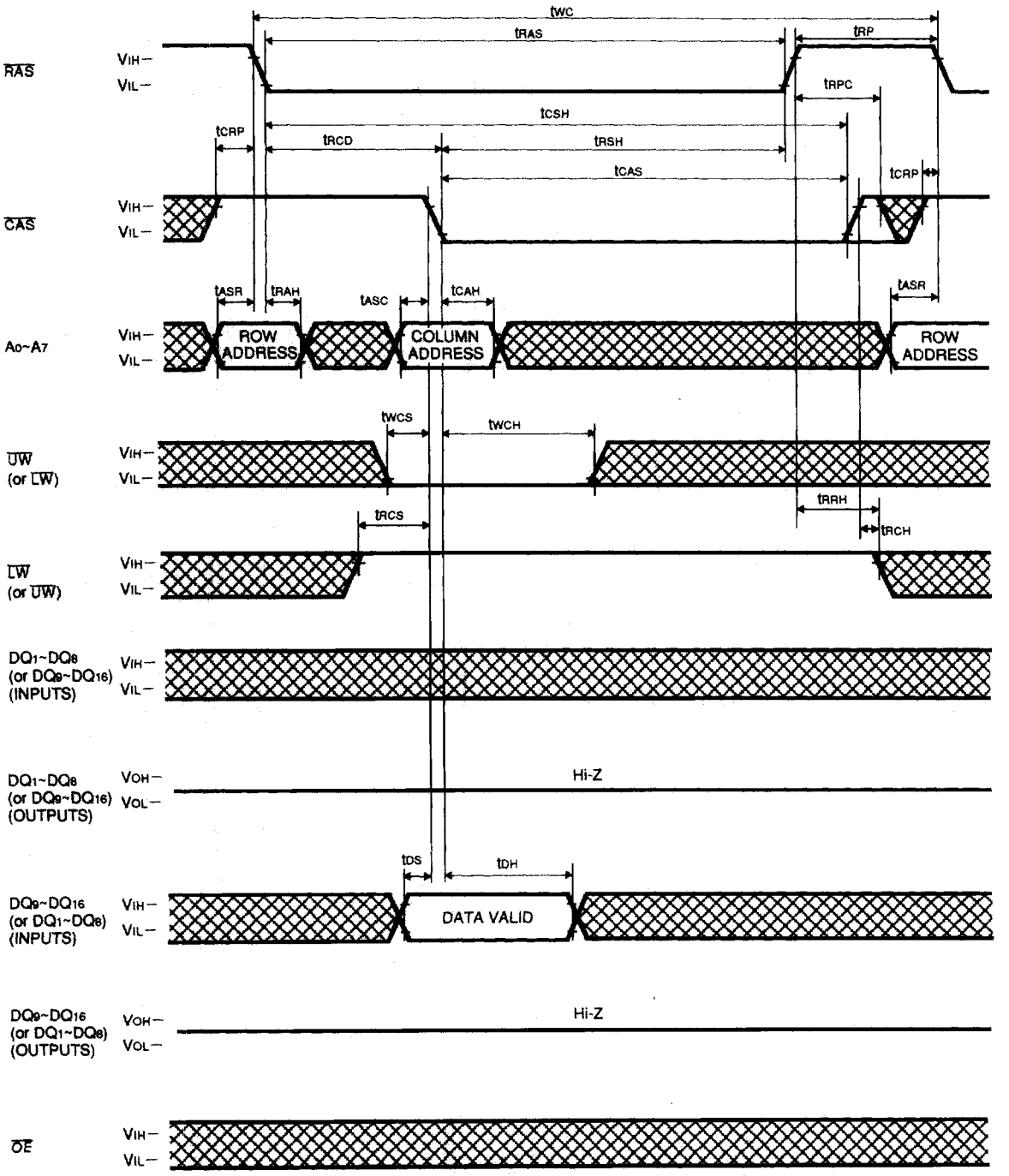
Indicates the invalid output.

M5M411665AJ,TP2,TP3 -5,-5S : Under development

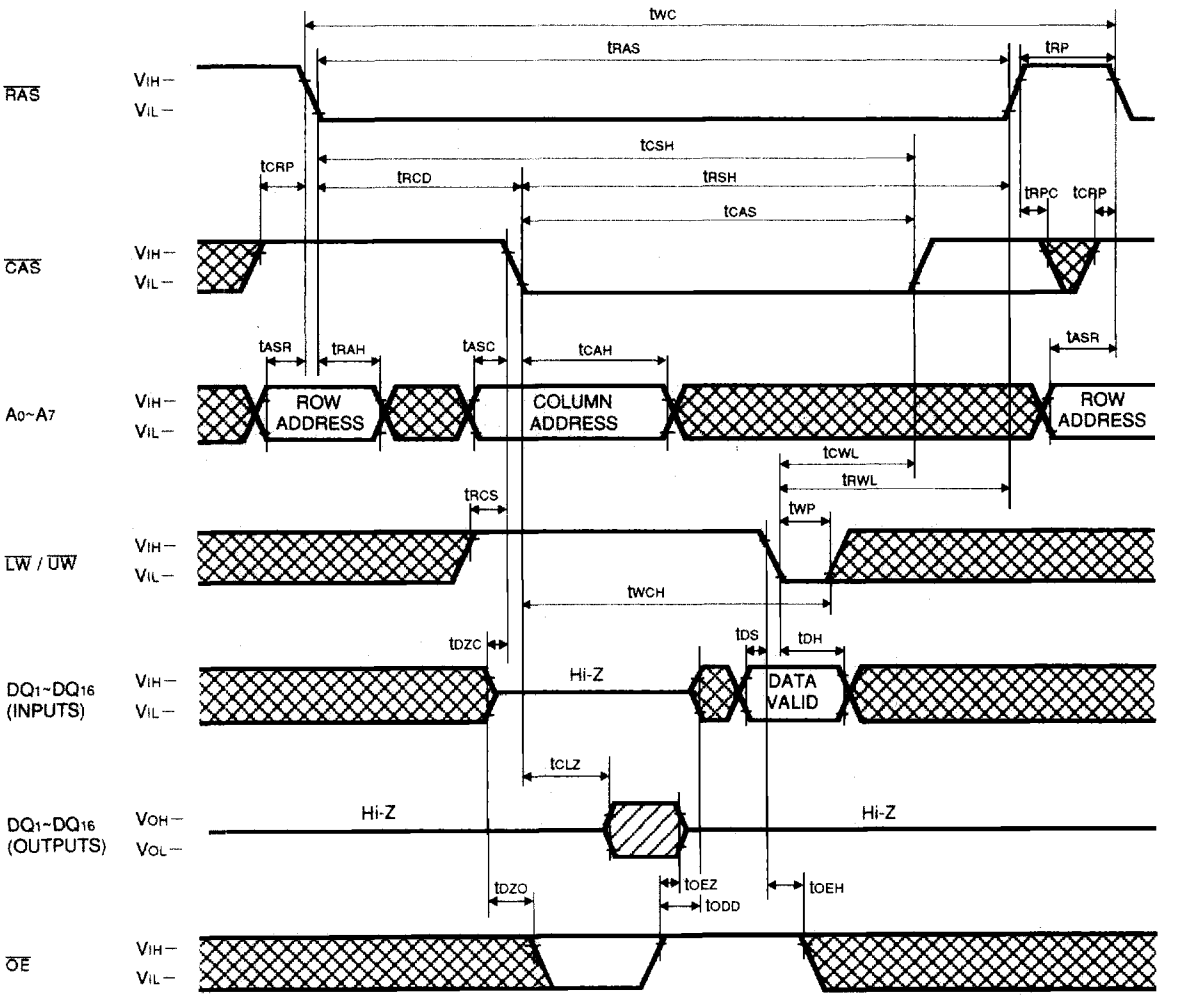
**Early Write Cycle**



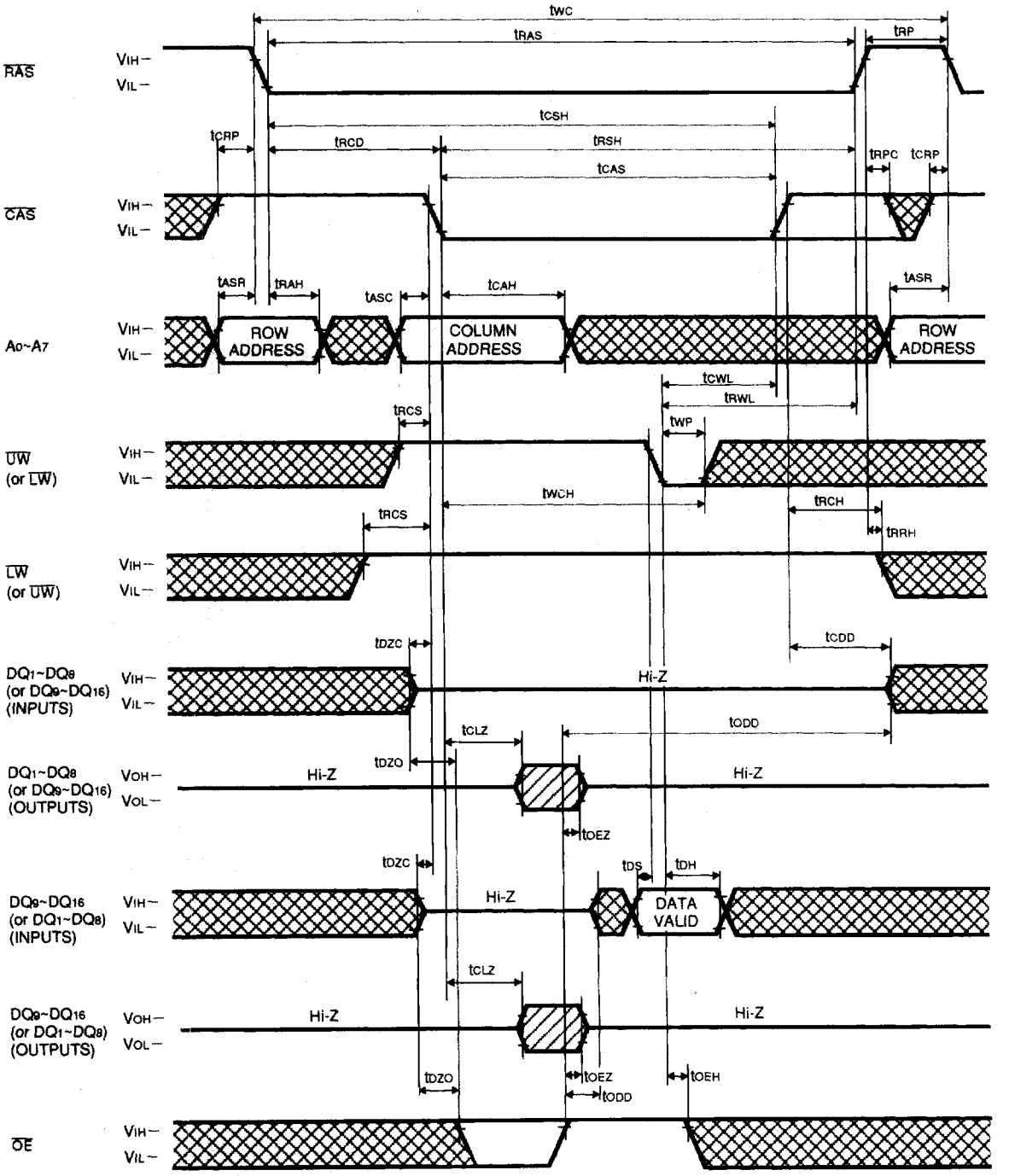
**Byte Early Write Cycle**



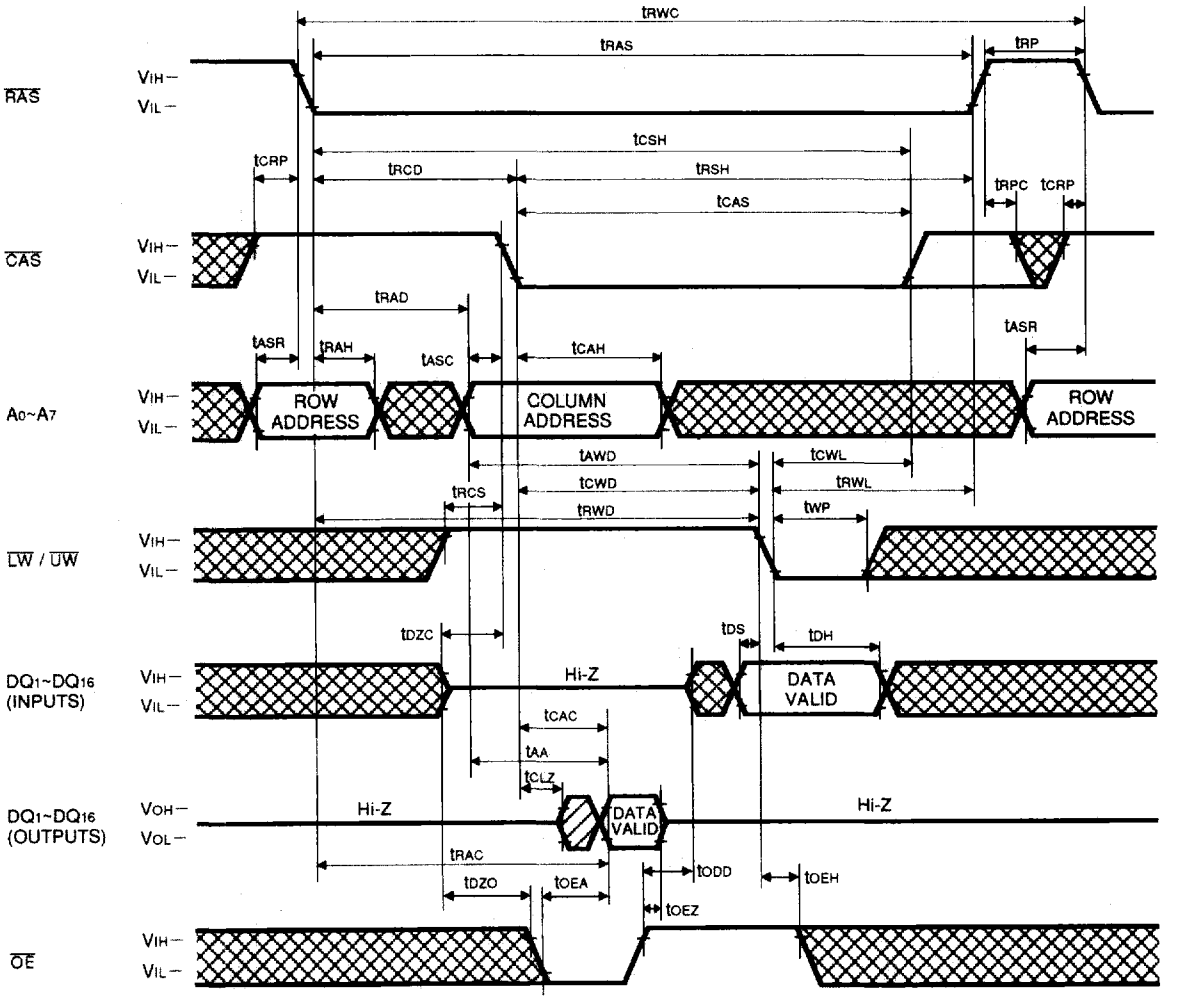
**Delayed Write Cycle**



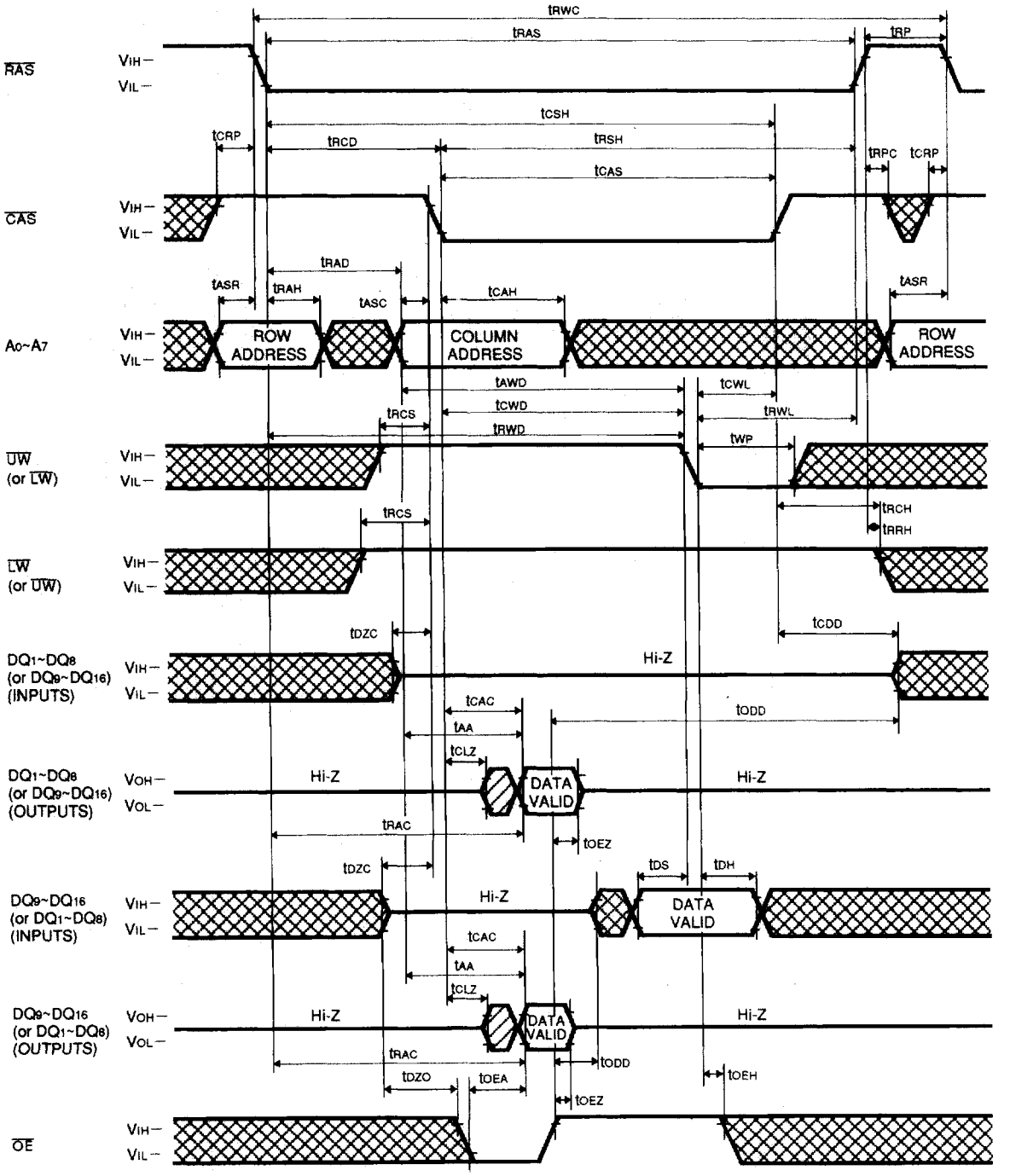
**Byte Delayed Write Cycle**



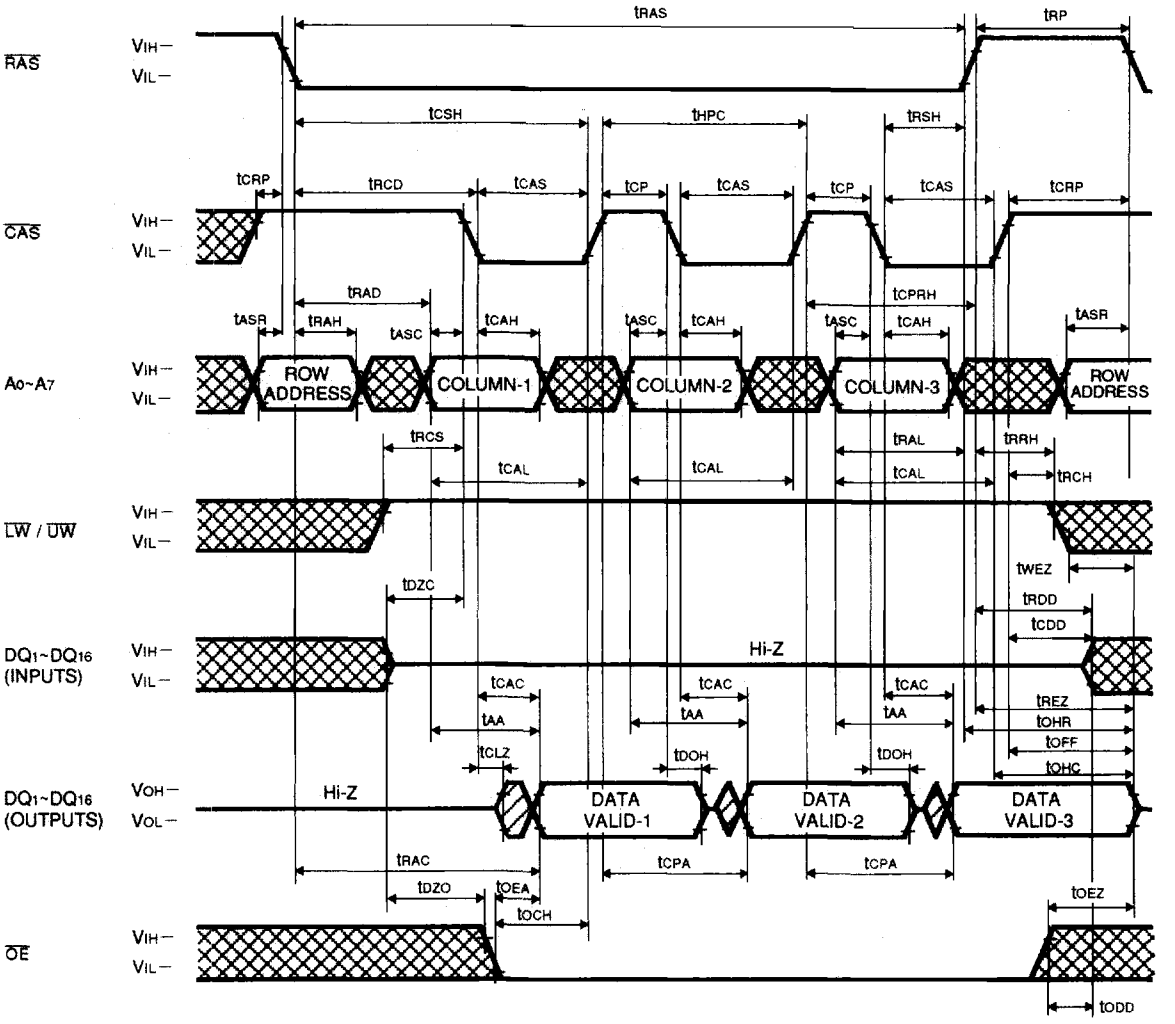
**Read-Write, Read-Modify-Write Cycle**



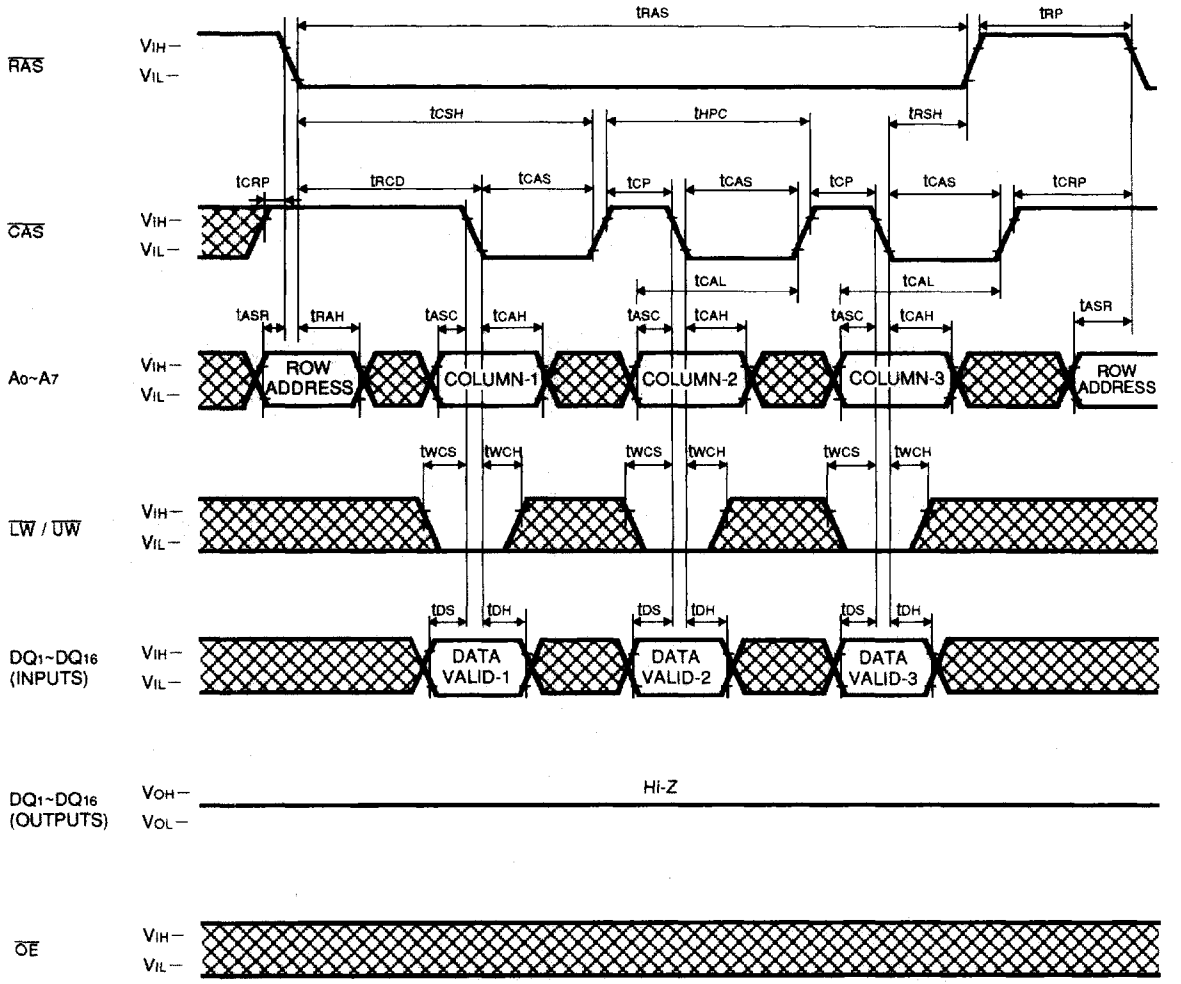
**Byte Read-Write, Read-Modify-Write Cycle**



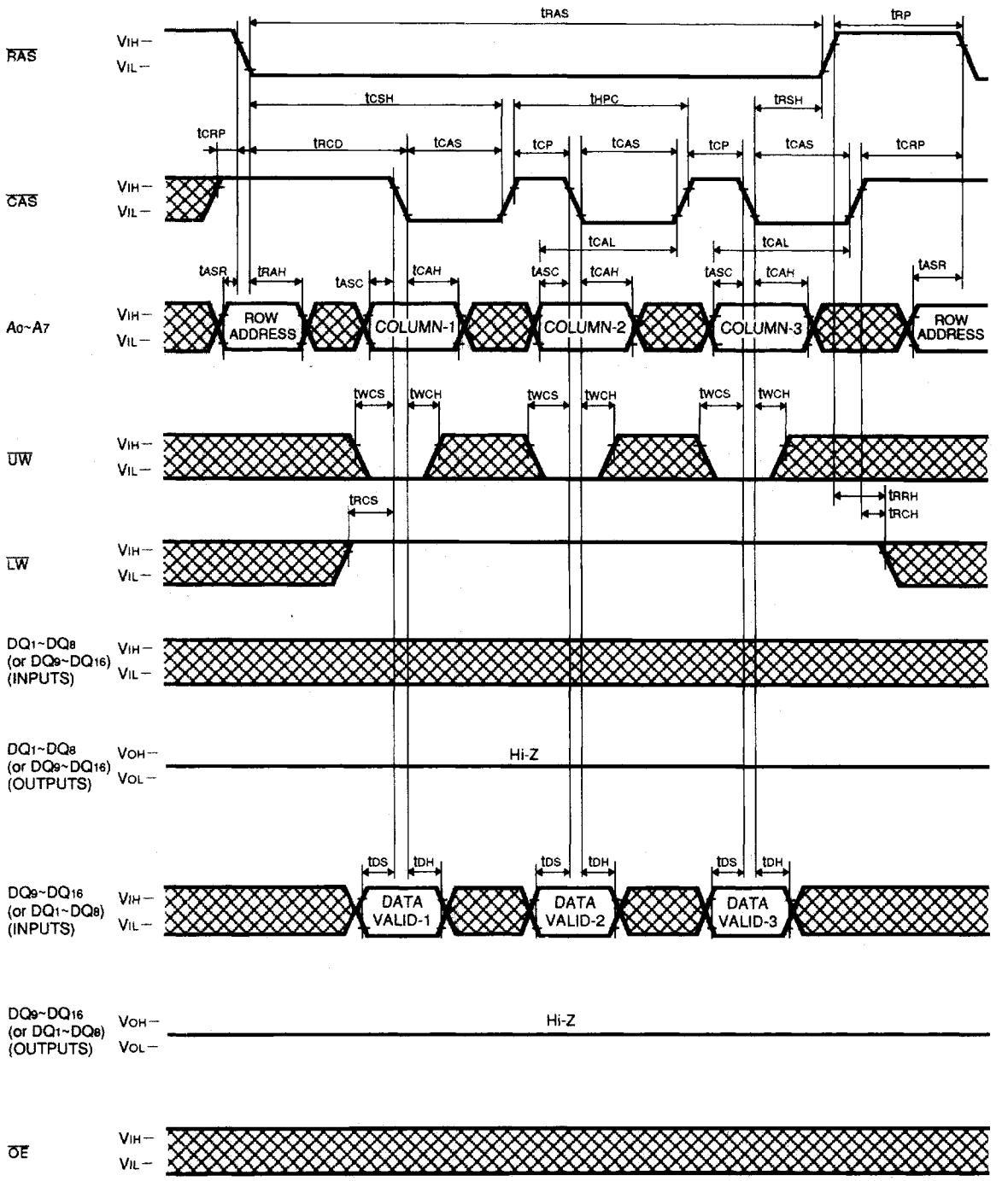
**Hyper Page Mode Read Cycle**



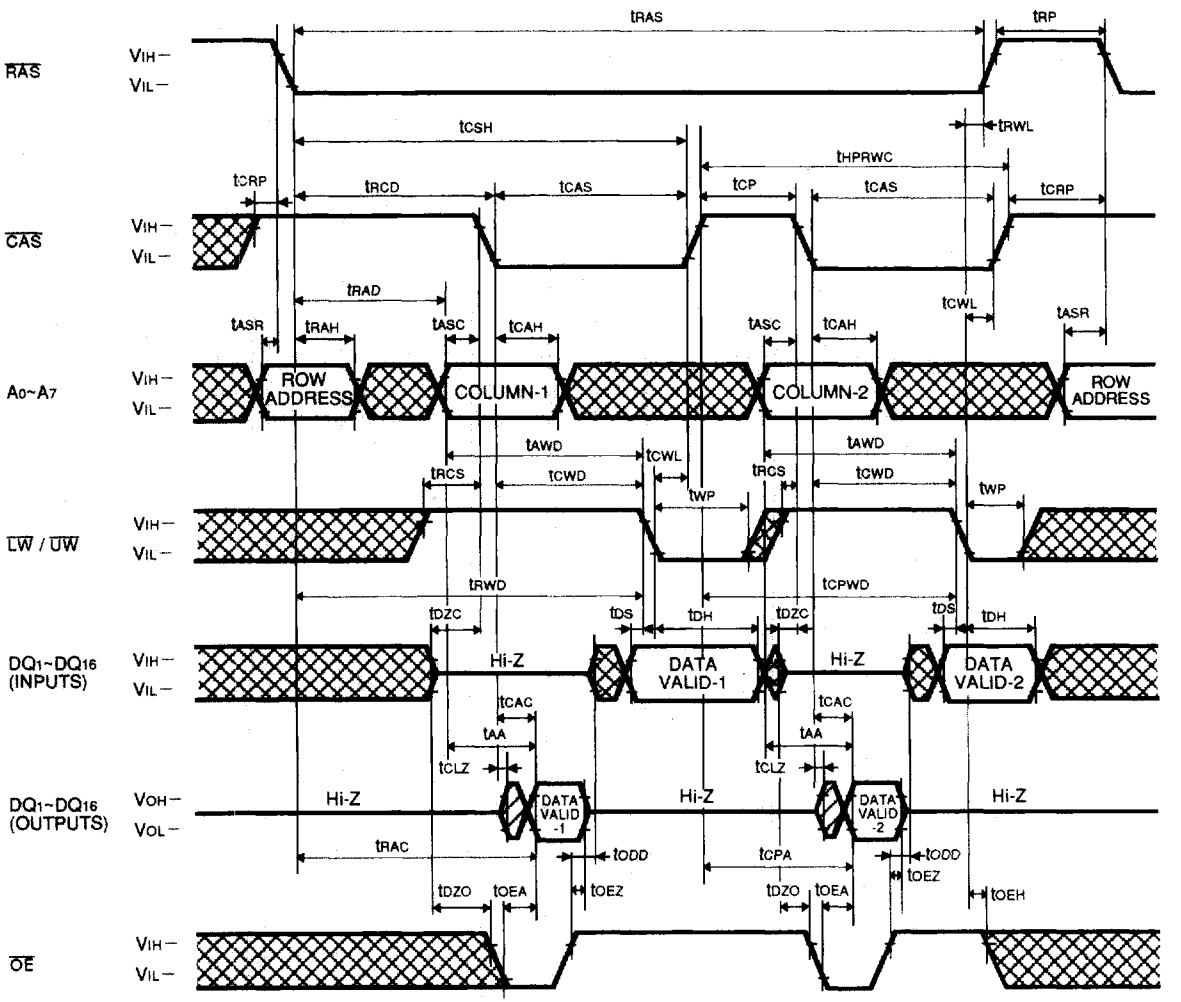
**Hyper Page Mode Early Write Cycle**



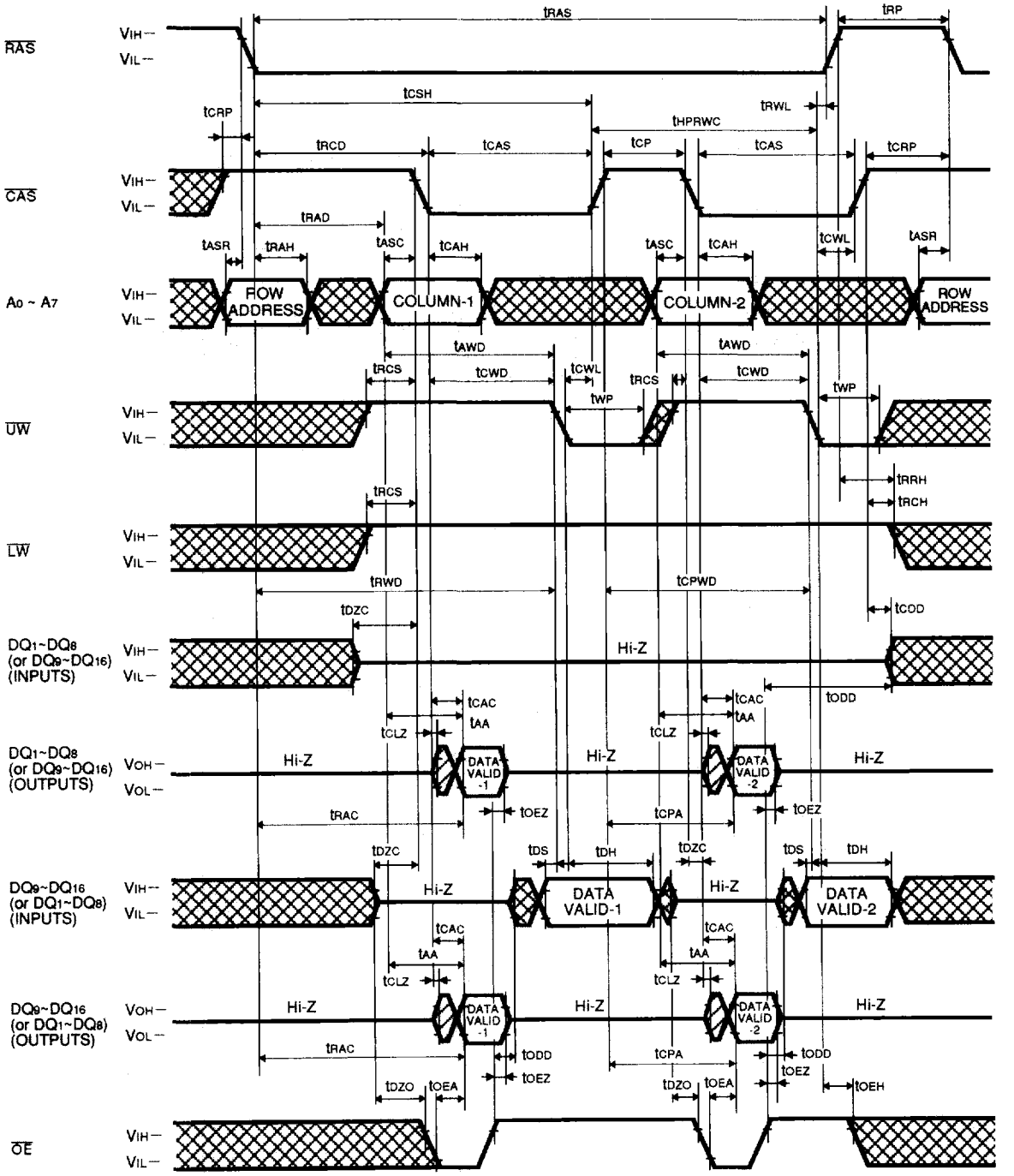
**Hyper Page Mode Byte Early Write Cycle**



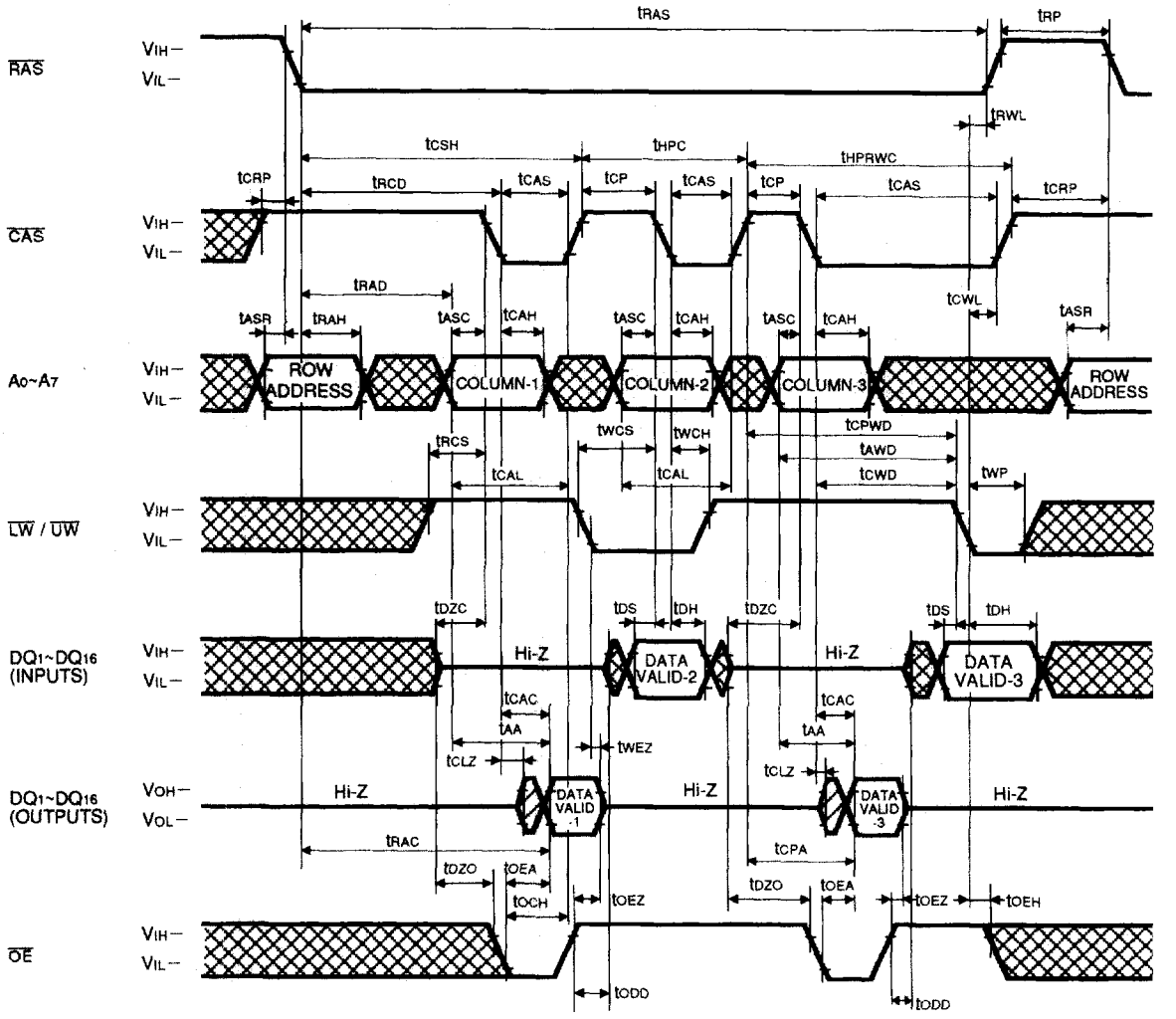
**Hyper Page Mode Read-Write, Read-Modify-Write Cycle**



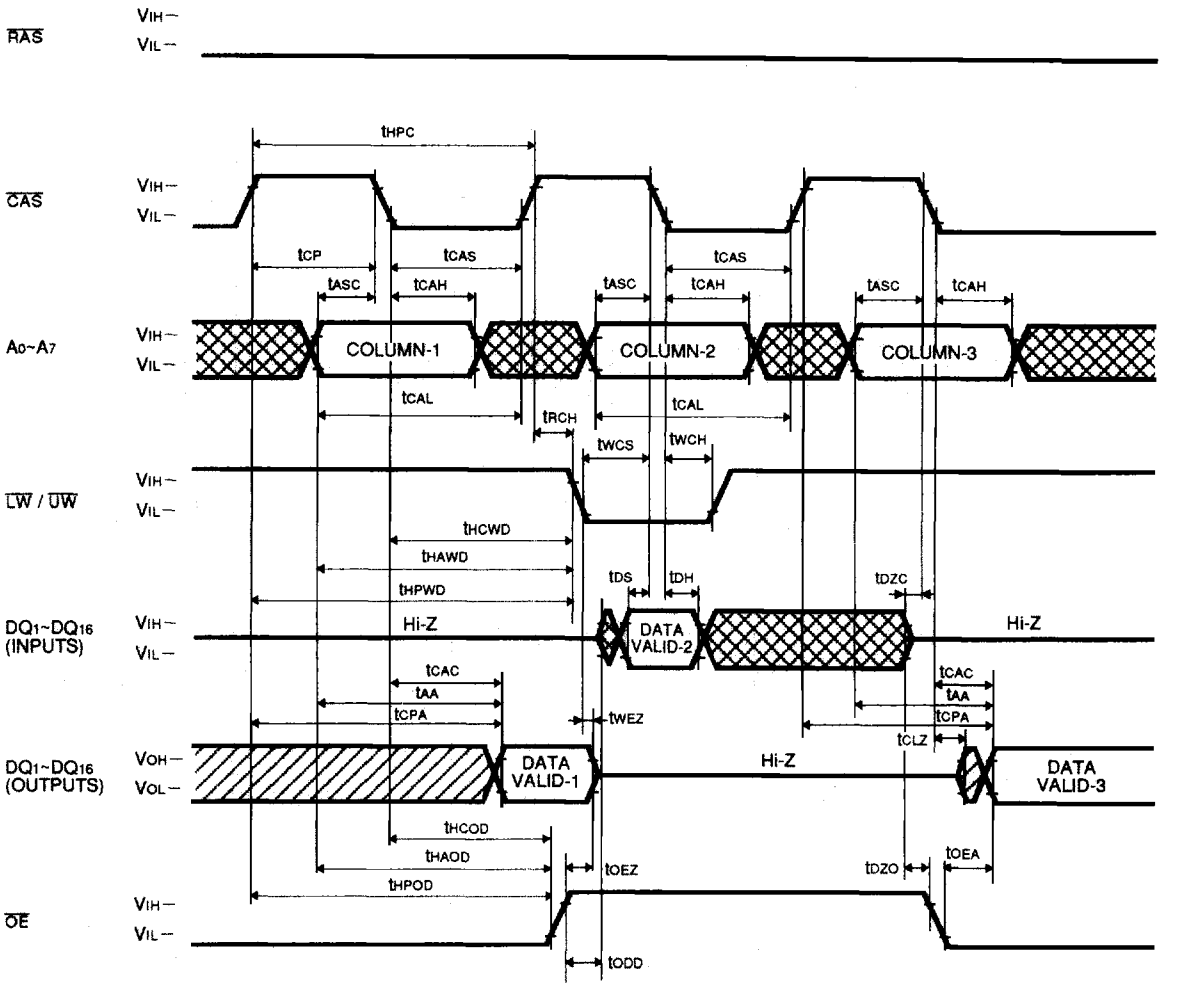
**Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle**



**Hyper Page Mode Mix Cycle (1)**



**Hyper Page Mode Mix Cycle (2)**




M5M411665AJ,TP2,TP3 -5,-5S : Under development



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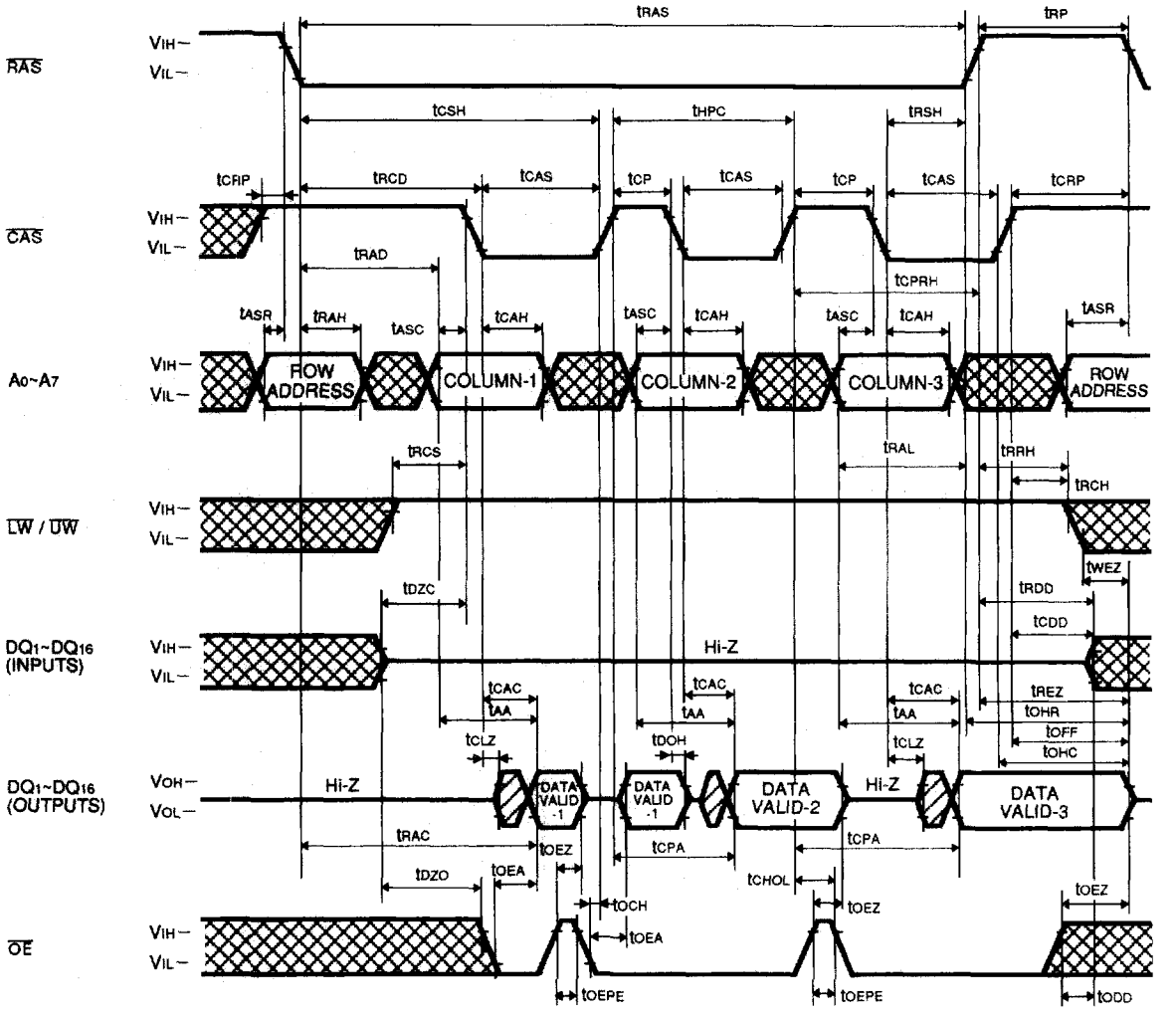
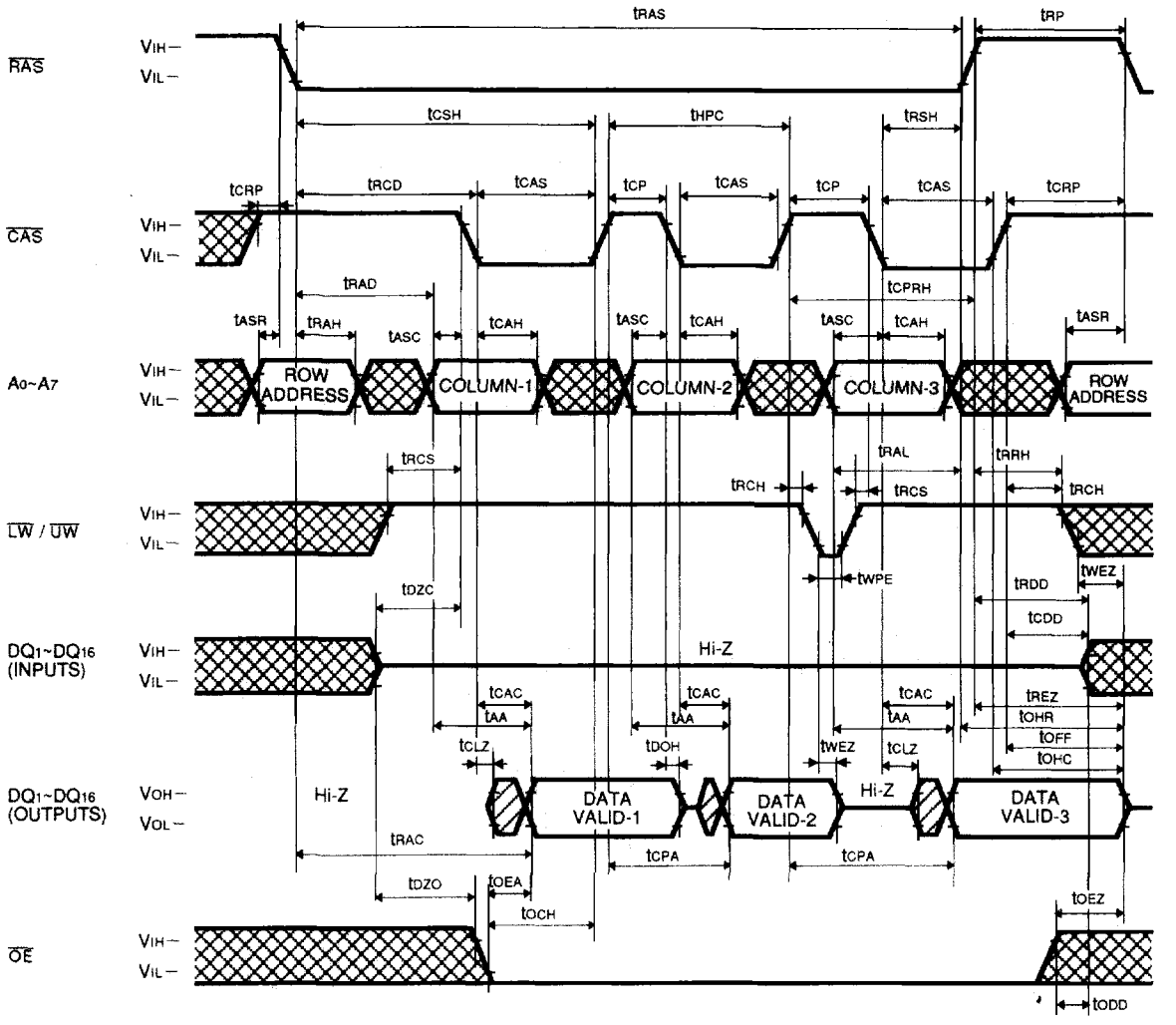
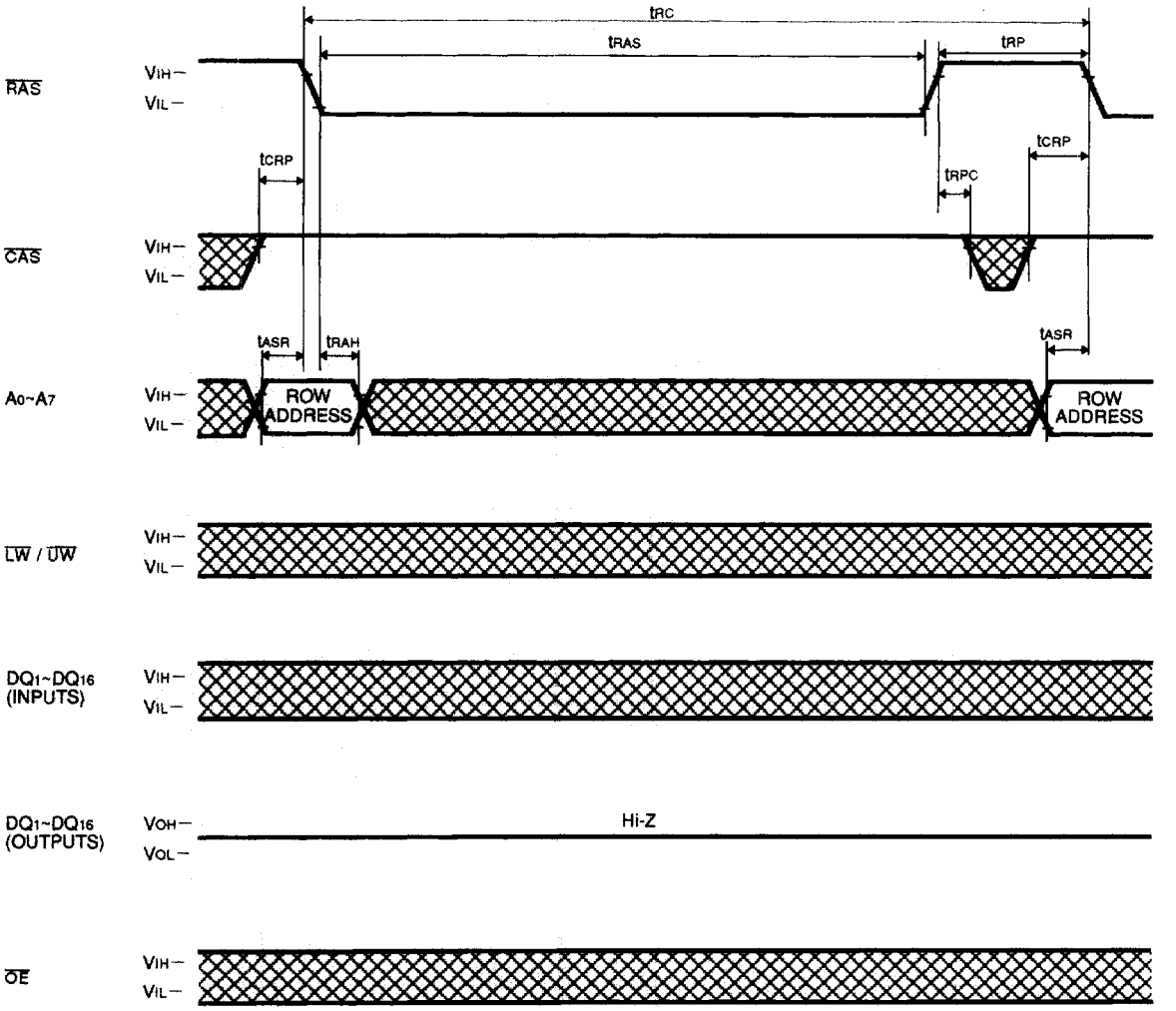
**Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)**



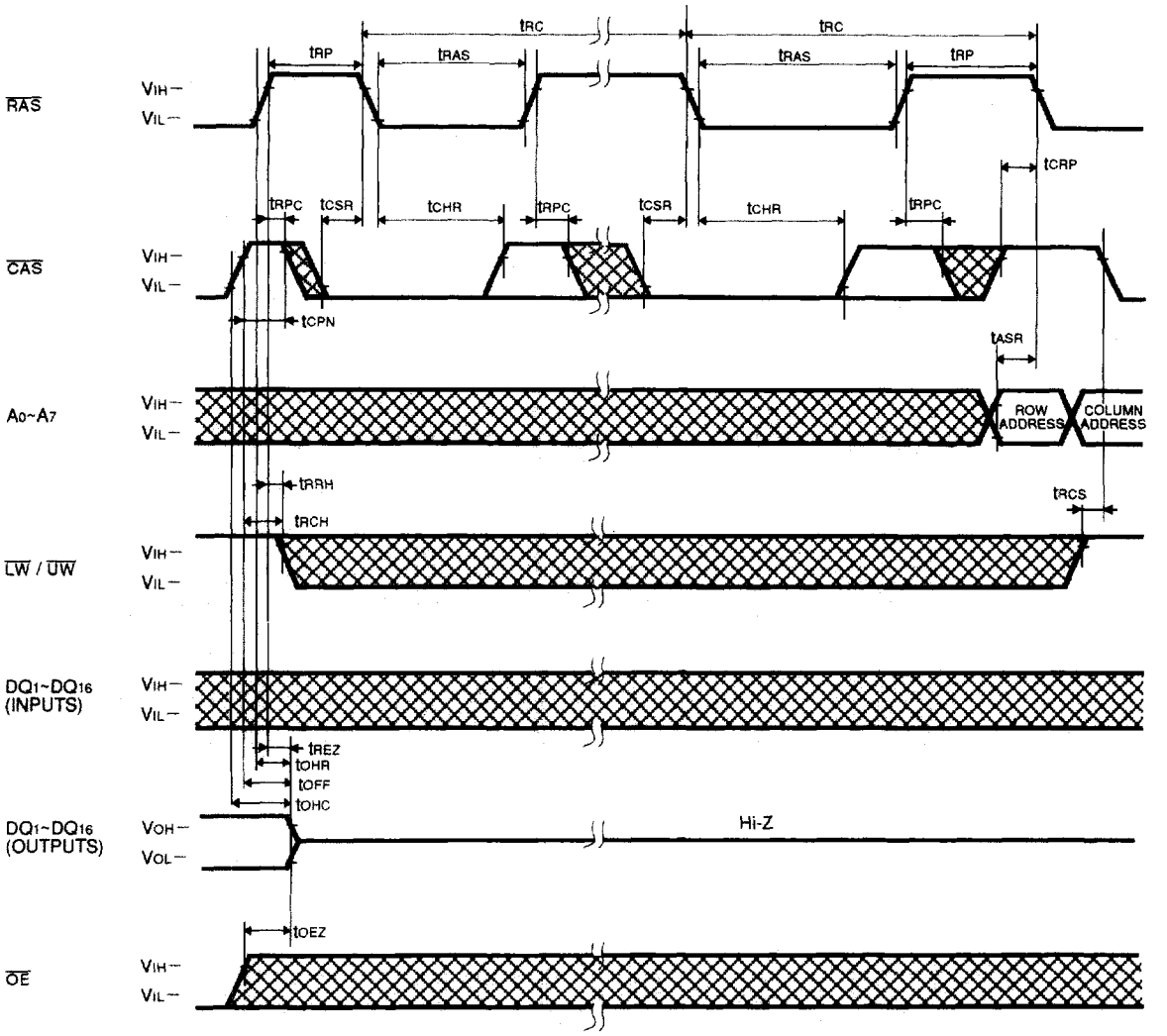
**Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)**



**$\overline{RAS}$-only Refresh Cycle**

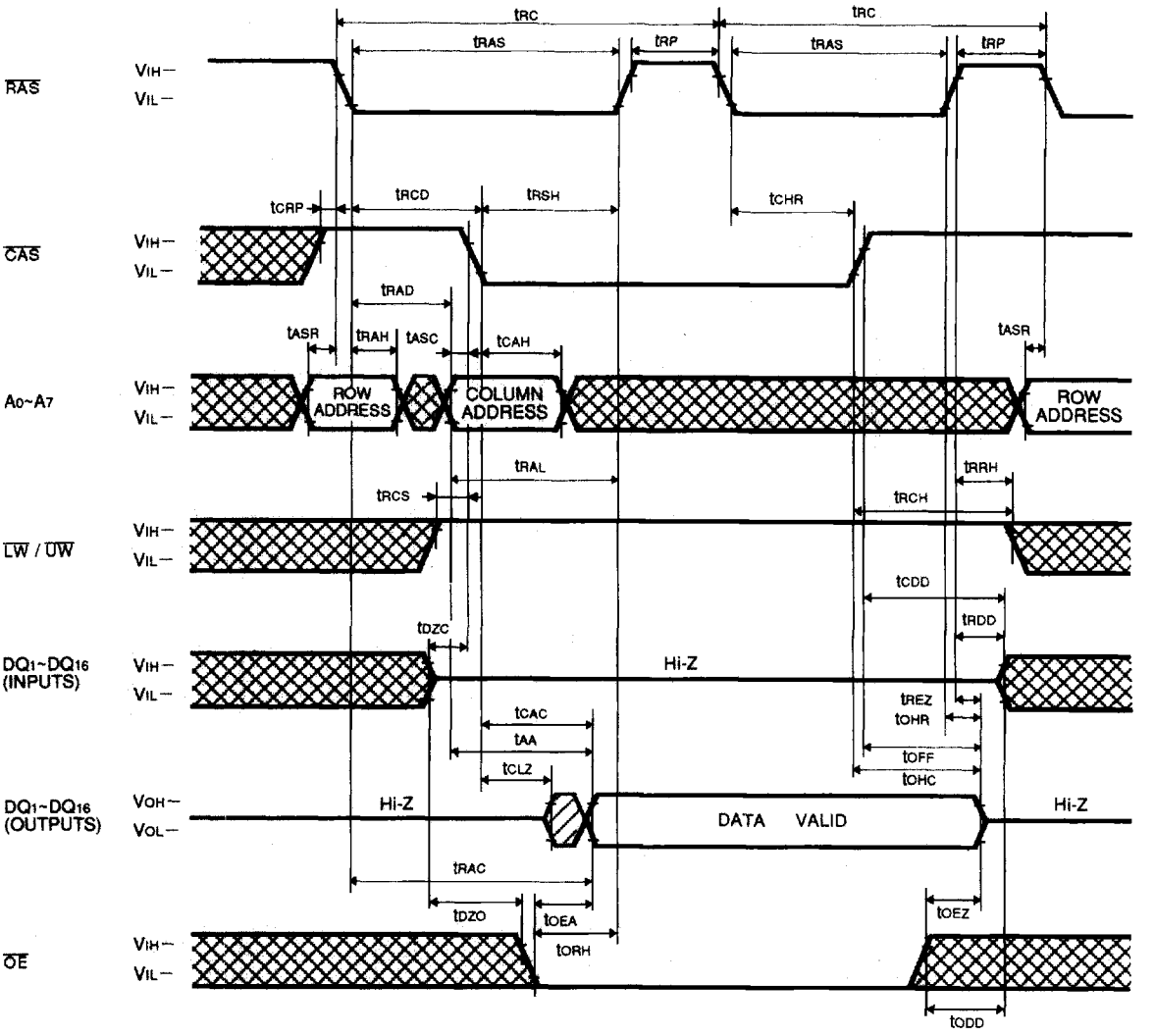


**$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle ***



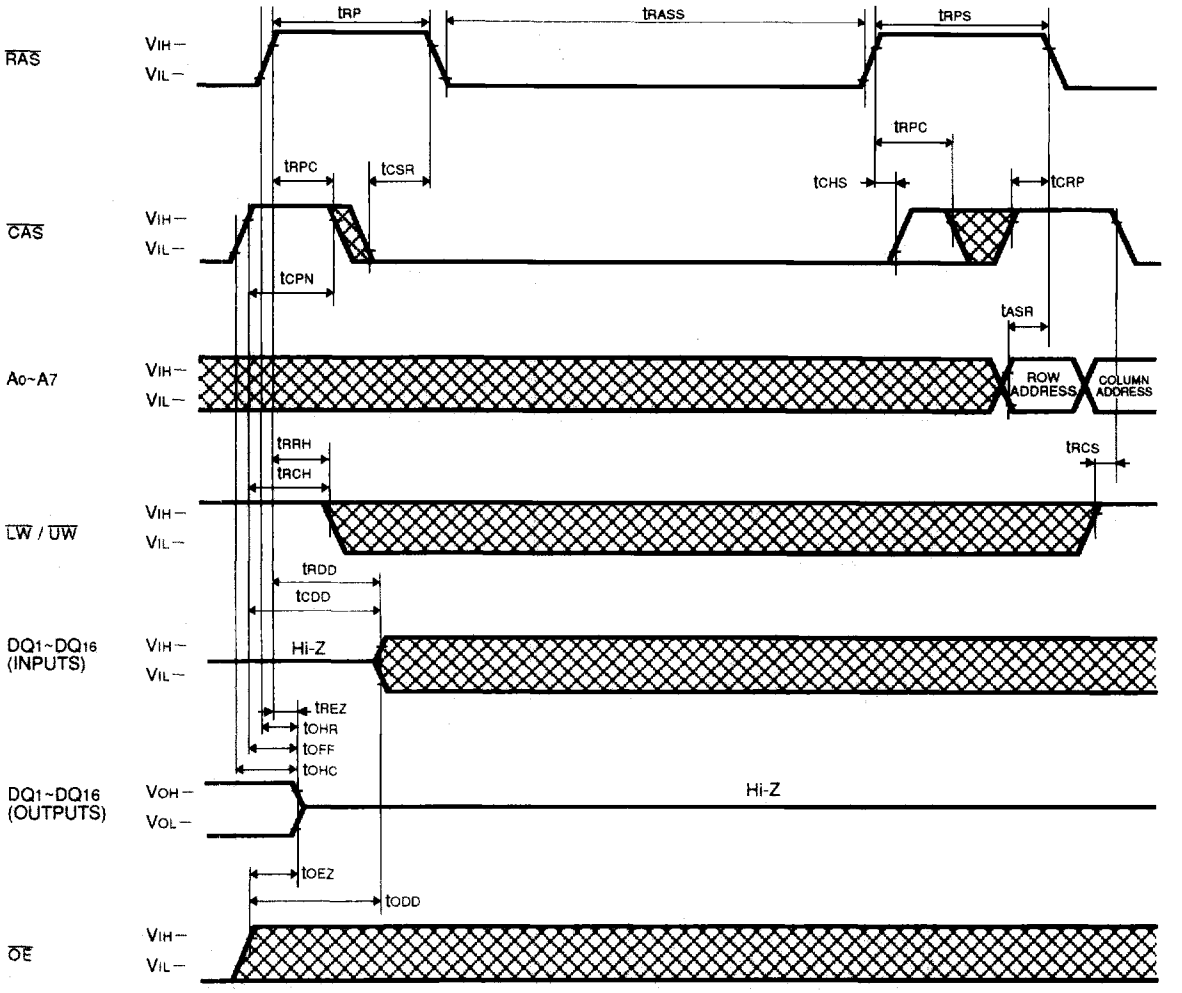

M5M411665AJ,TP2,TP3 -5,-5S : Under development

**Hidden Refresh Cycle (Read)** (Note 31)




*Note 31: Early write, delayed write, read write or read-modefy write cycle is applicable instead of read cycle.*
*Timing requirements and output state are the same as that of each cycle shown above.*

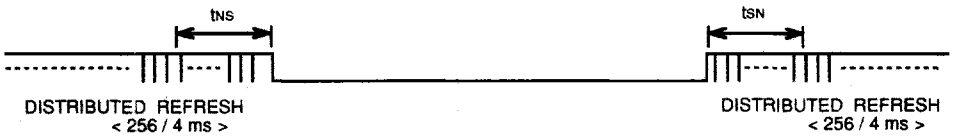
**Self Refresh Cycle** (Note 32)



Note32 : SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last and first full refresh cycles (256) must be done within $t_{NS}$ and $t_{SN}$ before and after self refresh, on the condition of $t_{NS} \leqq 4$ ms and $t_{SN} \leqq 4$ ms.




(2) In case of burst refresh

The last and first full refresh cycles (256) must be done within $t_{NS}$ and $t_{SN}$ before and after self refresh, on the condition of $t_{NS} \leqq 4$ ms and $t_{SN} \leqq 4$ ms.