M5M51004BP,J-15,-20,-25,-20L,-25L

1048576-BIT(262144-WORD BY 4-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51004BP,J are a family of 262144-word by 4-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M51004BP,J are offered in a 28-pin plastic dual-in-line package (DIP), 28-pin plastic small outline J-lead package (SOJ).

These devices operate on a single 5V supply, and are directly TTL compatible. They include power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M51004BP, J - 15	15ns	180mA	10mA
M5M51004BP, J - 20	20ns	160mA	
M5M51004BP, J - 20L			100μA
M5M51004BP, J - 25	25ns	140mA	10mA
M5M51004BP, J - 25L			100μA

- Single +5V power supply
- Fully static operation : No clocks, No refresh
- Common data I/O
- Easy memory expansion by $\overline{S}$
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

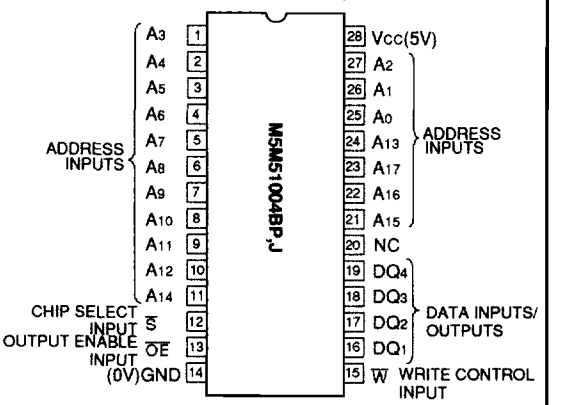
PACKAGE

M5M51004BP ..... 28pin 400mil DIP
M5M51004BJ ..... 28pin 400mil SOJ

APPLICATION

High speed memory units

PIN CONFIGURATION (TOP VIEW)



Outline 28P4F(P)
28P0K(J)

NC : NO CONNECTION

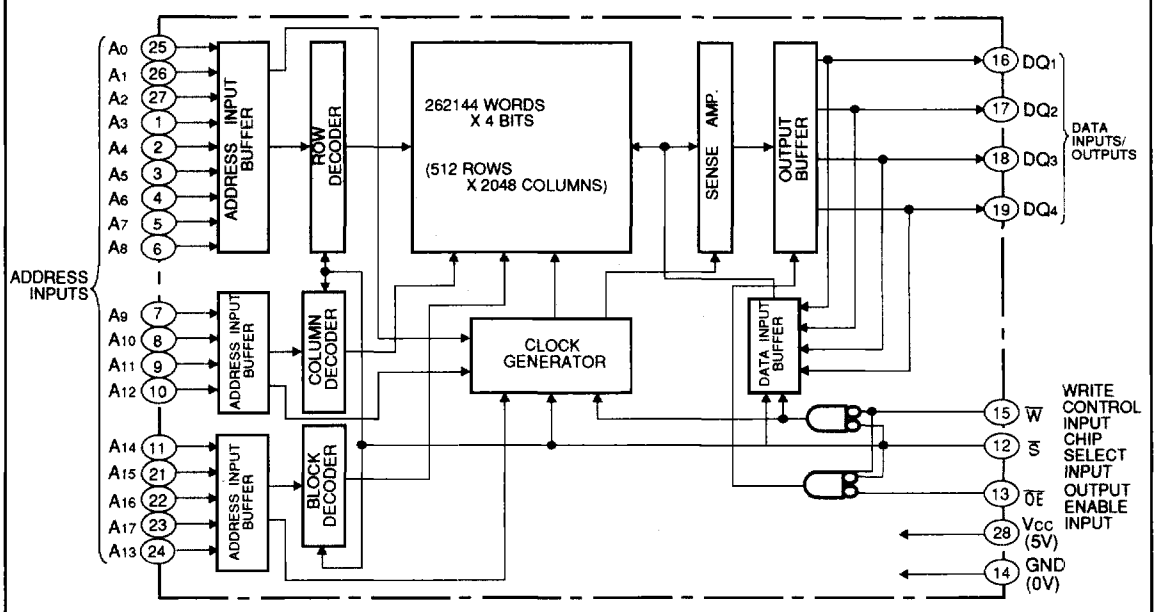
FUNCTION

The operation mode of the M5M51004B series is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$. Each mode is summarized in the function table shown in next page.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state ($\overline{S}$ = L)

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and write are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$.

Signal-S controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5* ~7	V
V_I	Input voltage		−3.5* ~ Vcc + 0.3	V
V_O	Output voltage		−3.5* ~ 7	V
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0 ~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	℃
T_{stg}	Storage temperature		−65 ~ 150	℃

* Pulse width≦20ns, in case of DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage				2.2		Vcc+0.3V	V
V_{IL}	Low-level input voltage				−0.3*		0.8	V
V_{OH}	High-level output voltage	I_{OH}=−4mA			2.4			V
V_{OL}	Low-level output voltage	I_{OL}=8mA					0.4	V
I_I	Input current	V_I=0~Vcc					2	μA
I_{OZ}	Output current in off-state	$V_{I(\overline{S})}$=V_{IH} $V_{I/O}$=0 ~ Vcc					10	μA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{S})}$=V_{IL} other inputs=V_{IH} or V_{IL} Output-open(duty 100%)	AC	15ns cycle			180	mA
				20ns cycle			160	
				25ns cycle			140	
			DC			60	75	
I_{CC2}	Stand-by supply current (TTL level)	$V_{I(\overline{S})}$=V_{IH}	AC (min cycle)				40	mA
			DC				30	
I_{CC3}	Stand-by current (MOS level)	$V_{I(\overline{S})}$≧Vcc−0.2V other inputs V_I≦0.2V or V_I≧Vcc−0.2V	-15,-20,-25			1	10	mA
			-20L,-25L			10	100	μA

* Pulse width≦20ns, in case of AC : −3.0V

CAPACITANCE (Ta = 0 ~ 70℃, Vcc = 5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			6	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V, Ta=25℃
3: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, Vcc = 5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· V_{IH} = 1.5V, V_{IL} = 1.5V
Reference levels ····· V_{OH} = 1.5V, V_{OL} =1.5V
Output loads ····· Fig1,Fig2

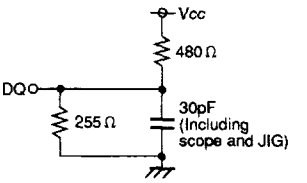


Fig.1 Output load

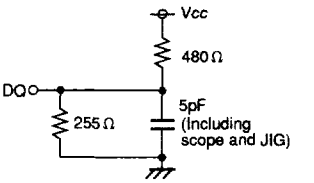


Fig.2 Output load for ten, tdis

(2) READ CYCLE

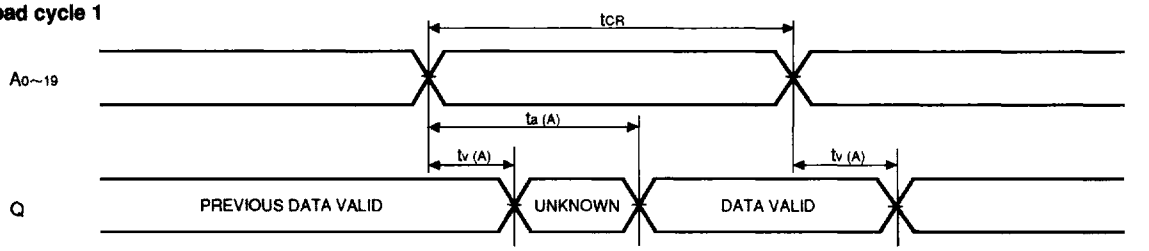
Symbol	Parameter	Limits						Unit
		M5M51004B-15		M5M51004B-20,-20L		M5M51004B-25,-25L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	15		20		25		ns
$t_{a(A)}$	Address access time		15		20		25	ns
$t_{a(S)}$	Chip select access time		15		20		25	ns
$t_{a(OE)}$	Output enable access time		8		10		13	ns
$t_{dis(S)}$	Output disable time after $\overline{S}_1$ high	0	7	0	7	0	8	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
$t_{en(S)}$	Output enable time after $\overline{S}$ low	6		6		6		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{v(A)}$	Data valid time after address change	7		7		7		ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		15		20		25	ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M51004B-15		M5M51004B-20,-20L		M5M51004B-25,-25L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	15		20		25		ns
$t_{w(W)}$	Write pulse width	12		15		20		ns
$t_{su(A)}$	Address setup time	0		0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	12		15		20		ns
$t_{su(S)}$	Chip select setup time	12		15		20		ns
$t_{su(D)}$	Data setup time	8		12		15		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	7	0	7	0	8	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	7	0	7	0	8	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns

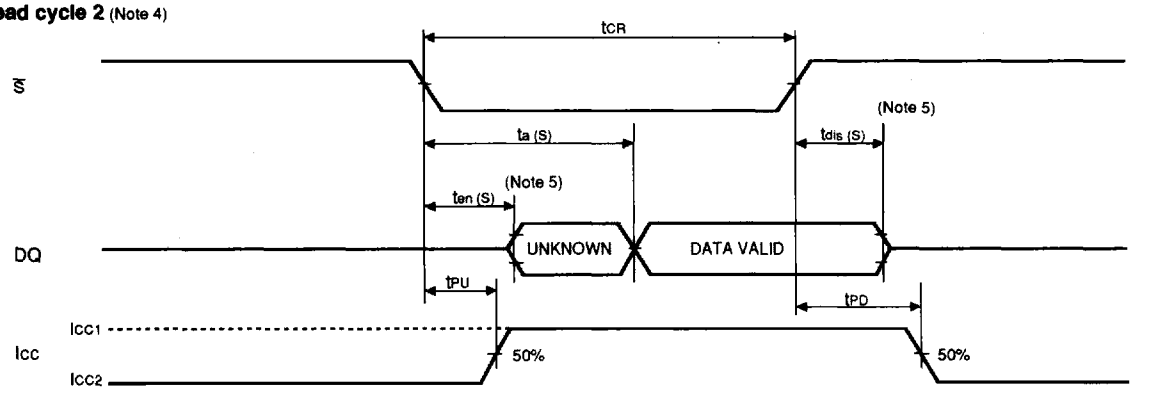
(4) TIMING DIAGRAMS

Read cycle 1



$\overline{W}$ = H
$\overline{S}$ = L
$\overline{OE}$ = L

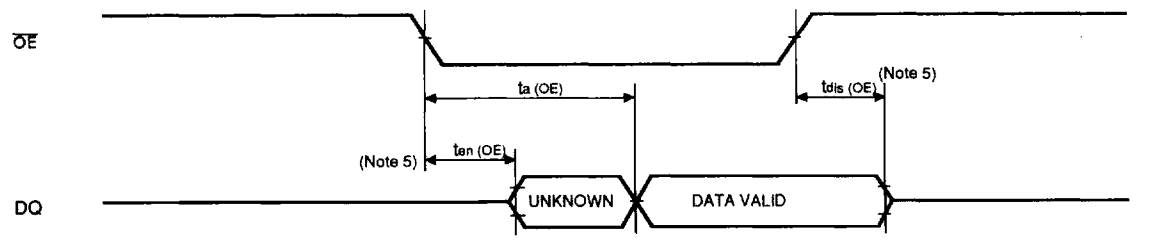
Read cycle 2 (Note 4)



$\overline{W}$ = H
$\overline{OE}$ = L

Note 4 : Addresses valid *prior to or coincident with* $\overline{S}$ transition low.
5 : Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

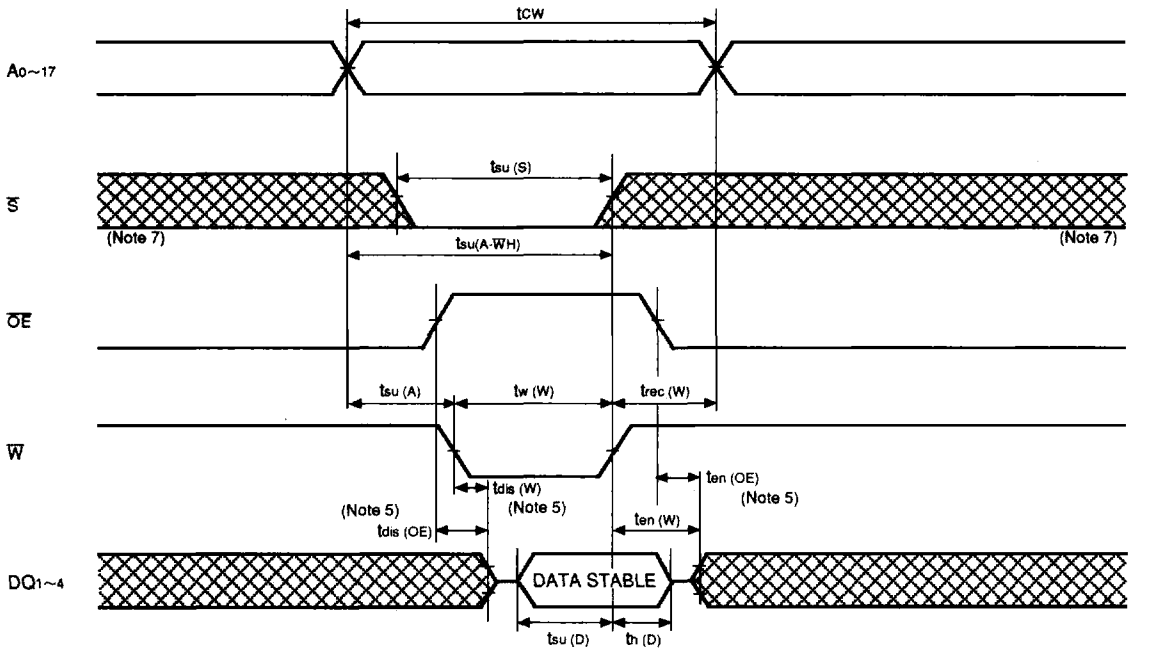
Read cycle 3 (Note 6)



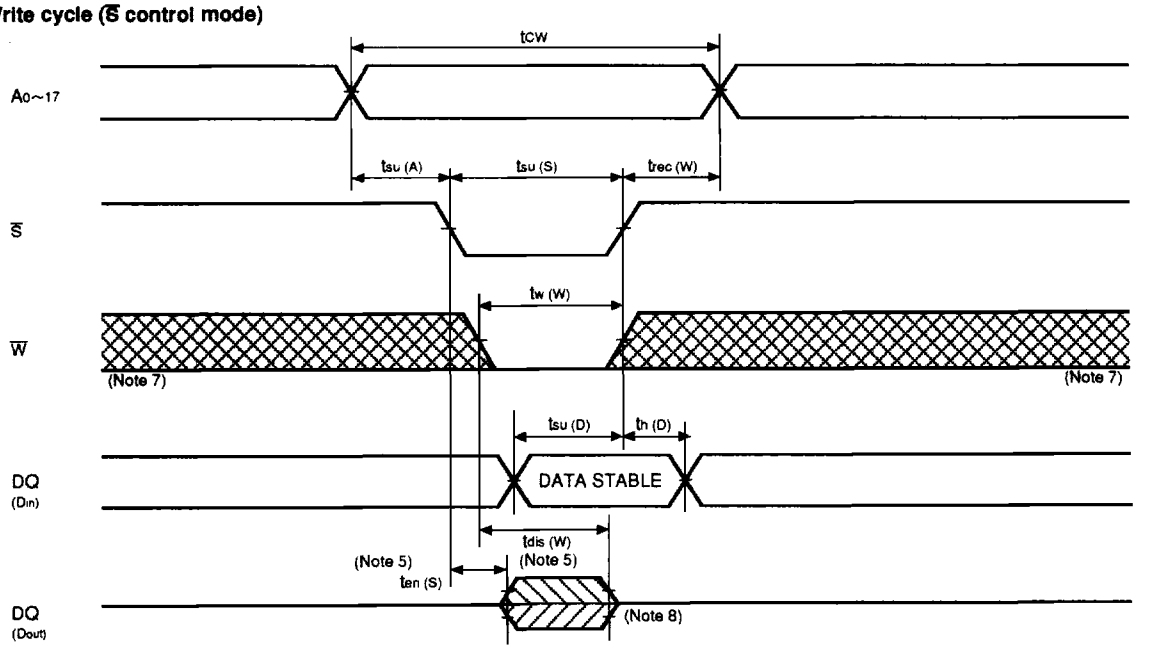
$\overline{W}$ = H
$\overline{S}$ = L

Note 6 : Addresses and $\overline{S}$ valid prior to $\overline{OE}$ transition low by (ta (A)-ta (OE)), (ta (S)-ta (OE)).

Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{S}$ control mode)



Note 7 : Hatching indicates the state is don't care.

8 : When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

9 : ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (Ta = 0 ~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage	$V_{I(\overline{S})} \geqq V_{CC} - 0.2V$ $V_I \geqq V_{CC} - 0.2V$ or $0V \leqq V_I \leqq 0.2V$		2			V
$V_{I(\overline{S})}$	Chip select input voltage			$V_{CC} - 0.2$			V
$t_{su\ (PD)}$	Power down setup time			0			ns
$t_{rec\ (PD)}$	Power down recovery time		-20L	20			ns
			-25L	25			
$I_{CC\ (PD)}$	Power down supply current	V_{CC} = 3.0V				50	μA
		V_{CC} = 5.5V				100	

Note 10 : This is only M5M51004BP, J-20L, -25L.

TIMING WAVEFORM FOR POWER DOWN