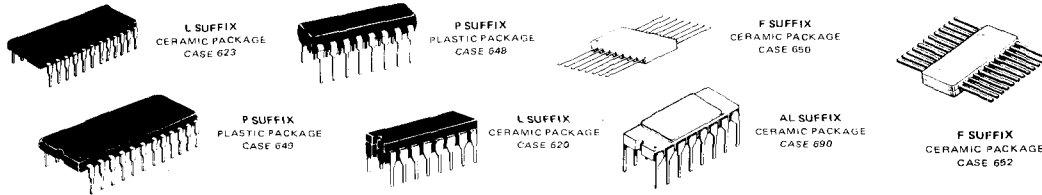


MC10,100/10,200 Series (-30 to +85°C)  
MC10,500/10,600 Series (-55 to +125°C)

MECL 10,000 has an excellent speed-power product, has relatively slow rise and fall times, and transmission-line drive capability. The combination of versatile logic functions and the 2.0 ns propagation delay make MECL 10,000 a versatile family for data handling and processing systems.

Circuit design with MECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. MECL III is directly compatible with MECL 10,000, and can be used to extend the speed capability of the MECL 10,000 series.



### FUNCTIONS AND CHARACTERISTICS ( $V_{CC} = 0, V_{EE} = -5.2 \text{ V}, T_A = 25^\circ\text{C}$ )

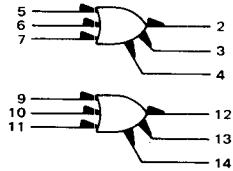
Function	Type ①		Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
	-30 to +85°C	-55 to +125°C			
Quad 2-Input NOR Gate With Strobe	MC10100	-	2.0	100	620
Quad OR/NOR Gate	MC10101	MC10501	2.0	100	620,648,650
Quad 2-Input NOR Gate	MC10102	MC10502	2.0	100	620,648,650
Quad 2-Input OR Gate	MC10103	-	2.0	100	620
Quad 2-Input AND Gate	MC10104	MC10504	2.7	140	620,648,650
Triple 2-3-2-Input OR/NOR Gate	MC10105	MC10505	2.0	90	620,648,650
Triple 4-3-3-Input NOR Gate	MC10106	MC10506	2.0	90	620,648,650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	2.5	110	620,648,650
Dual 4-5-Input OR/NOR Gate	MC10109	MC10509	2.0	60	620,648,650
Dual 3-Input 3-Output OR Gate	MC10110	-	2.4	160	620,648
Dual 3-Input 3-Output NOR Gate	MC10111	-	2.4	160	620,648
Quad Exclusive OR Gate	MC10113	-	2.5	175	620
Triple Line Receiver	MC10114	MC10514	2.4	145	620,648,650
Quad Line Receiver	MC10115	MC10515	2.0	110	620,648,650
Triple Line Receiver	MC10116	MC10516	2.0	85	620,648,650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate	MC10117	MC10517	2.3	100	620,648,650
Dual 2-Wide 3-Input OR-AND Gate	MC10118	MC10518	2.3	100	620,648,650
4-Wide 4-3-3-Input OR-AND Gate	MC10119	MC10519	2.3	100	620,648,650
4-Wide OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	2.3	100	620,648,650
Triple 4-3-3-Input Bus Driver	MC10123	-	3.0	310	620
Quad MTTL to MECL Translator	MC10124	MC10524	3.5	380	620,648,650
Quad MECL to MTTL Translator	MC10125	MC10525	4.5	380	620,648,650
Dual MECL to MOS Translator	MC10127	-	-	-	620
Bus Driver	MC10128	-	12.0	700	620
Quad Bus Receiver	MC10129	-	10.0	750	620
Dual Latch	MC10130	MC10530	2.5	155	620,648,650
Dual Type D Master-Slave Flip-Flop	MC10131	MC10531	f = 160 MHz	235	620,648,650
Dual Multiplexer With Latch and Common Reset	MC10132	-	3.0	225	620,648
Quad Latch	MC10133	MC10533	4.0	310	620,648,650
Multiplexer with Latch	MC10134	-	3.0	225	620,648
Dual J-K Master-Slave Flip-Flop	MC10135	MC10535	f = 140 MHz	280	620,648,650
Universal Hexadecimal Counter	MC10136	MC10536	f = 150 MHz	625	620,650

① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

\*External Load Power not included.

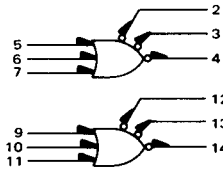
**GATES** (continued)

**MC10110  
MC10210**  
Dual 3-Input 3-Output  
OR Gate



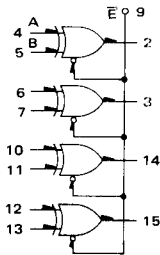
$P_D = 160$  mW typ/pkg (No Load)  
MC10110  
 $t_{pd} = 2.4$  ns typ  
MC10210  
 $t_{pd} = 1.5$  ns typ

**MC10111  
MC10211**  
Dual 3-Input 3-Output  
NOR Gate



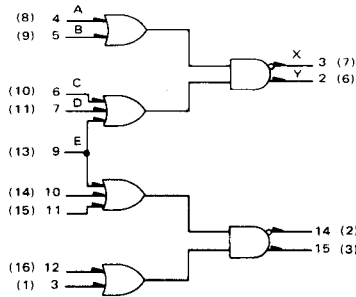
$P_D = 160$  mW typ/pkg (No Load)  
MC10111  
 $t_{pd} = 2.4$  ns typ  
MC10211  
 $t_{pd} = 1.5$  ns typ

**MC10113**  
Quad Exclusive  
OR Gate



$P_D = 175$  mW typ/pkg (No Load)  
 $t_{pd} = 2.5$  ns typ

**MC10117  
MC10517**  
Dual 2-Wide 2-3-Input  
OR-AND/OR-AND-INVERT  
Gate

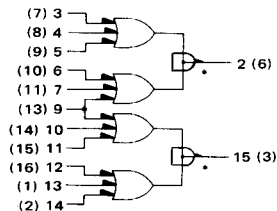


$P_D = 100$  mW typ/pkg (No Load)  
 $t_{pd} = 2.3$  ns typ

$$Y = (A + B) \bullet (C + D + E)$$

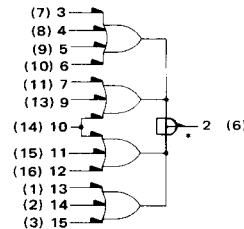
$$X = (A + B) \bullet (C + D + E)$$

**MC10118  
MC10518**  
Dual 2-Wide 3-Input  
OR-AND Gate



\*Collector Dot  
 $P_D = 100$  mW typ/pkg (No Load)  
 $t_{pd} = 2.3$  ns typ

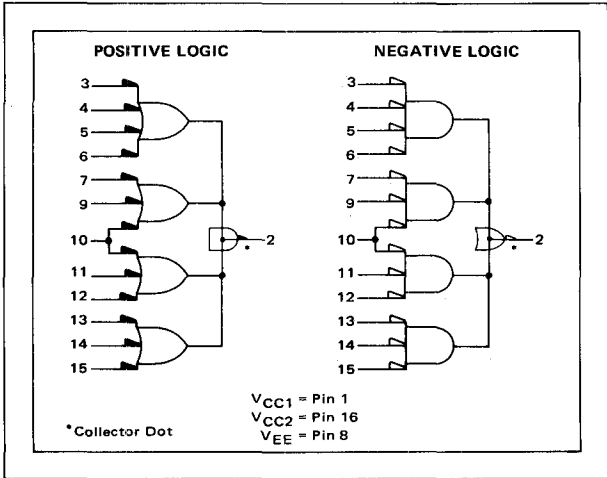
**MC10119  
MC10519**  
4-Wide 4-3-3-3 Input  
OR-AND-Gate



\*Collector Dot  
 $P_D = 100$  mV type/pkg (No Load)  
 $t_{pd} = 2.3$  ns typ

4-WIDE 4-3-3-3 INPUT  
"OR-AND" GATE

MC10119

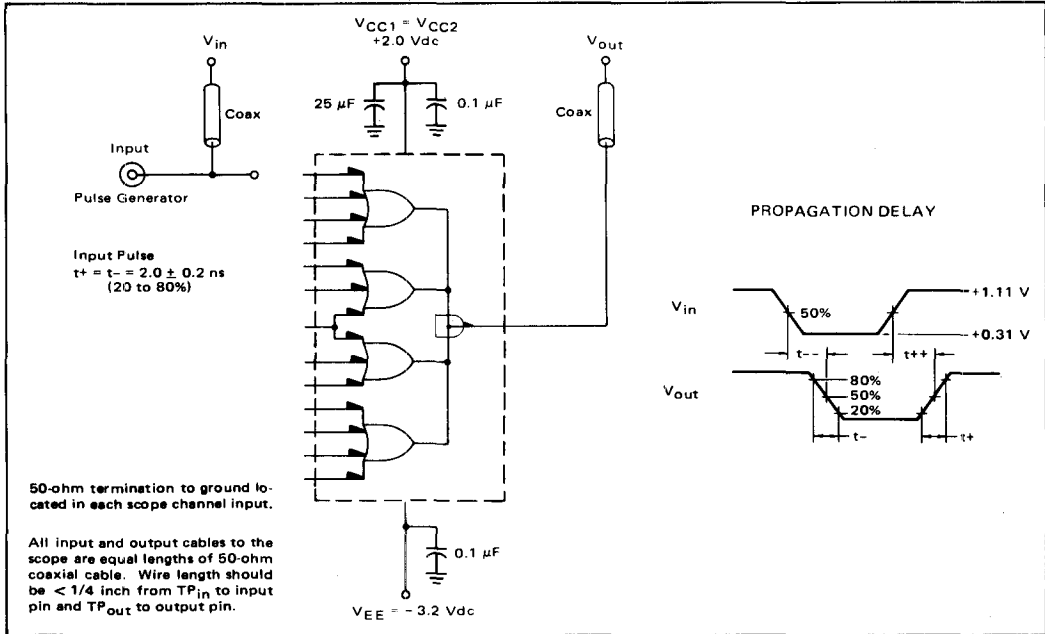


The MC10119 is a 4-Wide 4-3-3-3 Input OR-AND gate with one input from two gates common to pin 10. Input pulldown resistors eliminate the need to tie unused inputs to an external supply.

$P_D = 100 \text{ mW typ/pkg (No Load)}$   
 $t_{pd} = 2.3 \text{ ns typ}$   
 Output Rise and Fall Time:  
 = 3.5 ns typ (10% - 90%)  
 = 2.5 ns typ (20% - 80%)



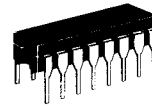
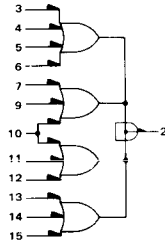
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



See General Information section for packaging.

## ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

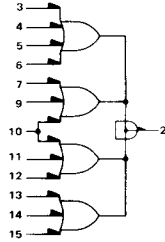


L SUFFIX  
CERAMIC PACKAGE  
CASE 620

Characteristic	Symbol	Pin Under Test	MC10119L Test Limits						TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					(V <sub>CC</sub> ) Gnd		
			-30°C		+25°C		+85°C		V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>ILA</sub> max	V <sub>EE</sub>			
			Min	Max	Min	Typ	Max	Min							Max	Unit
Power Supply Drain Current	I <sub>E</sub>	8	—	—	—	20	26	—	—	mAdc	—	—	—	—	8	1,16
Input Current	I <sub>in</sub> H	7	—	—	—	—	265	—	—	μAdc	7	—	—	—	8	1,16
		9	—	—	—	—	265	—	—	μAdc	9	—	—	—	↓	↓
		10	—	—	—	—	370	—	—	μAdc	10	—	—	—	↓	↓
Input Current	I <sub>in</sub> L	7	—	—	0.5	—	—	—	—	μAdc	—	7	—	—	8	1,16
		9	—	—	↓	—	—	—	—	μAdc	—	9	—	—	↓	↓
		10	—	—	—	—	—	—	—	μAdc	—	10	—	—	↓	↓
Logic "1" Output Voltage	V <sub>OH</sub>	2	-1.060	-0.890	-0.960	—	-0.810	-0.890	-0.700	Vdc	3,10,15	—	—	—	8	1,16
Logic "0" Output Voltage	V <sub>OL</sub>	2	-2.000	-1.675	-1.990	—	-1.650	-1.920	-1.615	Vdc	—	—	—	—	8	1,16
Logic "1" Threshold Voltage	V <sub>OHA</sub>	2	-1.080	—	-0.980	—	—	-0.910	—	Vdc	10,15	—	—	3	8	1,16
Logic "0" Threshold Voltage	V <sub>OLA</sub>	2	—	-1.655	—	—	-1.630	—	-1.595	Vdc	—	—	—	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t <sub>3+2+</sub> t <sub>3-2-</sub>	2	1.4 1.4	3.9 3.9	1.4 1.4	2.3 2.3	3.4 3.4	1.4 1.4	3.8 3.8	ns	10,13	—	3	2	8	1,16
Rise Time (20 to 80%)	t <sub>r</sub>	↓	0.8	4.1	1.5	2.5	4.0	1.5	4.6	↓	↓	—	↓	↓	↓	↓
Fall Time (20 to 80%)	t <sub>f</sub>	↓	0.8	4.1	1.5	2.5	4.0	1.5	4.6	↓	↓	—	↓	↓	↓	↓

**ELECTRICAL CHARACTERISTICS**

Each MECL 10,000 series has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648

3-53

Characteristic	Symbol	Pin Under Test	MC10119P Test Limits							Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW:					(V <sub>CC</sub> ) Gnd
			-30°C		+25°C			+85°C			V <sub>IH</sub> max	V <sub>IL</sub> min	V <sub>IHA</sub> min	V <sub>IHA</sub> max	V <sub>EE</sub>	
			Min	Max	Min	Typ	Max	Min	Max							
Power Supply Drain Current	I <sub>E</sub>	8	-	-	-	20	26	-	-	mAdc	-	-	-	-	8	1,16
Input Current	I <sub>in</sub> H	7	-	-	-	-	265	-	-	μAdc	7	-	-	-	8	1,16
		9	-	-	-	-	265	-	-	↓	9	-	-	-	↓	↓
		10	-	-	-	-	370	-	-	↓	10	-	-	-	↓	↓
	I <sub>in</sub> L	7	-	-	0.5	-	-	-	-	μAdc	-	7	-	-	8	1,16
		9	-	-	↓	-	-	-	-	↓	-	9	-	-	↓	↓
		10	-	-	↓	-	-	-	-	↓	-	10	-	-	↓	↓
Logic "1" Output Voltage	V <sub>OH</sub>	2	-1.060	-0.890	-0.960	-	-0.810	-0.890	-0.700	Vdc	3,10,15	-	-	-	8	1,16
Logic "0" Output Voltage	V <sub>OL</sub>	2	-2.000	-1.675	-1.990	-	-1.650	-1.920	-1.615	Vdc	-	-	-	-	8	1,16
Logic "1" Threshold Voltage	V <sub>OHA</sub>	2	-1.080	-	-0.980	-	-	-0.910	-	Vdc	10,15	-	3	-	8	1,16
Logic "0" Threshold Voltage	V <sub>OLA</sub>	2	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	-	-	3	8	1,16
Switching Times (50 Ω Load)											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t <sub>g+2+</sub> t <sub>3-2-</sub>	2	-	-	1.4	2.3	3.4	-	-	ns	10,13	-	3	2	8	1,16
Rise Time (20 to 80%)	t <sub>r</sub>	↓	-	-	1.5	2.5	4.0	-	-	↓	↓	-	↓	↓	↓	↓
Fall Time (20 to 80%)	t <sub>f</sub>	↓	-	-	1.5	2.5	4.0	-	-	↓	↓	-	↓	↓	↓	↓

