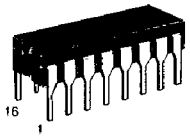
MOTOROLA

MC14528B

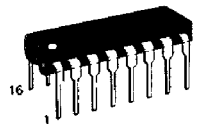
DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X.

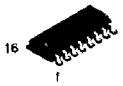
- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

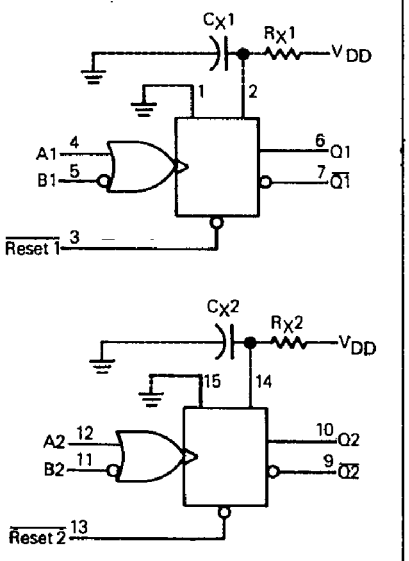
T_A = −55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

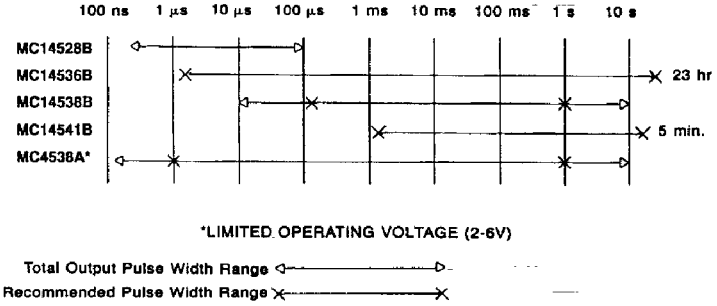
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

ONE-SHOT SELECTION GUIDE



*LIMITED OPERATING VOLTAGE (2-6V)

Total Output Pulse Width Range
Recommended Pulse Width Range

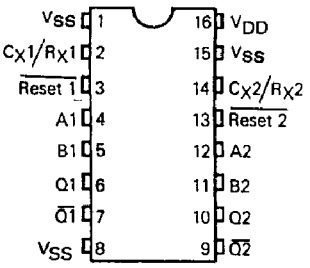
ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−1.2	—	−1.0	−1.7	—	−0.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
**Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula —	I_T	—	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2\times10^{-8} R_XC_X(V_{DD}-2)^2f] \times 10^{-3}$ where: I_T in μA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	—	—	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns	t_{PLH}, t_{PHL}	15	5.0	5.0 10 15	— — —	325 120 90	650 240 180	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns	t_{PLH}, t_{PHL}	1000	10	5.0 10 15	— — —	705 290 210	— — —	ns
Input Pulse Width — A or B	t_{WH}	15	5.0	5.0 10 15	150 75 55	70 30 30	— — —	ns
	t_{WL}	1000	10	5.0 10 15	— — —	70 30 30	— — —	ns
Output Pulse Width — Q or $\overline{Q}$ (For C_X < 0.01 μF use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0 10 15	— — —	550 350 300	— — —	ns
Output Pulse Width — Q or $\overline{Q}$ (For C_X > 0.01 μF use formula: t_W = 0.2 R_X C_X Ln [V_{DD} − V_{SS}])†	t_W	10,000	10	5.0 10 15	15 10 15	30 50 55	45 90 95	μs
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0 10 15	— — —	6.0 8.0 8.0	25 35 35	%
Reset Propagation Delay — $\overline{Reset}$ to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0 10 15	— — —	325 90 60	600 225 170	ns
		1000	10	5.0 10 15	— — —	1000 300 250	— — —	ns
Retrigger Time	t_{rr}	15	5.0	5.0 10 15	0 0 0	— — —	— — —	ns
		1000	10	5.0 10 15	0 0 0	— — —	— — —	ns
External Timing Resistance	R_X	—	—	—	5.0	—	1000	kΩ
External Timing Capacitance	C_X	—	—	—	No Limits*			μF

† R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.
* If C_X > 15 μF, Use Discharge Protection Dipde D_X, per Fig. 9.

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FUNCTION TABLE

Inputs			Outputs	
$\overline{Reset}$	A	B	Q	$\overline{Q}$
H	⌐	H	⌐¬	¬⌐
H	¬	L	⌐¬	¬⌐
H	⌐¬	L	Not Triggered	
H	H	⌐¬	Not Triggered	
H	L, H, ¬	H	Not Triggered	
H	L	L, H, ⌐	Not Triggered	
L	X	X	L	H
¬⌐	X	X	Not Triggered	

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

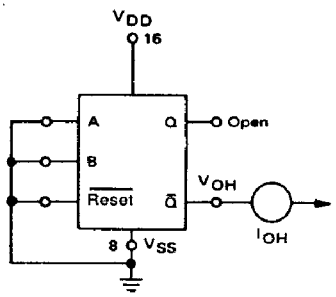


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

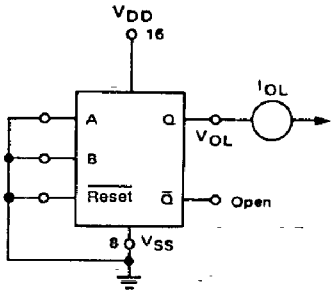
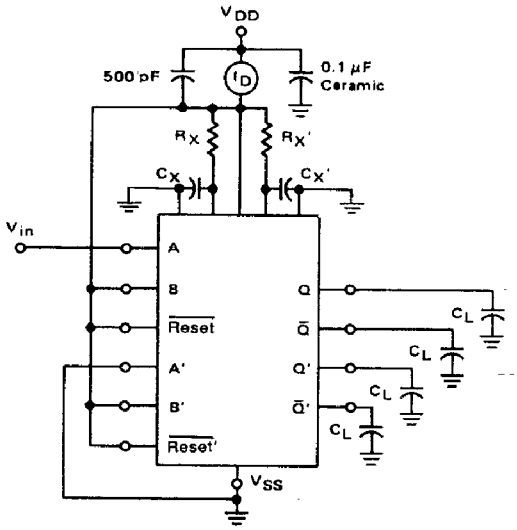
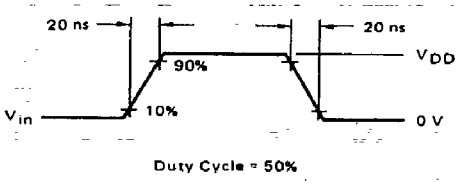


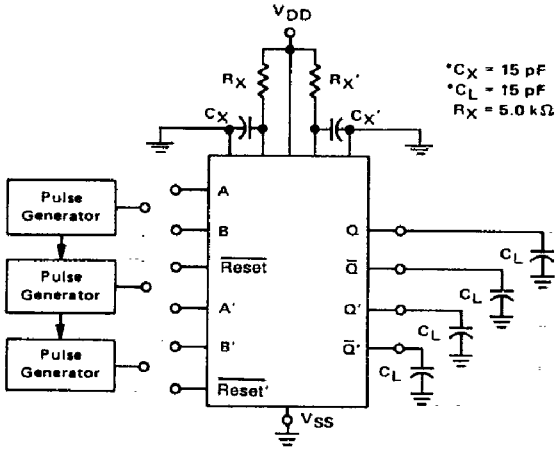
FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS





Duty Cycle = 50%

FIGURE 4 – AC TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	$\overline{\text{Reset}}$	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE. AC test waveforms for PG1, PG2, and PG3 on next page.

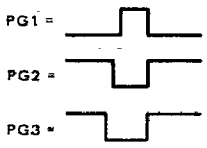


FIGURE 5 — AC TEST WAVEFORMS

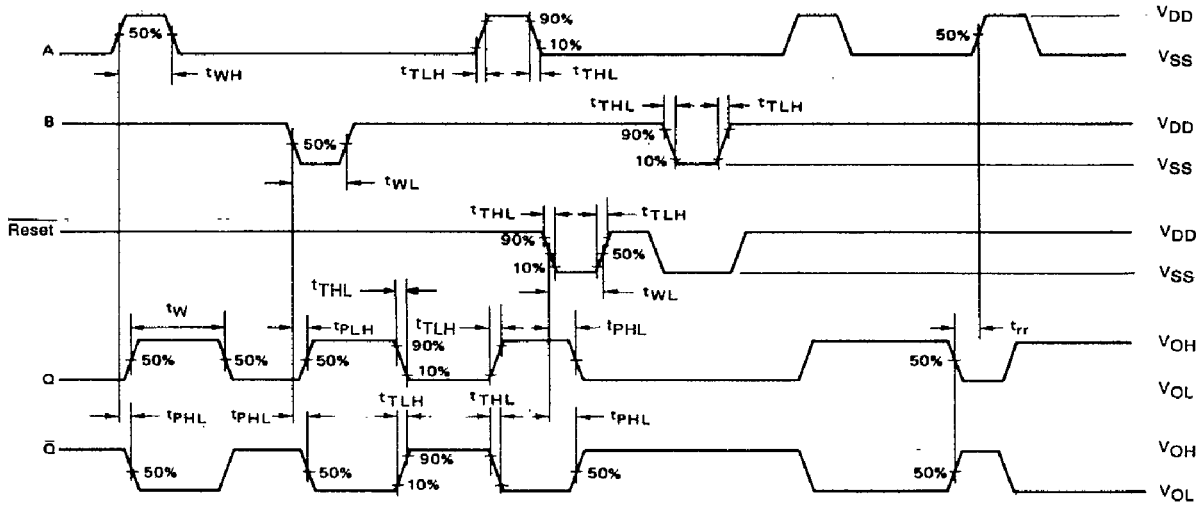
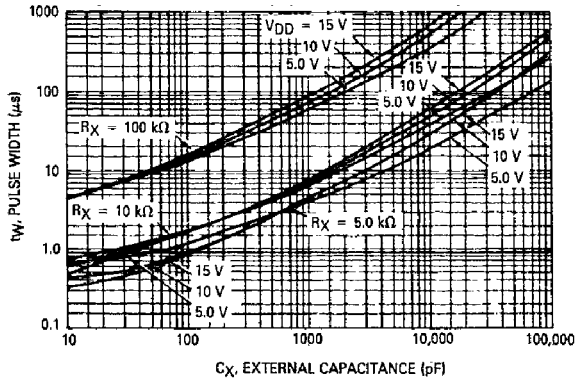


FIGURE 6 — PULSE WIDTH versus C_X



TYPICAL APPLICATIONS

FIGURE 7 — RETRIGGERABLE MONOSTABLES CIRCUITRY

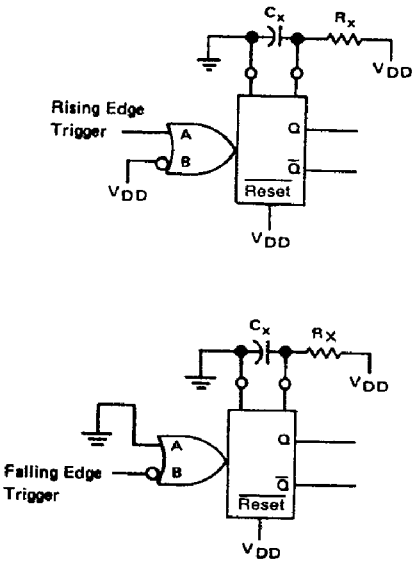


FIGURE 8 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

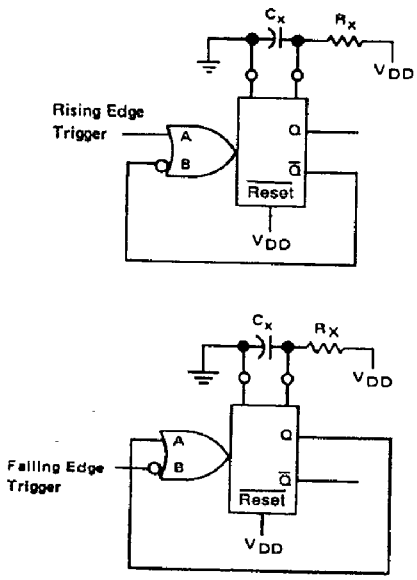


FIGURE 9 — USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE

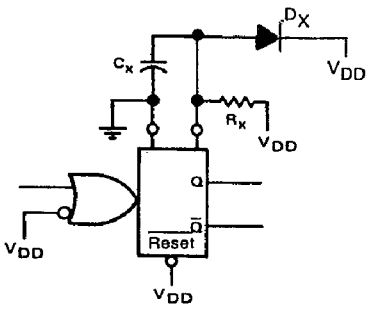


FIGURE 10 — CONNECTION OF UNUSED SECTIONS