

MC830 Series (0 to +75°C)
MC930 Series (-55 to +125°C)

ISSUE A

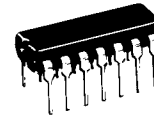
MAXIMUM RATINGS

| Rating | Value | Unit |
|--|----------------------------|-------------|
| Supply Voltage – Operating Continuous Pulsed, < 1 second | 4.5 to 5.5 8.0 12 | Vdc |
| Output Current (Into Outputs with Outputs Low) Buffers, Power Gates – Continuous Pulsed, < 30 ms All other types – Continuous Pulsed, < 30 ms | 100 300 30 90 | mAdc |
| Input Forward Current – Continuous Pulsed, < 30 ms or Negative Voltage at Input – Continuous Pulsed, < 30 ms | -10 -30 -0.5 -1.5 | mAdc Vdc |
| Input Reverse Current or Positive Voltage at Diode Input | 1.0 5.5 | mAdc Vdc |
| Operating Temperature Range MC930 Series MC830 Series | -55 to +125 0 to +75 | °C |
| Storage Temperature Range Metal Can, Ceramic Package Plastic Package | -65 to +150 -55 to +125 | °C |
| Maximum Junction Temperature MC930 Series MC830 Series | 175 150 | °C |

MDTL integrated circuits provide an excellent balance of speed, power dissipation, and noise immunity for general purpose digital applications. The line includes many multifunction types. Additional logic power is provided by the "wired OR" capability of the basic MDTL gate.



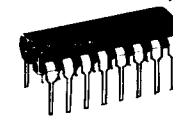
G SUFFIX
METAL PACKAGE
CASE 603-02
TO-100



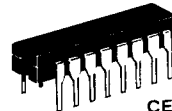
P SUFFIX
PLASTIC PACKAGE
CASE 646



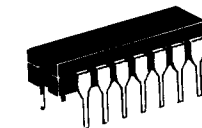
F SUFFIX
CERAMIC PACKAGE
CASE 607



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

| Function | Type ① 0 to +75°C | Case | Type ① -55 to +125°C | Case | Loading Factor Each Output | Propaga- tion Delay ns typ | Power Dissipation mW typ/pkg |
|--|-------------------------|------------------------------------|----------------------------|----------------------------|-------------------------------------|-------------------------------------|---------------------------------------|
| Expandable Dual 4 Input NAND Gate | MC830 | 607,632,646 | MC930 | 607,632 | 8 | 30 | 22 |
| Expandable Dual 3 2 Input NAND Gate | MC830 | 603 | MC930 | 603 | 8 | 30 | 22 |
| Expandable Dual 4 Input Buffer | MC832 | 607,632,646 | MC932 | 607,632 | 25 | 35 | 85 |
| Expandable Dual 3 2 Input Buffer | MC832 | 603 | MC932 | 603 | 25 | 35 | 85 |
| Dual 4 Input Expander | MC833 | 607,632,646 | MC933 | 607,632 | – | – | – |
| Dual 4 3 Input Expander | MC833 | 603 | MC933 | 603 | – | – | – |
| Hex Inverter | MC834 | 607,632,646 | MC934 | 607,632 | 8 | 30 | 66 |
| Hex Inverter (without output resistors) | MC835 | 607,632,646 | MC935 | 607,632 | 8 | 30 | 42 |
| Hex Inverter | MC836 | 607,632,646 | MC936 | 607,632 | 8 | 30 | 66 |
| Hex Inverter | MC837 | 607,632,646 | MC937 | 607,632 | 7 | 25 | 90 |
| Decade Counter | MC838 | 607,632,646 | MC938 | 607,632 | 8 | 30 MHz ③ | 150 |
| Divide-by-Sixteen Counter | MC839 | 607,632,646 | MC939 | 607,632 | 8 | 30 MHz ③ | 150 |
| Hex Inverter (without input diodes) | MC840 | 607,632,646 | MC940 | 607,632 | 8 | 30 | 66 |
| Hex Inverter (without output resistors and input diodes) | MC841 | 607,632,646 | MC941 | 607,632 | 8 | 30 | 42 |
| Expandable Dual 4 Input Power Gate | MC844 | 607,632,646 | MC944 | 607,632 | 27 | 30 | 65 |
| Expandable Dual 3 2 Input Power Gate | MC844 | 603 | MC944 | 603 | 27 | 30 | 65 |
| Clocked Flip-Flop | MC845 | 603,607,632,646 | MC945 | 603,607,632 | 12/10 ② | 40 | 60 |
| Quad 2-Input NAND Gate | MC846 | 607,632,646 | MC946 | 607,632 | 8 | 30 | 44 |
| Quad Inverter | MC846 | 603 | MC946 | 603 | 8 | 30 | 44 |
| Quad 2-Input Gate Expander | MC847 | 607,632,646 | MC947 | 607,632 | – | – | – |
| Clocked Flip-Flop | MC848 | 603,607,632,646 | MC948 | 603,607,632 | 11/9 ② | 40 | 70 |
| Quad 2-Input NAND Gate (2 k pullup resistor) | MC849 | 607,632,646 | MC949 | 607,632 | 7 | 25 | 66 |
| Quad Inverter (2 k pullup resistor) | MC849 | 603 | MC949 | 603 | 7 | 25 | 60 |
| Pulse Triggered Binary Monostable Multivibrator | MC850 MC851 | 603,607,632,646 603,607,632,646 | MC950 MC951 | 603,607,632 603,607,632 | 10/8 ② 10 | 15 40 | 50 30 |
| Dual J-K Flip-Flop (common clock and C _D , separate S _D) | MC852 | 607,632,646 | MC952 | 607,632 | 12/10 ② | 40 | 120 |
| Dual J-K Flip-Flop (separate clock and S _D , no C _D) | MC853 | 607,632,646 | MC953 | 607,632 | 12/10 ② | 40 | 120 |

① F suffix denotes Ceramic Flat Package, G suffix denotes Metal Can, L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package. (i.e., MC830G = Metal Can, MC830F = Flat Package, MC830L = Dual In-Line Ceramic Package, MC830P = Plastic Package)

② Fan-out for MC830 series type / Fan-out for MC930 series type.

③ Counting frequency.

continued

MDTL (continued)

| Function | Type ① 0 to +75°C | Case | Type ① -55 to +125°C | Case | Loading Factor Each Output | Propaga- tion Delay ns typ | Power Dissipation mW typ/pkg |
|--|-------------------------|-------------|----------------------------|---------|-------------------------------------|-------------------------------------|---------------------------------------|
| Dual J-K Flip-Flop (common clock and C _D , separate S _D , 2 k pullup resistor) | MC855 | 607,632,646 | MC955 | 607,632 | 11/9 ② | 40 | 140 |
| Dual J-K Flip-Flop (separate clock and S _D , no C _D , 2 k pullup resistor) | MC856 | 607,632,646 | MC956 | 607,632 | 11/9 ② | 40 | 140 |
| Quad 2-Input Buffer | MC857 | 607,632,646 | MC957 | 607,632 | 25 | 35 | 170 |
| Quad 2-Input NAND Power Gate | MC858 | 607,632,646 | MC958 | 607,632 | 27 | 30 | 130 |
| Expandable Dual 4-Input NAND Gate (2 k pullup resistor) | MC861 | 607,632,646 | MC961 | 607,632 | 7 | 25 | 33 |
| Expandable Dual 3-2 Input NAND Gate (2 k pullup resistor) | MC861 | 603 | MC961 | 603 | 7 | 25 | 33 |
| Triple 3-Input NAND Gate | MC862 | 607,632,646 | MC962 | 607,632 | 8 | 30 | 33 |
| Dual 2-Input NAND Gate plus Inverter | MC862 | 603 | MC962 | 603 | 8 | 30 | 30 |
| Triple 3-Input NAND Gate (2 k pullup resistor) | MC863 | 607,632,646 | MC963 | 607,632 | 7 | 25 | 50 |
| Dual 2-Input NAND Gate plus Inverter (2 k pullup resistor) | MC863 | 603 | MC963 | 603 | 7 | 25 | 45 |
| Dual 5 Input NAND Gate (6K pullup resistor) | MC1800 | 607,632,646 | MC1900 | 607,632 | 8 | 30 | 22 |
| Dual 5-Input NAND Gate (2k pullup resistor) | MC1801 | 607,632,646 | MC1901 | 607,632 | 7 | 25 | 33 |
| Expandable 8-Input NAND Gate | MC1802 | 607,632,646 | MC1902 | 607,632 | 8 | 30 | 11 |
| Expandable 8-Input NAND Gate (2 k pullup resistor) | MC1803 | 607,632,646 | MC1903 | 607,632 | 7 | 25 | 16.5 |
| 10-Input NAND Gate | MC1804 | 607,632,646 | MC1904 | 607,632 | 8 | 30 | 11 |
| 10-Input NAND Gate (2k pullup resistor) | MC1805 | 607,632,646 | MC1905 | 607,632 | 7 | 25 | 16.5 |
| Quad 2-Input AND Gate | MC1806 | 607,632,646 | MC1906 | 607,632 | 8 | 35 | 72 |
| Quad 2-Input AND Gate (2k pullup resistor) | MC1807 | 607,632,646 | MC1907 | 607,632 | 7 | 30 | 85 |
| Quad 2-Input OR Gate | MC1808 | 607,632,646 | MC1908 | 607,632 | 8 | 35 | 97 |
| Quad 2-Input OR Gate (2k pullup resistor) | MC1809 | 607,632,646 | MC1909 | 607,632 | 7 | 30 | 115 |
| Quad 2-Input NOR Gate | MC1810 | 607,632,646 | MC1910 | 607,632 | 8 | 30 | 60 |
| Quad 2-Input NOR Gate (2k pullup resistor) | MC1811 | 607,632,646 | MC1911 | 607,632 | 7 | 25 | 72 |
| Quad 2-Input Exclusive OR Gate | MC1812 | 607,632,646 | MC1912 | 607,632 | 8 | 40 | 120 |
| Quad Latch | MC1813 | 620,648 | — | — | 7 | 35 | 220 |
| Quad Latch | MC1814 | 607,632,646 | MC1914 | 607,632 | 7 | 35 | 220 |
| Parallel Gated Clocked Flip-Flop | MC1815 | 607,632,646 | MC1915 | 607,632 | 12/10 ② | 40 | 65 |
| Parallel Gated Clocked Flip-Flop | MC1816 | 607,632,646 | MC1916 | 607,632 | 11/9 ② | 40 | 75 |
| Quad 2-Input NAND Gate (without output resistor) | MC1818 | 607,632,646 | MC1918 | 607,632 | 8 | 30 | 32 |
| High Voltage Hex Inverter | MC1820 | 632,646 | — | — | 7 | 40 | 42 |

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② Fan-out for MC830 series type/Fan-out for MC930 series type.

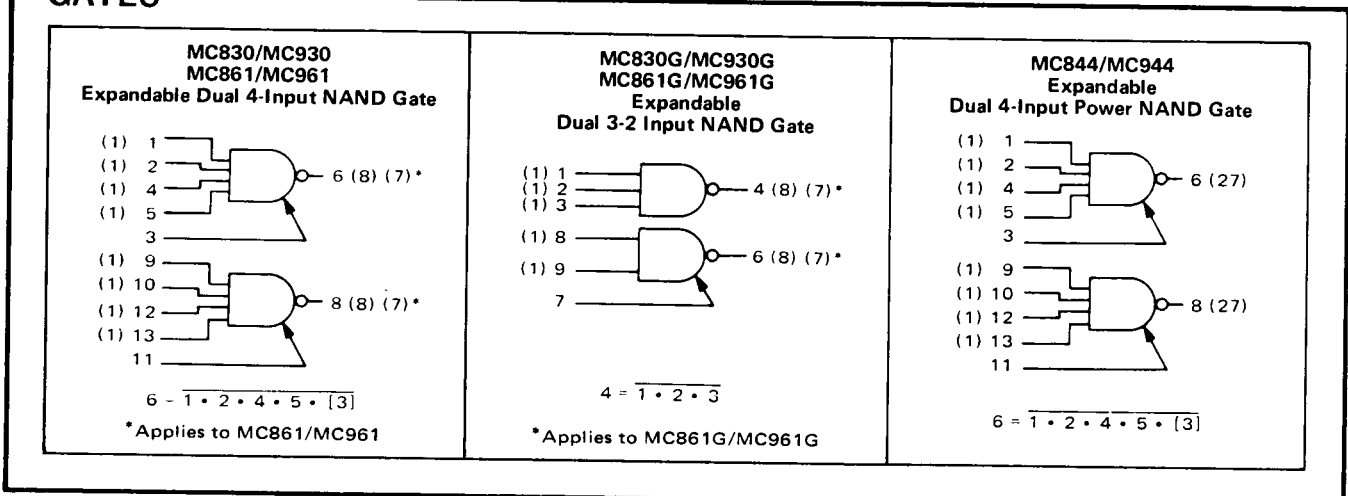
③ Counting frequency.

*Unless otherwise noted

| Case | Gnd* Pin No. | VCC* Pin No. |
|------|-----------------|-----------------|
| 603 | 5 | 10 |
| 646 | 7 | 14 |
| 607 | 7 | 14 |
| 648 | 8 | 16 |
| 620 | 8 | 16 |
| 632 | 7 | 14 |

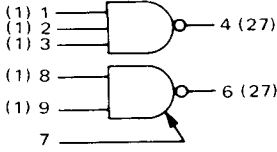
GATES

Numbers at ends of terminals represent pin numbers. Numbers in parenthesis indicate loading.



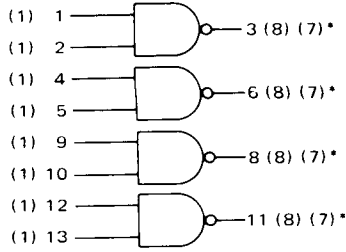
GATES (continued)

MC844G/MC944G
Expandable
Dual 3-2 Input NAND Power Gate



$$4 = \overline{1 \cdot 2 \cdot 3}$$

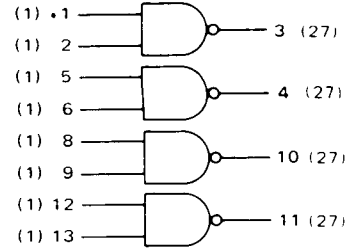
MC846/MC946
MC849/MC949
Quad 2-Input NAND Gate



$$3 = \overline{1 \cdot 2}$$

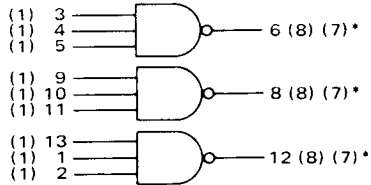
*Applies to MC849/MC949

MC858/MC958
Quad 2-Input NAND Power Gate



$$3 = \overline{1 \cdot 2}$$

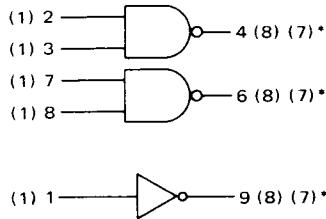
MC862/MC962
MC863/MC963
Triple 3-Input NAND Gate



$$6 = \overline{3 \cdot 4 \cdot 5}$$

*Applies to MC863/MC963

MC862G/MC962G
MC863G/MC963G
Dual 2-Input NAND Gate
Plus Inverter



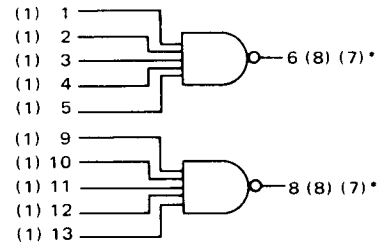
$$4 = \overline{2 \cdot 3}$$

$$6 = \overline{7 \cdot 8}$$

$$9 = \overline{1}$$

*Applies to MC863G/MC963G

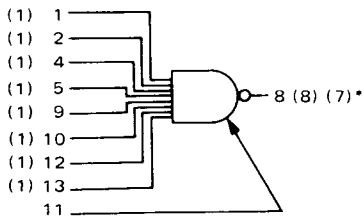
MC1800/MC1900
MC1801/MC1901
Dual 5-Input NAND Gate



$$6 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5}$$

*Applies to MC1801/MC1901

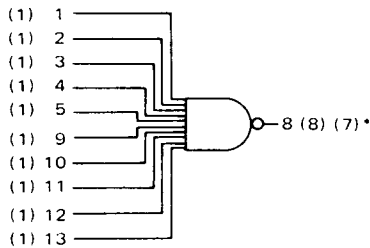
MC1802/MC1902
MC1803/MC1903
Expandable 8-Input NAND Gate



$$8 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot 9 \cdot 10 \cdot 12 \cdot 13 \cdot [11]}$$

*Applies to MC1803/MC1903

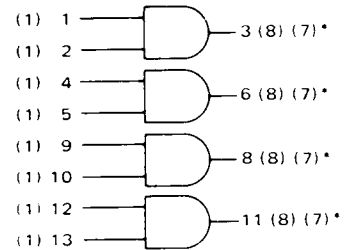
MC1804/MC1904
MC1805/MC1905
10-Input NAND Gate



$$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 9 \cdot 10 \cdot 11 \cdot 12 \cdot 13}$$

*Applies to MC1805/MC1905

MC1806/MC1906
MC1807/MC1907
Quad 2-Input AND Gate



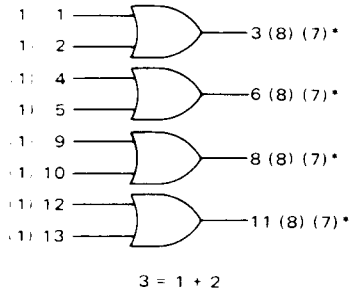
$$3 = 1 \cdot 2$$

*Applies to MC1807/MC1907

(continued)

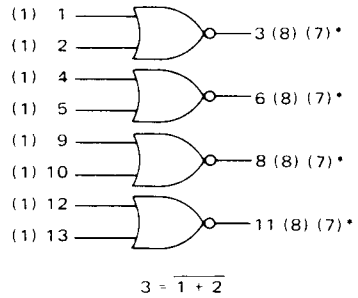
GATES (continued)

**MC1808/MC1908
MC1809/MC1909**
Quad 2-Input OR Gate



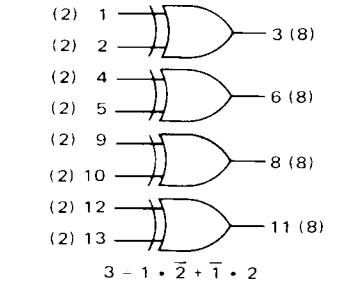
*Applies to MC1809/MC1909

**MC1810/MC1910
MC1811/MC1911**
Quad 2-Input NOR Gate

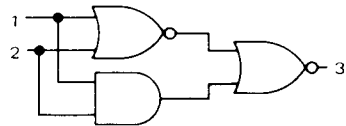


*Applies to MC1811/MC1911

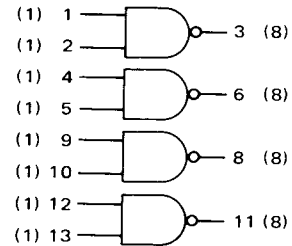
MC1812/MC1912
Quad 2-Input Exclusive OR Gate



FUNCTIONAL LOGIC DIAGRAM



MC1818/MC1918
Quad 2-Input NAND Gate
(Without Output Resistors)

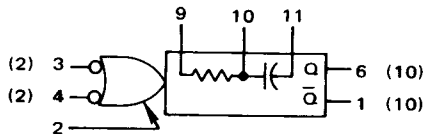


$3 = \overline{1 \cdot 2}$

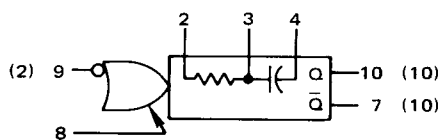
MULTIVIBRATOR

MC851/MC951
Monostable Multivibrator

F, L, P, PACKAGES



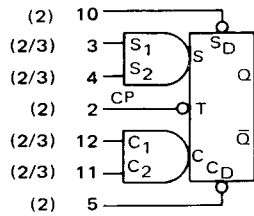
G PACKAGE
VCC = Pin 6, Gnd = Pin 1



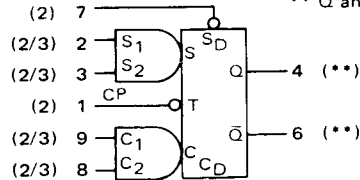
FLIP-FLOPS

MC845/MC945 MC848/MC948 Clocked Flip-Flop

F, L, & P PACKAGES



G PACKAGES



** Q and \bar{Q} loading factor: 12 for MC845 types
10 for MC945 types
11 for MC848 types
9 for MC948 types

SYNCHRONOUS TRUTH TABLE

| t_n | | | | t_{n+1} |
|-------|-------|-------|-------|-----------|
| S_1 | S_2 | C_1 | C_2 | Q |
| 0 | X | 0 | X | Q_n |
| 0 | X | X | 0 | Q_n |
| X | 0 | 0 | X | Q_n |
| X | 0 | X | 0 | Q_n |
| 0 | X | 1 | 1 | 0 |
| X | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | X | 1 |
| 1 | 1 | X | 0 | 1 |
| 1 | 1 | 1 | 1 | U |

0 — Low State (more negative)
1 — High State (more positive)
X — State of the input does not affect the state of the circuit.
U — Indeterminate State

J-K TRUTH TABLE
(Connect S_2 to \bar{Q} , C_2 to Q)

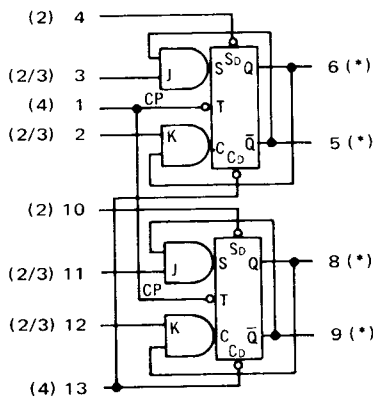
| t_n | | t_{n+1} |
|-------|-------|-------------|
| S_1 | C_1 | Q |
| 0 | 0 | Q_n |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | \bar{Q}_n |

ASYNCHRONOUS TRUTH TABLE

| S_D | C_D | Q | \bar{Q} |
|-------|-------|-----|-----------|
| 1 | 1 | NC | NC |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |

Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs: they are independent of all other inputs.

MC852/MC952 MC855/MC955 Dual J-K Flip-Flop



*Q and \bar{Q} loading factor:
12 — MC852
10 — MC952
11 — MC855
9 — MC955

ASYNCHRONOUS TRUTH TABLE
MC952/MC852 and MC955/MC855

| S_D | C_D | Q | \bar{Q} |
|-------|-------|-----|-----------|
| 1 | 1 | NC | NC |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |

ASYNCHRONOUS TRUTH TABLE
MC953/MC853 and MC956/MC856

| S_D | Q | \bar{Q} |
|-------|-----|-----------|
| 1 | NC | NC |
| 0 | 1 | 0 |

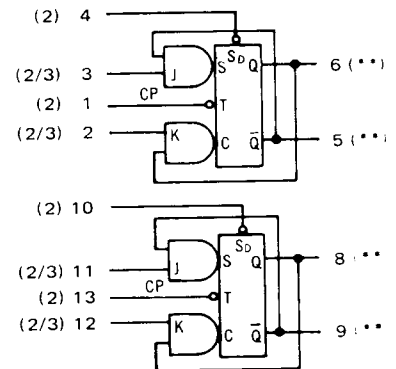
Asynchronous inputs, direct set (S_D) and direct clear (C_D), override the synchronous inputs: they are independent of all other inputs.

J-K TRUTH TABLE
All Types

| t_n | | t_{n+1} |
|-------|---|-------------|
| J | K | Q |
| 0 | 0 | Q_n |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | \bar{Q}_n |

J & K inputs must not change while clock is high.

MC853/MC953 MC856/MC956 Dual J-K Flip-Flop



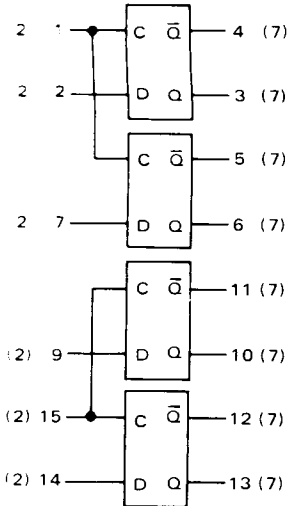
**Q and \bar{Q} loading factor
12 — MC853
10 — MC953
11 — MC856
9 — MC956

(cont. next)

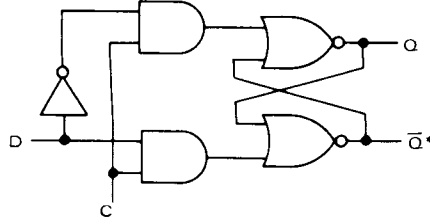
MDTL LOGIC DIAGRAMS

FLIP-FLOPS (continued)

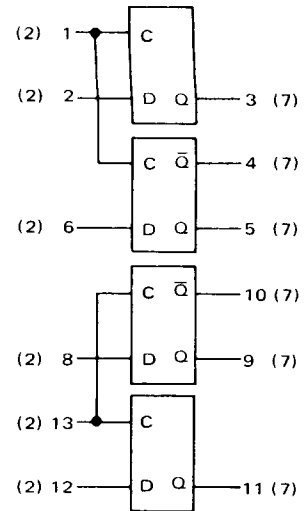
**MC1813
Quad Latch**



FUNCTIONAL LOGIC DIAGRAM



**MC1814/MC1914
Quad Latch**



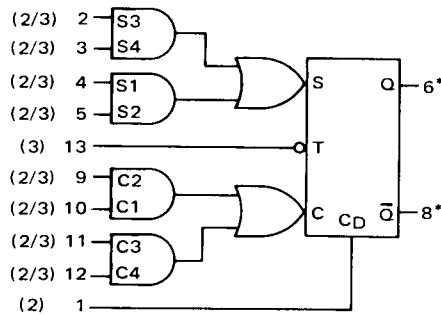
Information present at the Data Input D is transferred to the Q output when the clock is high, and the Q output will follow the state of the Data input as long as the clock remains high. Information present at the Q output will be retained as the clock goes low until such time as the clock is permitted to go high.

TRUTH TABLE

| D | t_n | |
|---|-------|-------------|
| | Q | \bar{Q}^* |
| 1 | 1 | 0 |
| 0 | 0 | 1 |

* As applicable (see loading diagram)

**MC1815/MC1915
MC1816/MC1916
Parallel Gated Clocked Flip-Flop**



* Q and \bar{Q} loading factor
 12 - MC1815
 10 - MC1915
 11 - MC1816
 9 - MC1916

SYNCHRONOUS TRUTH TABLE

| t_n | | | | | | | | | t_{n+1} |
|-------|----|----|----|----|----|----|----|----|-----------|
| C_D | C3 | C4 | C1 | C2 | S3 | S4 | S1 | S2 | Q |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Q_n |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | U |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | U |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | U |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | U |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | U |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | U |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | U |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | U |

0 - Low State (more negative) NC - No Change
 1 - High State (more positive) U - Indeterminate State

J-K TRUTH TABLE
 (Connect S2 and S4 to \bar{Q} , C2 and C4 to Q)

| t_n | | | | t_{n+1} |
|-------|----|----|----|-------------|
| S1 | S3 | C1 | C3 | Q |
| 0 | 0 | 0 | 0 | Q_n |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | \bar{Q}_n |

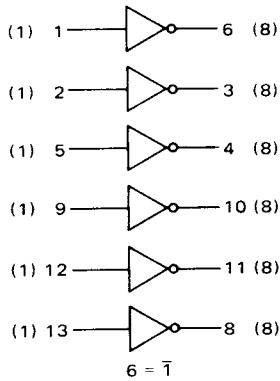
ASYNCHRONOUS TRUTH TABLE

| C_D | Q | \bar{Q} |
|-------|----|-----------|
| 1 | NC | NC |
| 0 | 0 | 1 |

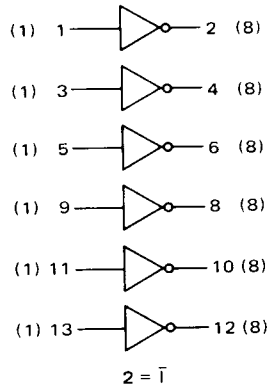
Asynchronous input, direct clear (C_D), overrides the synchronous inputs. Clocked operation will occur only when C_D is in the High State.

INVERTERS

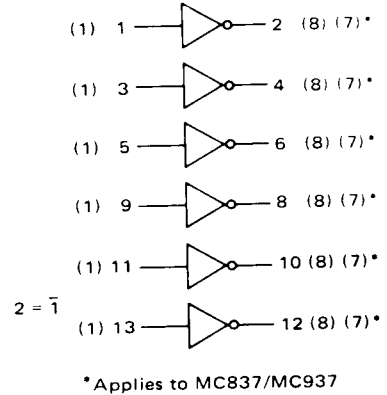
**MC834/MC934
Hex Inverter**



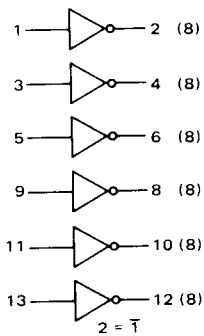
**MC835/MC935
Hex Inverter
(Without Output Resistors)**



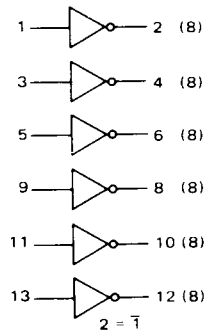
**MC836/MC936
MC837/MC937
Hex Inverter**



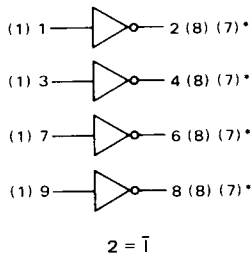
**MC840/MC940
Hex Inverter
(Without Input Diodes)**



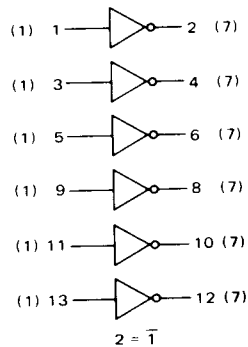
**MC841/MC941
Hex Inverter
(Without Output Resistors
and Input Diodes)**



**MC846G/MC946G
MC849G/MC949G
Quad Inverter**

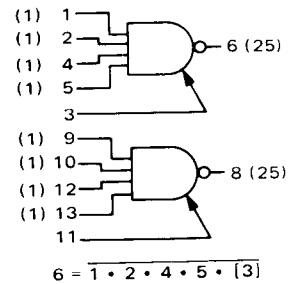


**MC1820
High Voltage
Hex Inverter
(Without Output Resistors)**

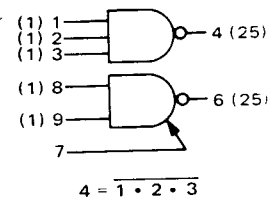


BUFFERS

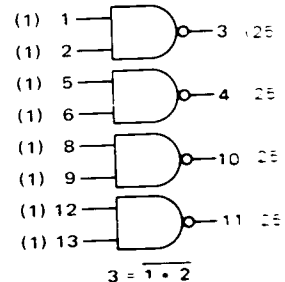
**MC832/MC932
Expandable Dual 4-Input Buffer**



**MC832G/MC932G
Expandable Dual 3-2 Input Buffer**

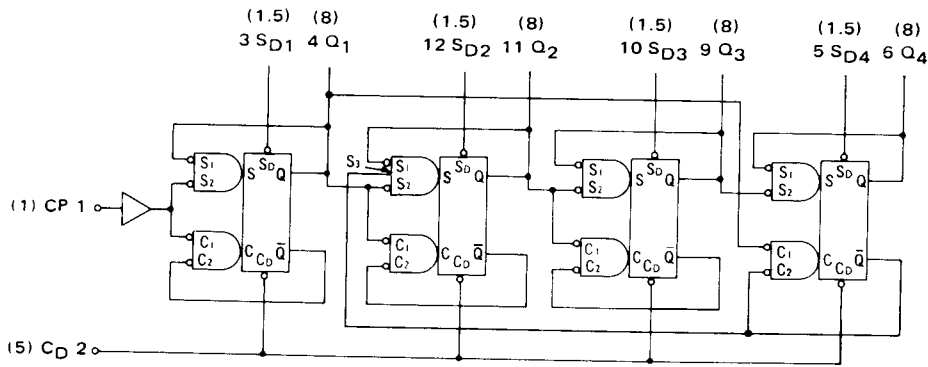


**MC857/MC957
Quad 2-Input Buffers**



COUNTERS

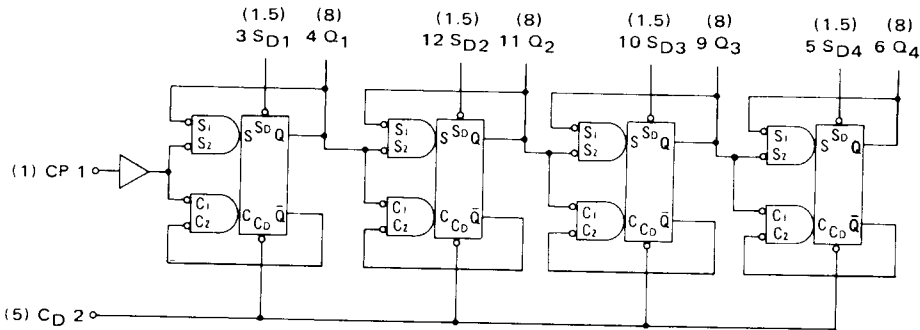
MC838/MC938
Decade Counter



DECODING LOGIC

| 0 | \bar{Q}_1 | \bar{Q}_2 | \bar{Q}_3 | \bar{Q}_4 |
|---|-------------|-------------|-------------|-------------|
| 1 | Q_1 | \bar{Q}_2 | \bar{Q}_3 | \bar{Q}_4 |
| 2 | \bar{Q}_1 | Q_2 | \bar{Q}_3 | \bar{Q}_4 |
| 3 | Q_1 | Q_2 | \bar{Q}_3 | \bar{Q}_4 |
| 4 | \bar{Q}_1 | \bar{Q}_2 | Q_3 | \bar{Q}_4 |
| 5 | Q_1 | \bar{Q}_2 | Q_3 | \bar{Q}_4 |
| 6 | \bar{Q}_1 | Q_2 | Q_3 | \bar{Q}_4 |
| 7 | Q_1 | Q_2 | Q_3 | \bar{Q}_4 |
| 8 | \bar{Q}_1 | | | Q_4 |
| 9 | Q_1 | | | Q_4 |

MC839/MC939
Divide-by-Sixteen Counter

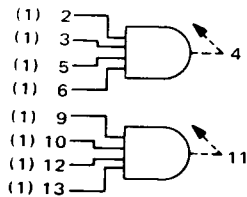


DECODING LOGIC

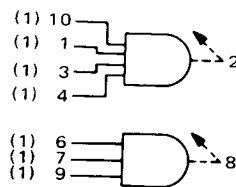
| 0 | \bar{Q}_1 | \bar{Q}_2 | \bar{Q}_3 | \bar{Q}_4 |
|----|-------------|-------------|-------------|-------------|
| 1 | Q_1 | \bar{Q}_2 | \bar{Q}_3 | \bar{Q}_4 |
| 2 | \bar{Q}_1 | Q_2 | \bar{Q}_3 | \bar{Q}_4 |
| 3 | Q_1 | Q_2 | \bar{Q}_3 | \bar{Q}_4 |
| 4 | \bar{Q}_1 | \bar{Q}_2 | Q_3 | \bar{Q}_4 |
| 5 | Q_1 | \bar{Q}_2 | Q_3 | \bar{Q}_4 |
| 6 | \bar{Q}_1 | Q_2 | Q_3 | \bar{Q}_4 |
| 7 | Q_1 | Q_2 | Q_3 | \bar{Q}_4 |
| 8 | \bar{Q}_1 | \bar{Q}_2 | \bar{Q}_3 | Q_4 |
| 9 | Q_1 | \bar{Q}_2 | \bar{Q}_3 | Q_4 |
| 10 | \bar{Q}_1 | Q_2 | \bar{Q}_3 | Q_4 |
| 11 | Q_1 | Q_2 | \bar{Q}_3 | Q_4 |
| 12 | \bar{Q}_1 | \bar{Q}_2 | Q_3 | Q_4 |
| 13 | Q_1 | \bar{Q}_2 | Q_3 | Q_4 |
| 14 | \bar{Q}_1 | Q_2 | Q_3 | Q_4 |
| 15 | Q_1 | Q_2 | Q_3 | Q_4 |

EXPANDERS

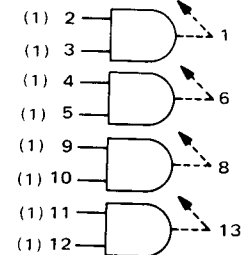
MC833/MC933
Dual 4-Input Expander



MC833G/MC933G
Dual 4-3 Input Expander

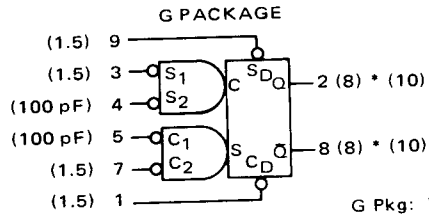
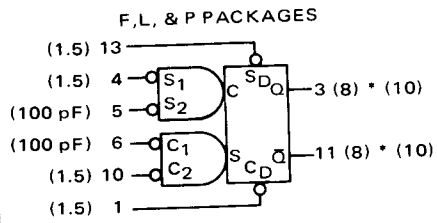


MC847/MC947
Quad 2-Input Gate Expander



PULSE TRIGGERED BINARY

MC850/MC950 Pulse Triggered Binary



G Pkg: V_{CC} = Pin 10, Gnd = Pin 6

* Applies to MC950

SYNCHRONOUS TRUTH TABLE

| t_n | | | | t_{n+1} |
|-------|-------|-------|-------|-----------|
| S_1 | S_2 | C_1 | C_2 | Q |
| 0 | 0 | 0 | 0 | U |
| 1 | X | 1 | X | Q_n |
| X | 1 | X | 1 | Q_n |
| 0 | 1 | 1 | 0 | Q_n |
| 0 | 0 | X | 1 | 1 |
| 0 | 0 | 1 | X | 1 |
| 1 | X | 0 | 0 | 0 |
| X | 1 | 0 | 0 | 0 |

ASYNCHRONOUS TRUTH TABLE

| S_D | C_D | Q | \bar{Q} |
|-------|-------|----|-----------|
| 1 | 1 | NC | NC |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |

0 = low state (more negative)
 1 = high state (more positive)
 X = don't care
 U = indeterminate state
 NC = no change

SINGLE TRIGGER TRUTH TABLE (Pins S_2 and C_1 tied together)

| t_n | | t_{n+1} |
|-------|-------|-----------|
| S_1 | C_2 | Q |
| 0 | 0 | U |
| 1 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 1 | Q_n |