MOTOROLA
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TECHNICAL DATA

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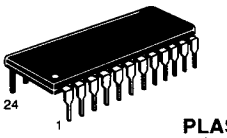
MCCS146818B

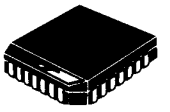
Product Preview

Real Time Clock plus SRAM

CMOS



PLASTIC DIP
CASE 709



PLCC
CASE 776

Ordering Information

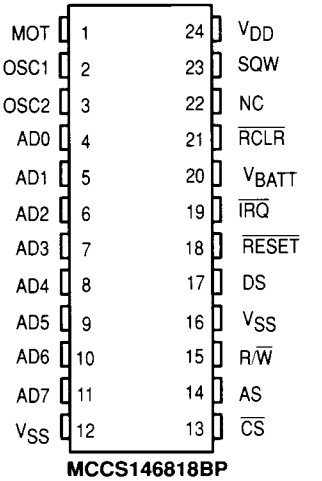
MCCS146818BP	PDIP
MCCS146818FN	PLCC

The MCCS146818B Real Time Clock plus RAM is a direct replacement for the DS1285. This device includes the unique MOTEL concept for use with both Motorola and Intel microprocessor timing cycles. This device combines four important features: 1) a complete time-of-day clock with alarm and a one hundred year calendar, 2) a programmable interrupt for alarm and timing functions, 3) a square wave generation circuit, and 4) 114 bytes of ultra low power static RAM. The MCCS146818B interfaces with 1-MHz processor buses while consuming very little power.

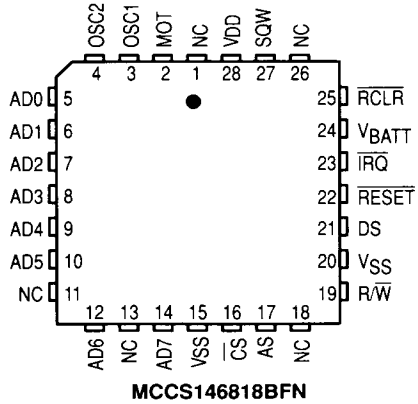
The real time clock plus RAM has two distinct uses. First, it is a CMOS part which includes all the common battery backed-up functions such as RAM, time, and calendar. Secondly, the MCCS146818B may be used with a CMOS microprocessor to relieve the processor of the time keeping workload, and to extend the available RAM of the MPU.

- Pin compatible with DS1285
- Counts seconds, minutes, hours, days, day of the week, date of month and year with leap year compensation
- Binary or BCD data representation
- 12/24 hour mode
- Daylight savings time option
- Multiplexed bus for pin efficiency
- Interfaced with software as 128 bytes of RAM
  - 14 bytes of clock and control registers
  - 114 bytes of general-purpose RAM
- Programmable square wave signal
- Three interrupts are separately software maskable and testable
  - Time-of-day alarm
  - Timed interrupt, once per second to once per day
  - End of clock update cycle
- Operating temperature range 0 to 70°C
- Digital inputs/outputs are TTL, NMOS, and CMOS compatible
- Application information included in Section 7.0

PIN ASSIGNMENTS



MCCS146818BP



MCCS146818BFN

NC = No Connect

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MOTOROLA

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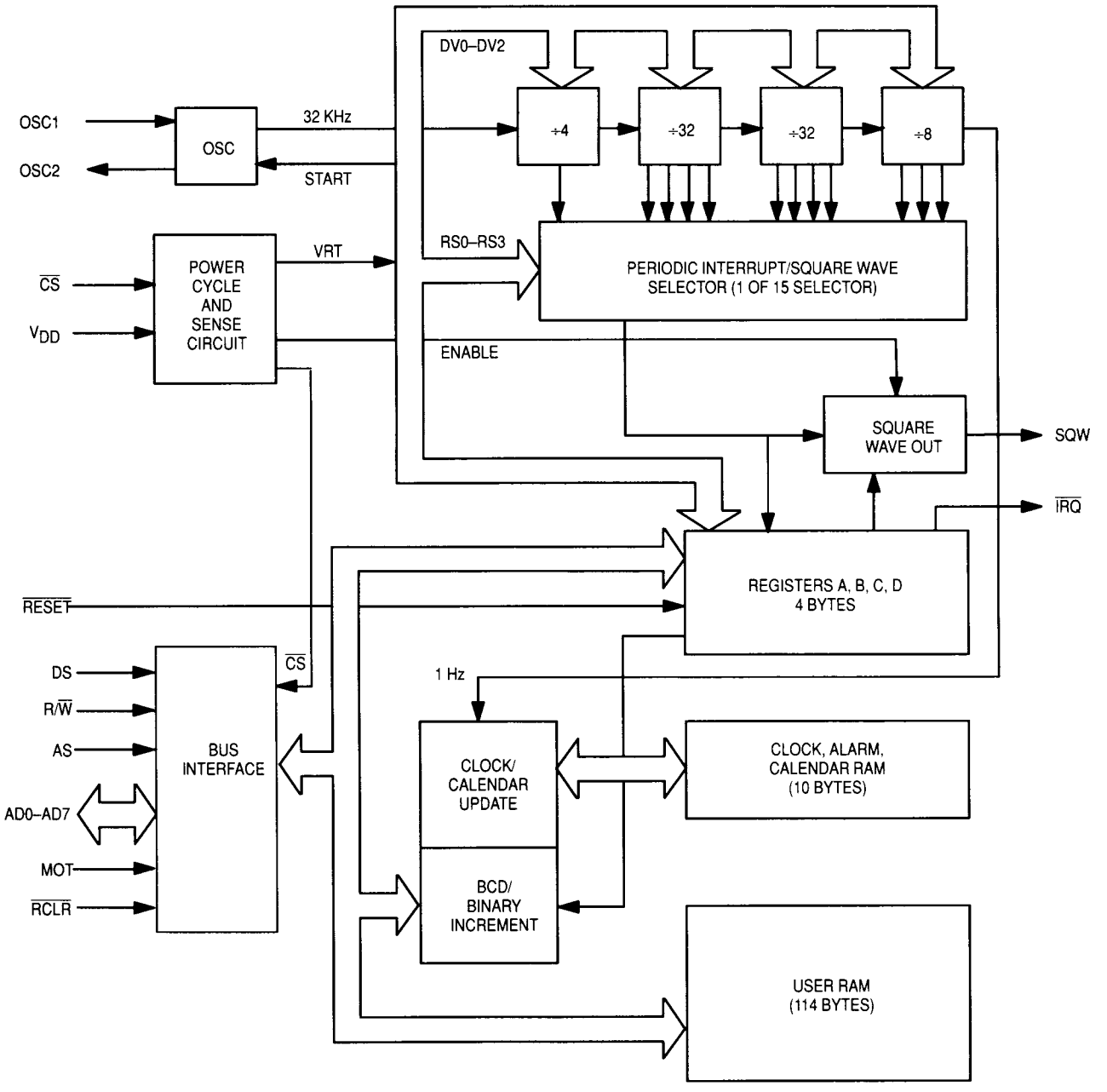
BLOCK DIAGRAM



1.0 MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	− 0.5 to 5.5	V
All Input Voltages Except OSC1	V_{in}	− 0.5 to V_{DD} + 0.5	V
Current Drain per Pin Excluding V_{DD} and V_{SS}	I_{in}	± 15	mA
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

1.1 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Device Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	120	°C/W

2.0 DC ELECTRICAL CHARACTERISTICS (V_{BATT} = 3.0 V, V_{DD} = 0 V, T_A = 25°C, Stand-by Mode)

Characteristics	Symbol	Guaranteed Limits		Unit
		Min	Max	
Frequency of Operation	f_{osc}	32.76750	32.76850	kHz
Battery Supply Current	I_{BATT}	500	800	nA

2.1 DC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = 0 to 70°C, Voltages Referenced to V_{SS})

Characteristics	Test Conditions	Symbol	Guaranteed Limits		Unit
			Min	Max	
Frequency of Operation		f_{osc}	32.768	32.768	kHz
Output Voltage	I_{LOAD} < 10 µA	V_{OL} V_{OH}	— V_{DD} − 0.1	0.1 —	V
Output High Voltage (see Note 1)	I_{LOAD} = 1.0 mA	V_{OH}	2.4	—	V
Output Low Voltage	I_{LOAD} = 4.0 mA, All Outputs	V_{OL}	—	0.4	V
Input High Voltage (AD0–AD7, DS, MOT, AS, R/$\overline{W}$, $\overline{CS}$, $\overline{RESET}$)		V_{IH}	2.2	V_{DD} + 0.3	V
Input Low Voltage (AD0–AD7, DS, R/$\overline{W}$, $\overline{CS}$, MOT, $\overline{RESET}$, AS)		V_{IL}	− 0.3	+ 0.8	V
Input Current (OSC1)		I_{in}	—	TBD	µA
All Other Inputs (Input Pull-Down) (see Note 2)		I_{in}	—	1.0	µA
Three-State Leakage	V_{out} = V_{SS} or V_{DD}	I_{OZ}	—	+ 10	µA
Power Supply Current	Bus Idle	I_{DD}	—	TBD	µA
	XTAL on Pins 2 and 3 Squarewave Out Disabled	I_{DD}	—	TBD	µA

TBD — To be determined

NOTES:

1. All outputs except IRQ. IRQ has open drain.
2. MOTEL pin #1 has a 20 kΩ pulldown resistor. $\overline{RCLR}$ pin #22 has a 20 kΩ pullup resistor.

3.0 BUS TIMING (V_{DD} = 4.5 to 5.5 V, C_L = 130 pF)

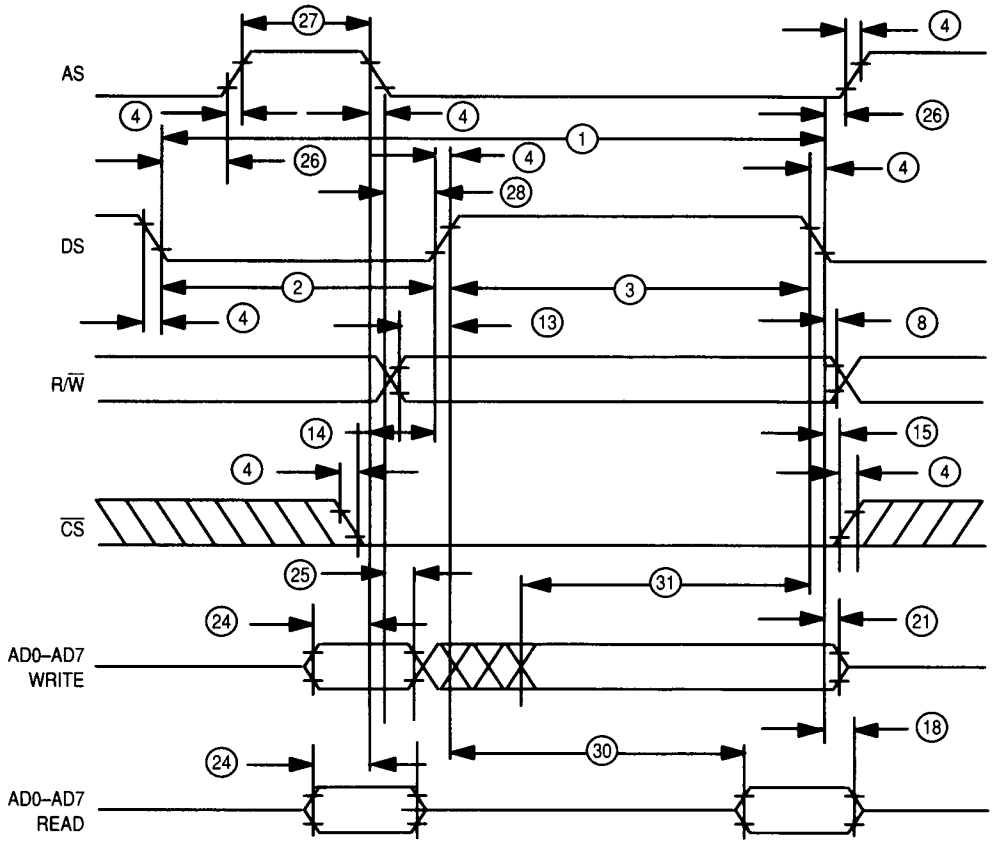
Num.	Characteristics	Symbol	Guaranteed Limits		Unit
			Min	Max	
1	Cycle Time	t_{cyc}	953	—	ns
2	Pulse Width, DS Low or R/$\overline{W}$ High	t_{WEL}	300	—	ns
3	Pulse Width, DS High or R/$\overline{W}$ Low	t_{WEH}	325	—	ns
4	Input Rise and Fall Time	t_r, t_f	—	30	ns
8	R/$\overline{W}$ Hold Time from DS Going Low	t_{RWH}	10	—	ns
13	R/$\overline{W}$ Setup Time Before DS	t_{RWS}	80	—	ns
14	Chip Select Setup Time Before DS, $\overline{WR}$, $\overline{RD}$	t_{CS}	25	—	ns
15	Chip Select Hold Time from DS	t_{CH}	0	—	ns
18	Read Data Hold Time	t_{DHR}	10	TBD	ns
21	Write Data Hold Time	t_{DHW}	0	—	ns
24	Multiplexed Address Valid Time to AS/ALE Fall	t_{ASL}	TBD	—	ns
25	Multiplexed Address Hold Time	t_{AHL}	20	—	ns
26	Delay Time DS to AS/ALE Rise	t_{ASD}	50	—	ns
27	Pulse Width, AS/ALE High	t_{PASH}	60	—	ns
28	Delay Time, AS/ALE to DS Change	t_{ASED}	60	—	ns
30	Peripheral Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20	—	ns
31	Peripheral Data Setup Time	t_{DSW}	200	—	ns

3.1 SWITCHING CHARACTERISTICS (V_{DD} = 4.5 to 5.5 V, T_A = 0 to 70°C)

Num.	Description	Symbol	Guaranteed Limits		Unit
			Min	Max	
32	Oscillator Startup Time	t_{RC}	—	200	ms
33	$\overline{RESET}$ Pulse Width	t_{RWL}	TBD	—	µs
34	$\overline{RESET}$ Delay Time	t_{RLH}	TBD	—	µs
35	$\overline{IRQ}$ Release from DS	t_{IRDS}	—	TBD	µs
36	$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}	—	TBD	µs

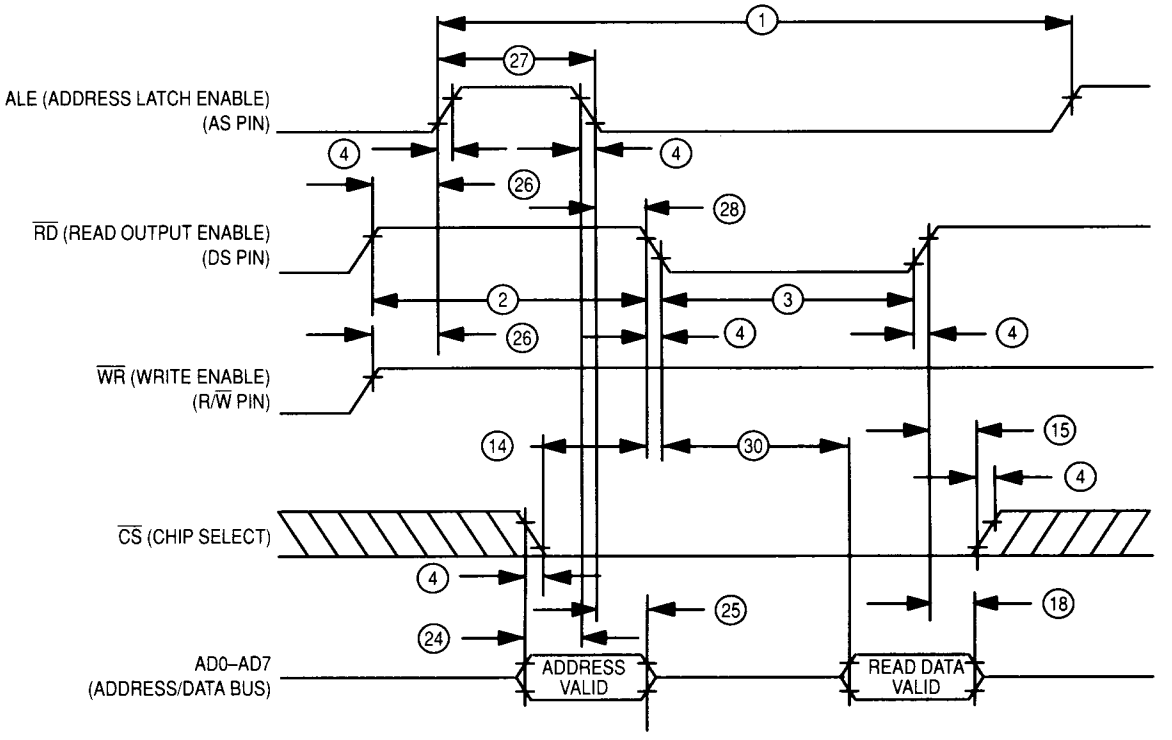
TBD — To be determined

READ/WRITE TIMING FOR MOTOROLA BUS CYCLE



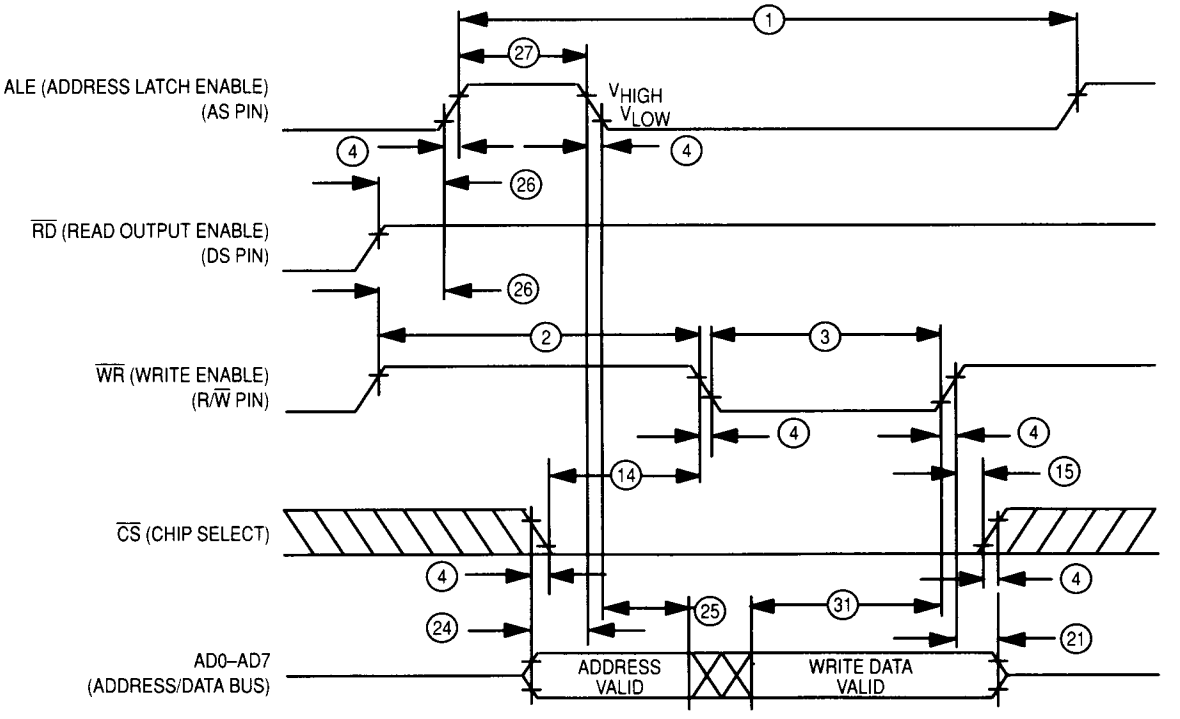
NOTE: $V_{HIGH} = V_{DD} - 2.0$, $V_{LOW} = 0.8$ V for $V_{DD} = 5.0$ V ± 10% for outputs only.
$V_{HIGH} = 2.0$ V, $V_{LOW} = 0.5$ V for $V_{DD} = 3.0$ V for outputs only.
MOT = V_{DD} = + 5 V

INTEL BUS READ CYCLE



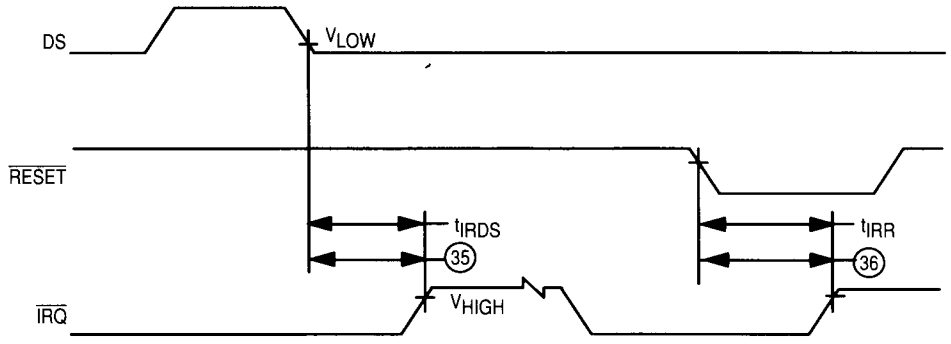
NOTE: MOT = V_{SS} = 0 V

INTEL BUS WRITE CYCLE



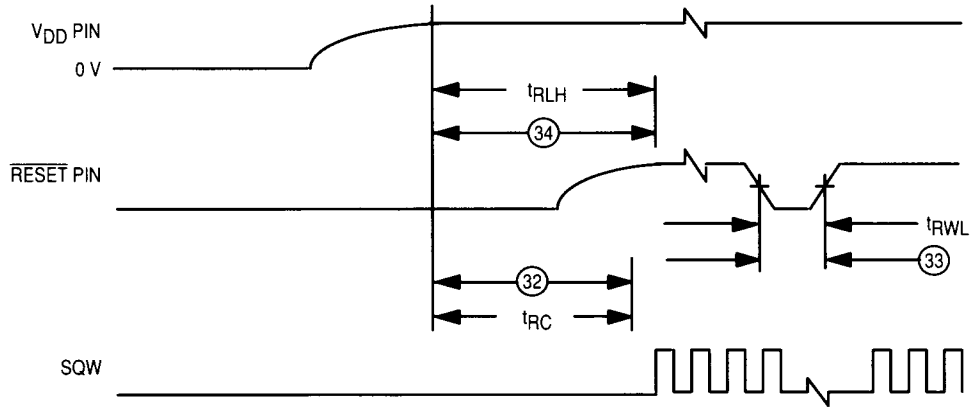
NOTE: $V_{HIGH} = V_{DD} - 2.0$, V_{LOW} = 0.8 V for V_{DD} = 5.0 V ± 10% for outputs only.
V_{HIGH} = 2.0 V, V_{LOW} = 0.5 V for V_{DD} = 3.0 V for outputs only.
MOT = V_{SS} = + 5 V

$\overline{IRQ}$ RELEASE DELAY



NOTE: $V_{HIGH} = V_{DD} - 2.0$ V, $V_{LOW} = 0.8$ V for $V_{DD} = 5.0$ V ± 10%

POWER-UP TIMING



4.0 SIGNAL DESCRIPTIONS

The block diagram shows the pin connections with the major internal functions of the MCCS146818B Real-Time Clock plus RAM. The following paragraphs describe the functions of each pin.

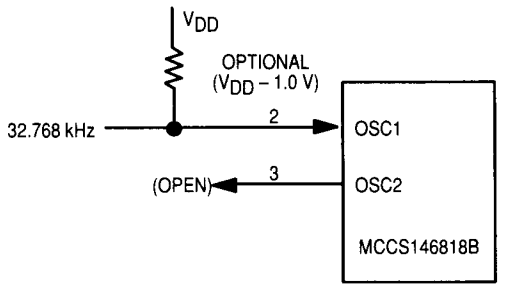
Pin numbers for the PDIP are in parenthesis (Pin 1) and pin numbers for the PLCC package are in brackets {Pin 1}.

MOT —MOTOROLA/INTEL (Input, Pin 1) {Input, Pin 2}

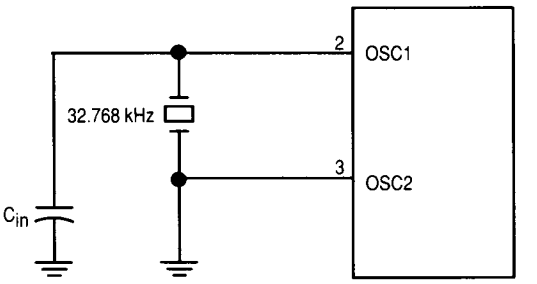
This pin is used to select different bus timing structures. When V_{DD} or a logic high is applied to this pin, the MCCS146818B responds to a Motorola microprocessor bus cycle. If a logic low or V_{SS} is applied to this pin, the Intel bus cycle is used. This pin should be hard-wired to V_{DD} or V_{SS} and should not change states during normal operation. This pin has an internal 20 kΩ pulldown resistor.

OSC1, OSC2 — OSCILLATOR/CRYSTAL (Input/Output, Pins 2, 3) {Input/Output, Pins 3, 4}

These pins serve a single function in two different ways. First, the user may attached a 32.768 kHz quartz crystal to these pins to supply the on-board oscillator with a frequency reference. Secondly, OSC1 may be used to supply the MCCS146818B an off-chip 32.768 kHz signal to run the internal counters. This signal may be supplied from a can oscillator or other source. Figure 1 shows the schematic for both these configurations. Figure 2 shows the crystal equivalent circuit. External trimming capacitors are required and the voltage requirements are $0 V \le V_{in} \le V_{DD}$. The fixed input capacitor shown in Figure 1 may be replaced by a 5–15 pF tunable cap when higher accuracy is desired.



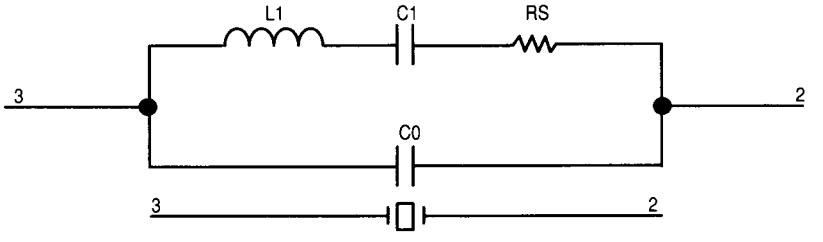
1a — EXTERNAL SOURCE



The value of C_{in} should be chosen according to the suppliers specifications.

1b — CRYSTAL SOURCE

Figure 1. Oscillator Input Configurations



f_{osc}	32.768 kHz
R_S (max)	50 kΩ
C_0 (max)	1.7 pF
C_1	0.003 pF
Q	40 k
C_{XTAL}	6–8 pF*
C_{in}	2–10 pF Fixed*

*May vary due to board layout

Figure 2. Crystal Equivalent Circuit

AD0–AD7 — ADDRESS/DATA (Input/Output, Pins 4–11) {Input/Output, Pins 5–10, 12, 14}

These pins are the media for which data and information is passed to and from the system microprocessor or other host. These pins are multiplexed and supply the MCCS146818B with both address and data. An address is applied to these pins, and then an address select is applied to the AS pin (see the AS pin description). After the address is applied the RAM or clock location may be read from or written to depending on the other control signals applied to the MCCS146818B. During a read cycle the data is valid just after the DS or $\overline{RD}$ signal is applied. The bus returns to a high impedance state, after DS is removed. The delay is defined by t_{DDR} in the timing characteristics. During a write cycle the data must be stable just before the DS or $\overline{WR}$ signal goes high. This parameter is also supplied in the AC characteristics of this data sheet. The address must be valid just prior to the fall of AS. This pin has an active pulldown of approximately 20K.

$\overline{CS}$ — CHIP SELECT (Input, Pin 13) {Input, Pin 16}

This pin is used by the host's address decoding scheme to select or enable this device. This signal must be stable over the entire cycle. If unused, this input should be grounded. If grounded, the application must always use AS and DS in pairs as any AS latchs a new address into the internal address latch. For instance, if the $\overline{CS}$ pin is grounded and a AS occurs, an address is latched into the internal address buffer and internal decoding takes place to select the proper RAM or clock location. At this point, a DS should be applied to act upon the data in that RAM or clock location.

When V_{DD} is below $V_{BATT} \times 1.25$, the MCCS146818B internally inhibits access cycles by internally disabling the $\overline{CS}$ input. This action protects both the MCCS146818B clock data and RAM data from a spurious write during a power cycle. This pin has an active pulldown of approximately 20K.

AS — ADDRESS STROBE (Input, Pin 14) {Input, Pin 17}

This pin is used to multiplex the address/data bus. When an address is supplied to the MCCS146818B, this pin is pulsed, latching the address into internal latches. After this occurs, the data may then be transferred to or from the MCCS146818B via the address/data bus. This pin has an active pulldown of approximately 20K. See **Application Information** for more information.

R/$\overline{W}$ — READ/WRITE (Input, Pin 15) {Input, Pin 19}

The MOTEL circuit treats the R/$\overline{W}$ pin in one of two ways. When a Motorola type processor is connected, R/$\overline{W}$ is a level sensitive input which indicates whether the current cycle is a read or write cycle. A read cycle is indicated with a high level on R/$\overline{W}$ while DS is high, a write is a low on R/$\overline{W}$ during DS.

The second interpretation of R/$\overline{W}$ are as negative write pulses, $\overline{WR}$, $\overline{MEMW}$, and $\overline{IOW}$ from an Intel processor. The MOTEL circuit in this mode gives R/$\overline{W}$ the same meaning as a write (W) pulse on many generic RAMs. This pin has an active pulldown of approximately 20K.

DS — DATA STROBE (Input, Pin 17) {Input, Pin 21}

The DS pin has two interpretations via the MOT circuit. When emanating from a Motorola type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and $\phi 2$ ($\phi 2$ clock or phase 2 clock). During read cycles, DS signifies the time that the MCCS146818B is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the MCCS146818B to latch the written data. See **Application Information**, item 2, for more information.

The second MOT interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, and $\overline{IOR}$ emanating from the Intel processor. In this case, DS identifies the time period when the MCCS146818B drives the bus with read data. This interpretation of DS is also the same and an output-enable signal on a typical memory. This pin has an active pulldown of approximately 20K.

$\overline{RESET}$ — RESET (Input, Pin 18) {Input, Pin 22}

The $\overline{RESET}$ pin does not affect the clock, calendar or RAM functions of the MCCS146818B. On power up, the $\overline{RESET}$ pin must be held low for the specified item, t_{RLH}, in order for the power supply to stabilize during the power cycle.

When $\overline{RESET}$ is low the following occurs:

a) Periodic interrupt enable (PIE) bit is cleared to zero.
b) Alarm interrupt enable (AIE) bit is cleared to zero.
c) Update ended interrupt flag (UF) bit is cleared to zero.
d) Interrupt request status flag (IRQF) bit is cleared to zero.
e) Periodic interrupt flag (PF) is cleared to zero.
f) The device is not accessible.
g) Alarm interrupt flag (AF) bit is cleared to zero.
h) $\overline{IRQ}$ pin is in a high impedance state.
i) Square wave output enable (SQWE) is cleared to zero.
j) Update ended interrupt enable (UIE) is cleared to zero.

In a typical application $\overline{RESET}$ may be connected to V_{DD}. This connection allows the MCCS146818B to go in and out of power fail without affecting any of the control registers. $\overline{RESET}$ function is not available when $V_{DD} < (1.25 * V_{BAT})$. This pin has an active pulldown of approximately 20K.

$\overline{IRQ}$ — INTERRUPT REQUEST (Output, Pin 19) {Input, Pin 23}

The $\overline{IRQ}$ pin is an active-low open-drain to ground output of the MCCS146818B that may be used as an interrupt input to a processor. This $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C. The $\overline{RESET}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor. $\overline{IRQ}$ is disabled during Stand-by Mode.

V_{BATT} — BACKUP POWER (Pin 20) {Input, Pin 24}

This pin supplies the MCCS146818B with power while the system is in Stand-by Mode. This input is designed for a 3.0 volt lithium cell. This voltage needs to be held between 2.2 and 3 volts for proper operation. The nominal write protect trip point voltage at which access to the MCCS146818B is prohibited, is set by internal circuitry as $1.25 \times V_{BATT}$. A maximum load of 500–700 nA at 25°C in the absence of V_{DD} should be used to size the battery or other source.

This device is optimized for a lithium cell. If a NiCAD is used the application must not allow the charging voltage at pin 20 to exceed the $V_{BATT} \times 1.25$ criteria. If the voltage at the V_{BATT} pin is too great, the device's internal power switching circuit disallows access to the device.

$\overline{RCLR}$ — RAM CLEAR (Input, Pin 21) {Input, Pin 25}

The $\overline{RCLR}$ pin is used to clear (set to logic high ($FF) or V_{DD}), all 114 bytes of general-purpose RAM but does not affect the RAM associated with the clock and calendar functions, or registers. In order to clear the RAM, $\overline{RCLR}$ must be forced to an input logic low (V_{SS}) during battery backup mode when V_{DD} is not applied. This can be done by placing a jumper from $\overline{RCLR}$ to V_{SS} while the device is powered down.

SQW — SQUARE WAVE (Output, Pin 23) {Input, Pin 27}

The SQW pin can output a signal from one of the 13 taps provided by the 15 internally-divided stages. The frequency of the SQW may be altered by programming Register A, as shown in Table 2. The SQW signal may be turned on by setting the SQWE (square wave enable) bit in Register B to a '1', logic high.

V_{DD} — POWER (Pin 24) {Power, Pin 28}

DC power, + 5 Vdc, is provided to the MCCS146818B via this pin. This pin only supplies power during normal operation. During stand-by mode, power is supplied via the V_{BATT} pin.

V_{SS} — POWER (Pins 12, 16) {Pins 15, 20}

These pins supply the MCCS146818B with system ground. Pin 16 is convenient to ground the back-up battery; however, this ground may also be used as a system ground along with the battery ground. Both pins should be grounded for optimum performance.

NC — No-Connect (Pin 22) {Pins 1, 11, 13, 18, 26}

These pins are not connected to any internal device.

5.0 REGISTER DESCRIPTIONS

The MCCS146818B has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

5.1 REGISTER A — READ/WRITE — ($0A)

MSB							LSB
7	6	5	4	3	2	1	0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

Bit 7 — UIP — Update in Progress

The update in progress bit is a status flag that may be monitored by the program. When UIP is a '1', if the update cycle is not in progress it will soon begin. When UIP is a 0, the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is '0'. The UIP is a read-only bit, and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in register B to a 1 inhibits any update transfer and clears the UIP status bit.

Bits 6, 5, 4 — DV2, DV1, DV0 — Divider

These three bits are used to turn the oscillator on and off and to reset the count-down chain. A pattern of '010' is the only combination of bits which will turn the oscillator on and allow the MCCS146818B to keep time. A pattern of '11X' will enable the oscillator but holds the countdown chain in reset. The next update will occur at 500 ms after a pattern of '010' is written to DV2, DV1, DV0. See Table 1 for more information.

Bits 3, 2, 1, 0 — RS3, RS2, RS1, RS0 — Rate Select

The four rate selection bits select one of 13 taps of the 15-stage divider, or disable the divider output. The tap selected may be used to generate an output square wave (SQW) and/or a periodic interrupt. The program may do one of the following:

1) Enable the interrupt with the PIE bit
2) Enable the SQW output pin with the SQWE bit
3) Enable both at the same time at the same rate
4) Enable neither

Table 2 lists the periodic interrupt rates and the square wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by $\overline{\text{RESET}}$.

5.2 REGISTER B — READ/WRITE — ($0B)

MSB							LSB
7	6	5	4	3	2	1	0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

Bit 7 — SET

When the SET bit is 0, the update cycle functions normally by advancing the count once per second. When the SET bit is written to a 1, any update cycle is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initialization. SET is a read/write bit which is not modified by $\overline{\text{RESET}}$ or an internal function of the MCCS146818B.

Bit 6 — PIE — Periodic Interrupt Enable

This bit is a read/write bit which allows the periodic interrupt flag (PF) bit in register C to drive the $\overline{\text{IRQ}}$ pin low. A program writes a 1 to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in register A. A '0' in PIE blocks $\overline{\text{IRQ}}$ from being initiated by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is not modified by any internal MCCS146818B functions, but is cleared to 0 by $\overline{\text{RESET}}$.

Bit 5 — AIE — Alarm Interrupt Enable

This bit is a read/write bit which when set to a 1 permits the alarm flag (AF) bit in Register C to assert $\overline{\text{IRQ}}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code by binary 11XXXXXX). When the AIE bit is a '0', the AF bit does not initiate an $\overline{\text{IRQ}}$ signal. The $\overline{\text{RESET}}$ pin clears AIE to '0'. The internal functions do not affect the AIE bit.

Table 1. Divider Configurations

DV2	DV1	DV0	Divider $\overline{\text{RESET}}$	Oscillator
0	0	0	No	Off
0	0	1	No	Off
0	1	0	No	On
0	1	1	No	Off
1	0	0	No	Off
1	0	1	No	Off
1	1	0	Yes	On
1	1	1	Yes	On

Table 2. Periodic Interrupt and Square Wave Output Frequency

RS3	RS2	RS1	RS0	Periodic Interrupt Rate TPI	SQW Output Frequency
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	112.070 µs	8.192 kHz
0	1	0	0	244.141 µs	4.096 kHz
0	1	0	1	488.284 µs	2.048 kHz
0	1	1	0	976.562 µs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

Bit 4 — UIE — Update-Ended Interrupt Enable

This bit enables the update-ended flag (UF) bit in Register C to assert $\overline{IRQ}$ allowing an interrupt when an update is finished. The $\overline{RESET}$ pin does not affect the UIE.

Bit 3 — SQWE — Square Wave Enable

When this bit is set to a '1' by the programmer, a square wave signal at the frequency specified in the rate selection bits (RS3–RS0) in register A appears on the SQW pin. When the SQWE bit is set to a '0', the SQW pin is held low. The state of SQWE is cleared by the $\overline{RESET}$ pin. This bit is reset to '0' when V_{DD} is cycled.

Bit 2 — DM — Data Mode

This bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{RESET}$. A '0' in DM signifies binary-coded-decimal (BCD) data, a '1' in DM signifies binary data.

Bit 1 — 24/12 — 24/12 Control Bit

This establishes the format of the hours bytes as either the 24-hour mode (24/12 = 1) or the 12-hour mode (24/12 = 0). This bit is affected only by the software; $\overline{RESET}$ does not change this bit.

Bit 0 — DSE — Daylight Savings Enable

This bit is a read/write bit which allows the program to enable two special updates (DSE = 1). On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM, it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a 0. DSE is not changed by any internal operations or $\overline{RESET}$. The day of week byte must be set for the DSE function to operate properly.

5.3 REGISTER C — READ ONLY — ($0C)

MSB							LSB
7	6	5	4	3	2	1	0
IRQF	PF	AF	UF	0	0	0	0

Bit 7 — IRQF — Interrupt Request Flag

This bit is set to a 1 when one or more of the following are true:

1) PF = PIE = 1
2) AF = AIE = 1
3) UF = UIE = 1

i.e., IRQF = (PF × PIE) + (AF × AIE) + (UF × UIE)
Any time the IRQF bit is a 1, the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read or when $\overline{RESET}$ occurs.

Bit 6 — PF — Periodic Interrupt Flag

This bit is a read-only bit which is set to a 1 when a particular edge is detected on the selected tap of the divider chain. The RS3–RS0 bits establish the periodic rate. PF is set to a '1' independent of the state of the PIE bit. PF being a '1' initiates an $\overline{IRQ}$ signal and sets the IRQF bit only when PIE is also a '1'. The PF bit is cleared by a $\overline{RESET}$ or a read of Register C.

Bit 5 — AF — Alarm Flag

A '1' in this bit indicates that the current time has matched the alarm time. A '1' in AF causes the $\overline{IRQ}$ pin to go low and a '1' to appear in the IRQF only when the AIE bit is also set to a '1'. A $\overline{RESET}$ or a read of Register C clears AF.

Bit 4 — UF — Update-Ended Interrupt Flag

This bit is set after each update cycle. When the UIE bit is a 1 the 1 in UF causes the IRQF bit to be a 1 asserting $\overline{IRQ}$. UF is cleared by a register C read or a $\overline{RESET}$.

Bits 3–0 — Unused

These bits are unused and are read as 0. They can not be written.

5.4 REGISTER D — READ ONLY — ($0D)

MSB							LSB
7	6	5	4	3	2	1	0
VRT	0	0	0	0	0	0	0

Bit 7 — VRT — Valid RAM and Time

This bit indicates the condition of the contents of the RAM. A '0' appears in the VRT bit when $V_{BATT} < 2.2$ V. This indicates invalid data in RAM or questionable data in RAM. The VRT is a read-only bit which is not modified by the $\overline{RESET}$ pin. The VRT bit can only be reset by reading register D.

Bits 6–0 — Unused

These bits are not used and should not be written to.

6.0 FUNCTIONAL DESCRIPTION

6.1 ADDRESS MAP

Figure 3 shows the address map of the MCCS146818B. The memory consists of 114 general-purpose RAM bytes; 10 RAM bytes which contain the time, calendar, and alarm data; and 4 RAM bytes which contain control and status information. All 128 bytes are directly readable and writable by the processor program except for the following: 1) Register C and D are read only, 2) bit 7 of Register A is read only, and 3) the high-order bit of the seconds byte is read only and is always 0. The contents of the four control and status registers (A, B, C, and D) are described in **Register Descriptions**.

6.2 TIME, CALENDAR, AND ALARM LOCATIONS

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm bytes may either be binary-coded-decimal (BCD) or binary. Before initializing the internal registers, the SET bit in Register B should be set to a 1 to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, binary or BCD. The SET bit may now be cleared to allow updates. Once initialized, the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23 hours. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high-order bit of the hours byte represents PM when it is a 1.

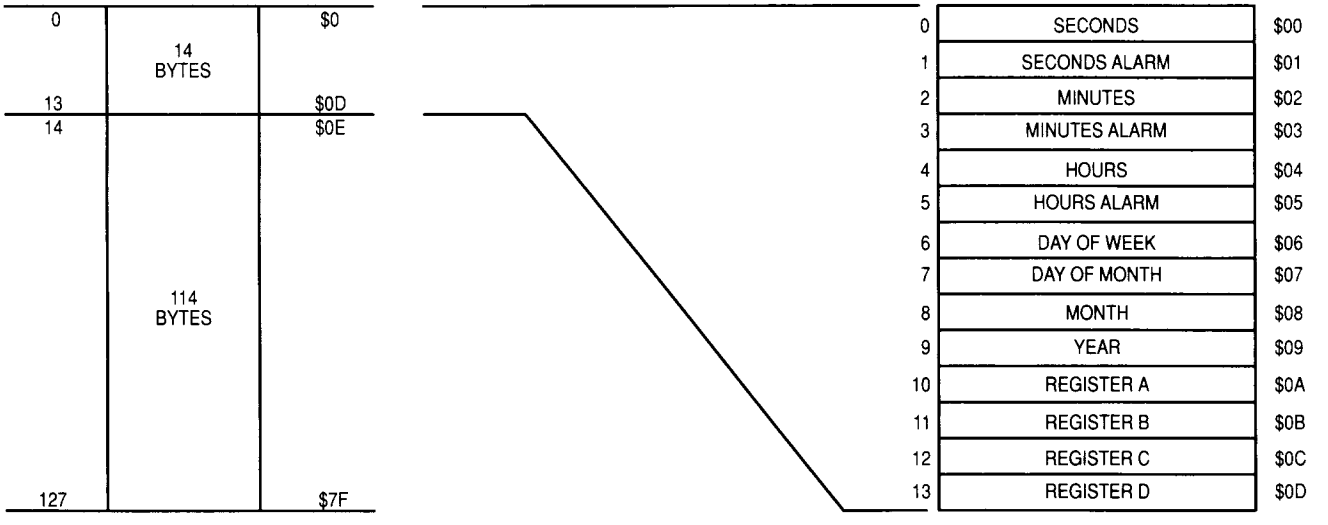


Figure 3. MCCS146818B Address Map

Table 3. Time, Calendar, and Alarm Data Modes

Address Location	Function	Decimal Range	Range	
			Binary Data Mode	BCD Data Mode
$0	Seconds	0-59	$00–$3B	$00–$59
$1	Second Alarm	0–59	$00–$3B	$00–$59
$2	Minutes	0–59	$00–$3B	$00–$59
$3	Minute Alarm	0–59	$00–$3B	$00–$59
$4	Hours 12 Hour 24 Hour	 1–12 0–23	 $01–$0C AM $81–$8C PM $00–$17	 $10-$12 AM $81–$92 PM $00–$23
$5	Hour Alarm 12 Hour 24 Hour	 1–12 0–23	 $01–$0C AM $81–$8C PM $00–$17	 $01–$12 AM $81–$92 PM $00–$23
$6	Day of Week Sunday = 1	 1–7	 $01–$07	 $01–$07
$7	Day of Month	1–31	$01–$1F	$01–$31
$8	Month	1–12	$01–$0C	$01–$12
$9	Year	0–99	$00–$63	$00–$99

The three alarm bytes may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a don't care code in any hexadecimal byte from $CO to $FF. That is, the two most significant bits of each byte when set to 1, create a don't care situation. An alarm interrupt each hour is created with a don't care code in the hours alarm locations. Similarly, an alarm is generated every minute with don't care codes in the hours and minutes alarm bytes. The don't care codes in all three alarm bytes create an interrupt every second.

6.3 STATIC CMOS RAM

The 114 bytes of general-purpose RAM are not dedicated within the MCCS146818B. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back up, very frequently there is other non-volatile data that must be retained when main power is removed. The 114 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional MCCS146818Bs may be included in the system. The time/calendar functions may be disabled by holding the DV0–DV2 dividers in Register A in the reset state by setting the SET bit in register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 123 bytes. The high-order bit of the seconds byte ($02) (read as '0'), bit 7 of Register A and all bits of Registers C and D cannot effectively be used as general-purpose RAM.

6.4 POWER DOWN CONSIDERATIONS

During and after the power source conversion, the V_{in} maximum specification must never be exceeded. Failure to meet the V_{in} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part. During the transition from system to battery power, the designer of a battery backed-up system must protect data integrity, minimize power consumption, and ensure hardware reliability.

When V_{DD} is applied to the MCCS146818B, and reaches a level of greater than V_{BATT} pin potential x 1.25, the device becomes accessible. When V_{DD} falls below V_{BATT} x 1.25, the chip select input is internally forced to an inactive level regardless of the value of $\overline{CS}$ at the input pin and the MCCS146818B is write protected. When the MCCS146818B is in a write protected state, all inputs are ignored and all outputs are in a high impedance state.

6.5 UPDATE CYCLE

The MC146818B executes an update cycle once per second provided the DV0–DV2 divider bits are 010 and the SET bit (in Register B) is clear. When an update cycle occurs, the contents of an internal copy of the time-keeping RAM is updated. A transfer of the user copy RAM to the internal RAM occurs prior to the update when a write to any of the time-keeping RAM has been detected between update cycles. After the update cycle is finished, the new values will be written to the user copy of the time-keeping RAM.

An exception to the update cycle occurs when the SET bit in REG B is set to a one (1). The SET bit in a one (1) state permits the program to initialize the time and calendar bytes by inhibiting update transfers. If the SET bit is set to a one (1) RAM will be frozen, but the internal copy or RAM will continue to keep time and will issue an alarm match if it occurs. Upon the

release of the SET bit, update cycles would result with a transfer of data to the user copy RAM.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match occurs or if a don't care code (11XXXXXX) is present in all three positions.

Three methods of accommodating non-availability during update are usable by the program. In discussing the three methods, it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transferred to continually available RAM. Before leaving the interrupt service routing, the IRQF bit in Register C should be cleared.

The second method uses the UIP in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once per second. After the UIP bit goes high, the update cycle begins 244 µs before the time/calendar data may be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 µs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C. Periodic interrupts that occur at a rate of greater that $t_{BUC} + t_{UC}$ allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(t_{PL}/2) + t_{BUC}$ to ensure that data is not read during the update cycle.

To properly setup for daylight savings time operation, the user must set the time at least one second before the roll over will occur (i.e., 1:59:59 AM). See Figure 4.

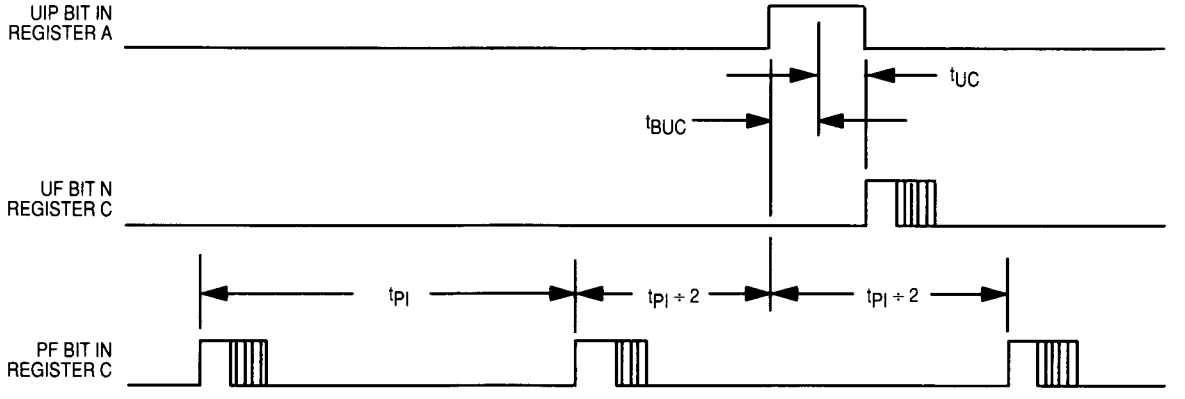
6.6 DIVIDER STAGES

The MCCS146818B has 15 binary-divider stages following the time base as shown in the block diagram. The output of the dividers is a 1 Hz signal to the update system logic. The dividers are controller by three divider bits (DV2, DV1, DV0) in Register A. The only time base for this device is 32.768 kHz. The divider chain may be held at reset, which allows precision setting of the time. When the divider is changed from reset to an operation time base, the first update system is one second later.

6.7 SQUARE-WAVE OUTPUT SELECTION

13 of the 15 divider taps are made available to a 1-of-15 selector as shown in the block diagram. The first purpose of selecting a divider tap is to generate a square wave output signal at the SQW pin. The RS0–RS3 bits in Register A establish the square wave frequency as listed in Table 2. The SQW frequency selection shares the 1-of-15 selector with the periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave output selection bit (SQWE bit) in Register B. The MCCS146818B then generates an asymmetrical waveform at the time of execution. The square save output pin has a number of potential uses. For example, it can serve as a frequency standard for internal use, a frequency synthesizer, or should be used to generate one or more audio tones under program control.



t_{PI} = Periodic Interrupt Time Interval (500 ms, 125 ms, 62.5 ms, etc. per Table 2)
t_{UC} = Update Cycle Time (1984 µs)
t_{BUC} = Delay Time Before Update Cycle (244 µs)

Figure 4. Update Ended and Periodic Relationships

6.8 INTERRUPTS

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-per-day. The periodic interrupt may be selected for rates from half-a-second to 122 µs. The update-ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections of this data sheet.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a '1' to an interrupt-enable bit allows the interrupt to be initiated when the event occurs. A '0' in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{IRQ}$ pin is immediately activated, though the interrupt causing the event may have occurred much earlier. Thus, there are cases where the programs should clear such earlier interrupts before first enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a '1' in register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned or polling case, the program does not enable the interrupt. The interrupt flag bit becomes a status bit, which the software interrogates when it wishes. When the software detects that the flag is set, it is an indication to the software that the interrupt event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable through the read cycle.

All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held after the read cycle. One, two, or three flag bits may be found to be set when Register C is used. The program should inspect all utilized flag bits every time register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted a long as one of the three interrupted sources has its flag and enables bits set. The IRQF bit in Register C is a '1' whenever the $\overline{IRQ}$ pin is being driven low.

The processor program can determine that the RTC initiated the interrupt by reading register C. A '1' in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bit set and service each interrupt which is set. Again, more than one interrupt-flag may be set.

6.9 PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500 ms to once every 122 µs. The periodic interrupt is separate from the alarm interrupt which may be output from once per second to once per day.

Table 2 shows that the periodic interrupt rate is selected with the same Register A bits which select the square wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit in Register B. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real time systems. It can be used to scan for all forms of inputs from contact closure to serial receive bits or bytes. It can be used in multiplexing displays or with software counters to measure inputs, creating output intervals, or await the next needed software function.

7.0 APPLICATION INFORMATION

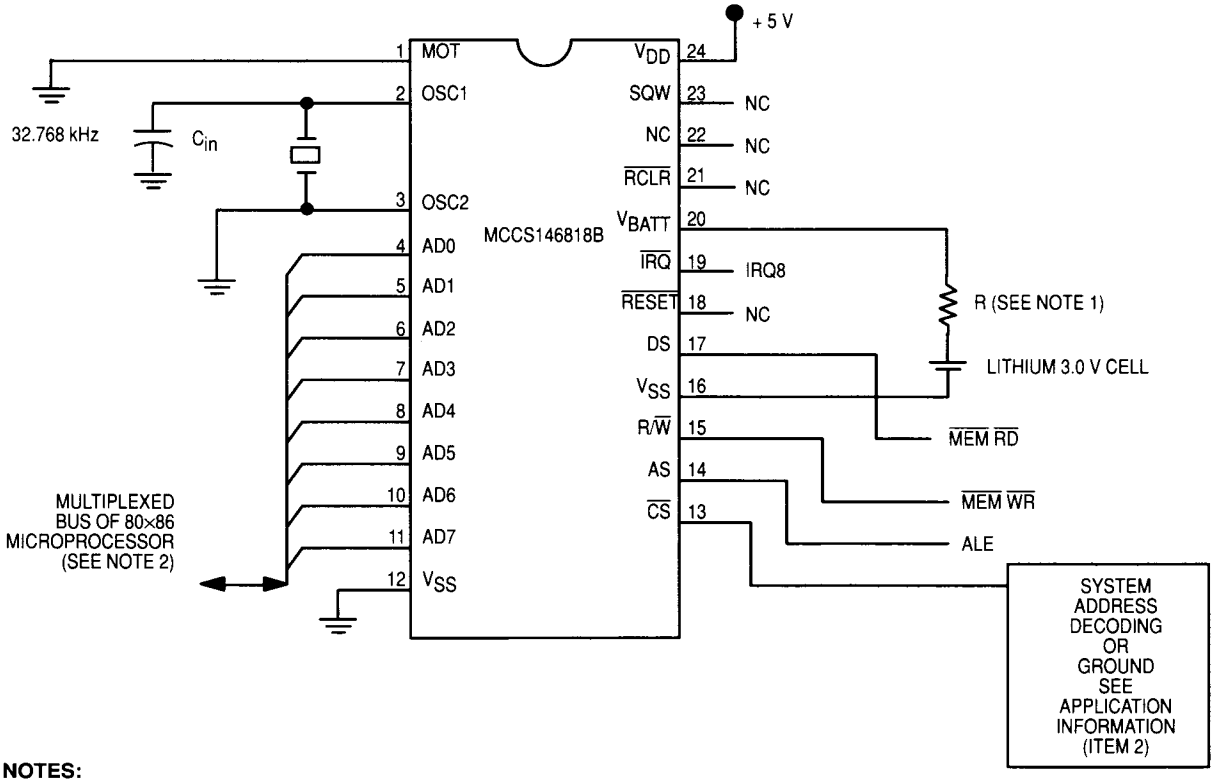
Refer to Figures 5 through 9 and the following notes for application examples. Pin numbers for the FN package are in brackets.

1. The MCCS146818B will drop directly into a MCCS146818A circuit with some modifications. The user may use the MCCS146818B if the following steps are taken:
   a) Cut trace or wire going to pin 20 {24} (CKFS); this is a battery connection on the MCCS146818B. The user needs to supply battery back-up power to this pin. A 3.0 V lithium cell is suggested.
   b) Cut the trace or wire to pin 21 {25} ($\overline{RCLR}$); this pin is used to clear the contents of the RAM in stand-by mode.
   c) It is not recommended to connect any signal to pin 22 {1, 11, 13, 18, 26} (NC). Therefore, it is suggested that the user cut the wire or trace going to this pin and leave it open.
   d) The user will need to disconnect the battery from pin 24 {28} (V_{DD}). The battery connection for the MCCS146818B is on pin 20 {24}. While ni-cads may be used (see V_{BATT} in Pin Descriptions) the part is designed for lithium.
   e) The MCCS146818B is a one-frequency device. The only crystal this chip accepts is the 32.768 kHz type. If the user has the 1, 2, or 4 MHz crystal or oscillator in the MCCS146818A circuit, these will need to be replaced with the 32.768 kHz type. For this reason, the MCCS146818B cannot be used in applications that take advantage of the MCCS146818A's 1, 2, or 4 MHz clock outputs.
   f) Pin 16 {20} (V_{SS}) is used for a system ground. The MCCS146818A used this as a stand-by input signal. This function is now done internally and this trace or wire will need to be replaced with a system ground or with a battery ground.
   g) The user may also wish to replace the MCCS146818A with a MCCS146818B1M, which will eliminate all above except b) and e). The $\overline{RCLR}$ pin on the MCCS146818B1M will need to be clipped off for proper operation. Or, the user may wish to use the MCCS146818BM which already has pin 21 {25} clipped. The MCCS146818BM is a device which includes the MCCS146818B along with a crystal and a battery on board encapsulated into a module. The MCCS146818B1M is the same module with $\overline{RCLR}$ available.

2. In some applications, the user may choose to tie $\overline{CS}$ directly to ground. This is acceptable: however, this will force the programmer to always apply AS and DS in pairs. This means that if $\overline{CS}$ is grounded, any ALE (IBM/Intel timing cycle) will cause a new address to be latched into the MCCS146818B. It is good practice to use the AS and DS signals in pairs at any time in any application. It is also good practice to use a true chip select derived from address decoding for $\overline{CS}$.

   If $\overline{CS}$ is grounded, the user must always use AS and DS in pairs since any AS will latch a new address into the internal address latch. For instance, If the $\overline{CS}$ pin is grounded and a AS occurs an address is latched into the internal address buffer and internal decoding takes place to select the proper RAM or clock location. At this point, a DS should be applied to act upon the data in said RAM or clock location.

3. C_{in} is dependent on C_{LOAD} of XTAL being selected.
4. This device is optimized for a lithium cell. If a NiCAD is used the application must not allow the charging voltage at pin 20 {24} to exceed the $V_{BATT} \times 1.25$ criteria. That is, if the voltage at pin 20 {24} is too great, the devices internal power switching circuit will disallow access to the device.



NOTES:
1. R is for UL listing. See battery suppliers specification sheet for proper size.
2. The IBM AT writes a 7–bit address to I/O port $70 and then reads the data from I/O port $71 or writes I/O address $71. This is a typical application for a non-multiplexed bus.
3. C_{in} is dependent on C_{LOAD} of XTAL being selected.

Figure 5. IBM/INTEL Application Circuit Multiplexed Bus IBM PC/AT Intel 80 × 86 Multiplexed Bus Microprocessors

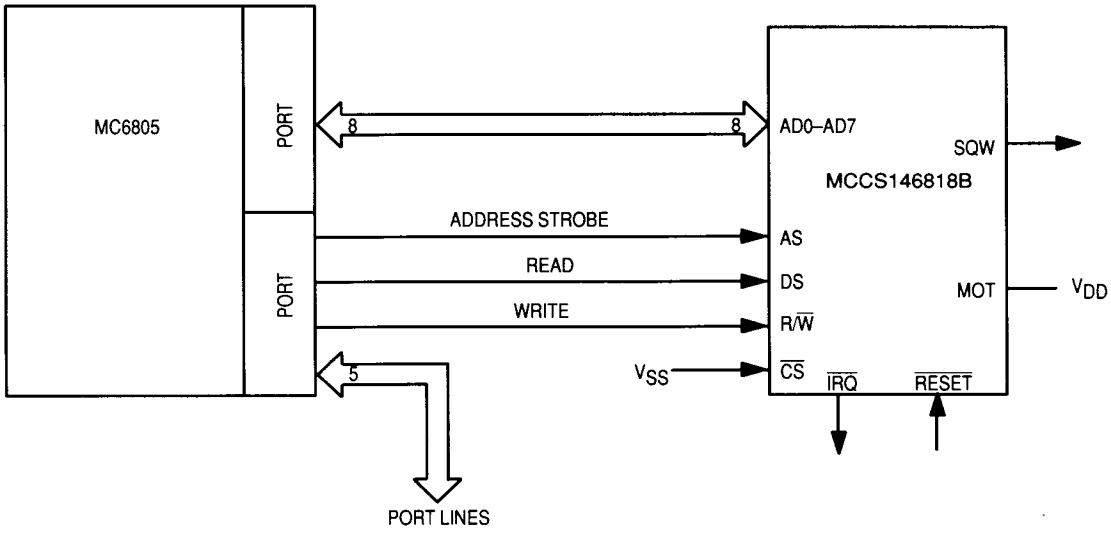


Figure 6. MCCS146818B Interfaced with the Ports of a Typical Single-Chip Microcomputer

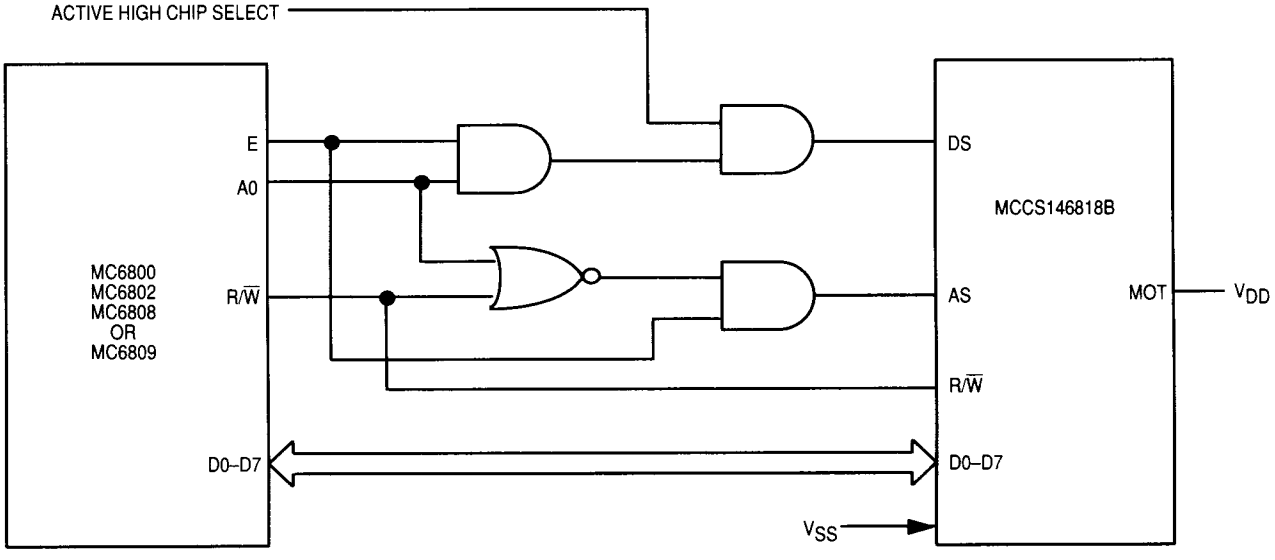


Figure 7. MCCS146818B Interfaced with Motorola Processors

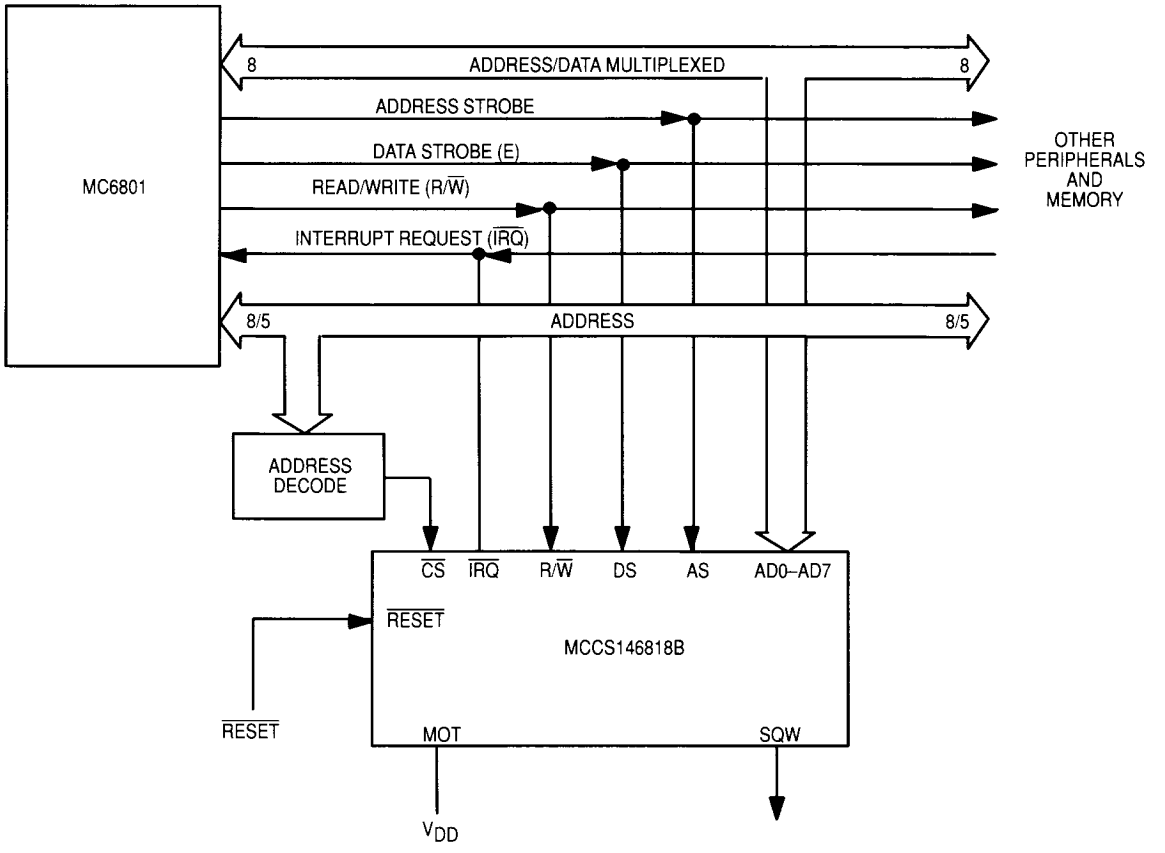


Figure 8. MCCS146818B Interfaced with Motorola Compatible Multiplexed Bus

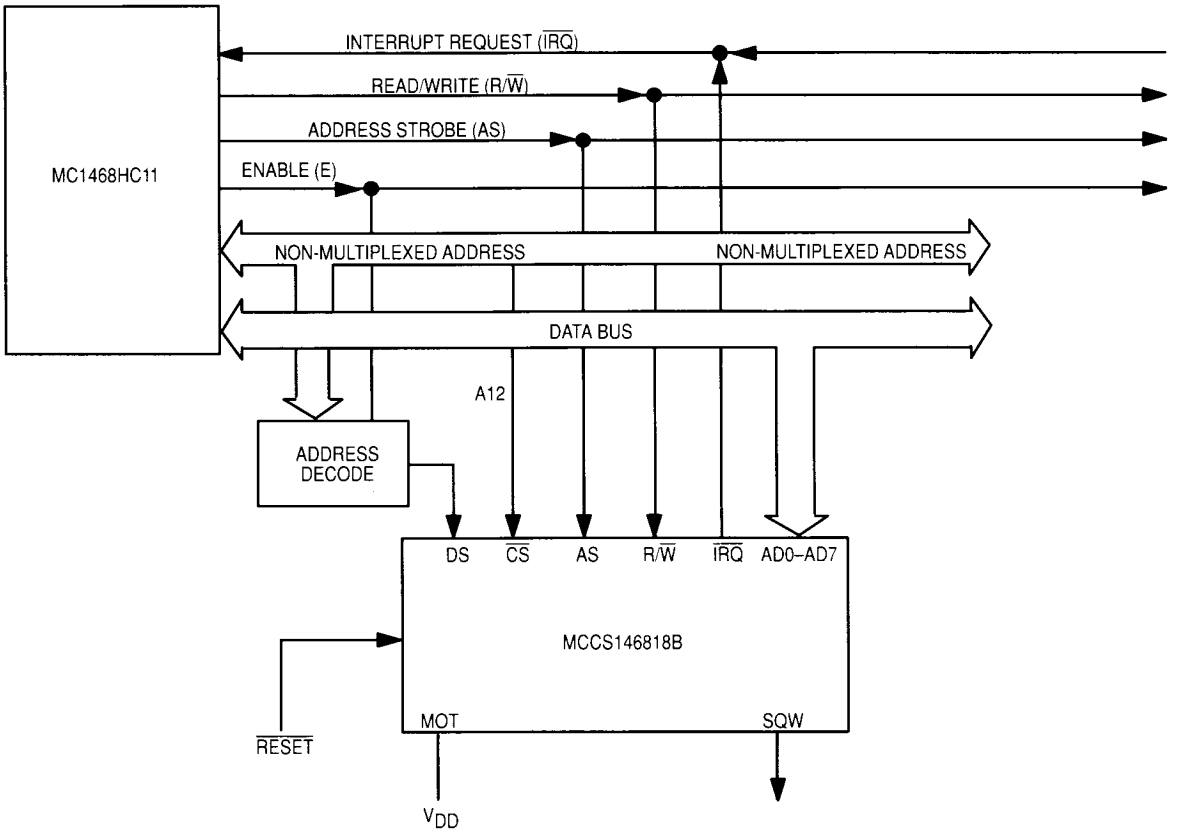
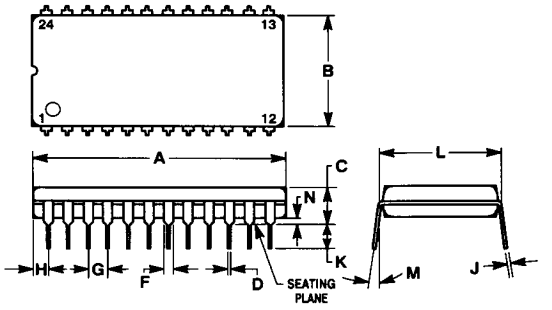


Figure 9. MCCS146818B Interfaced with MC1468HC11 CMOS Multiplexed Microprocessor with Slow Address Decoding

8.0 PACKAGE DIMENSION

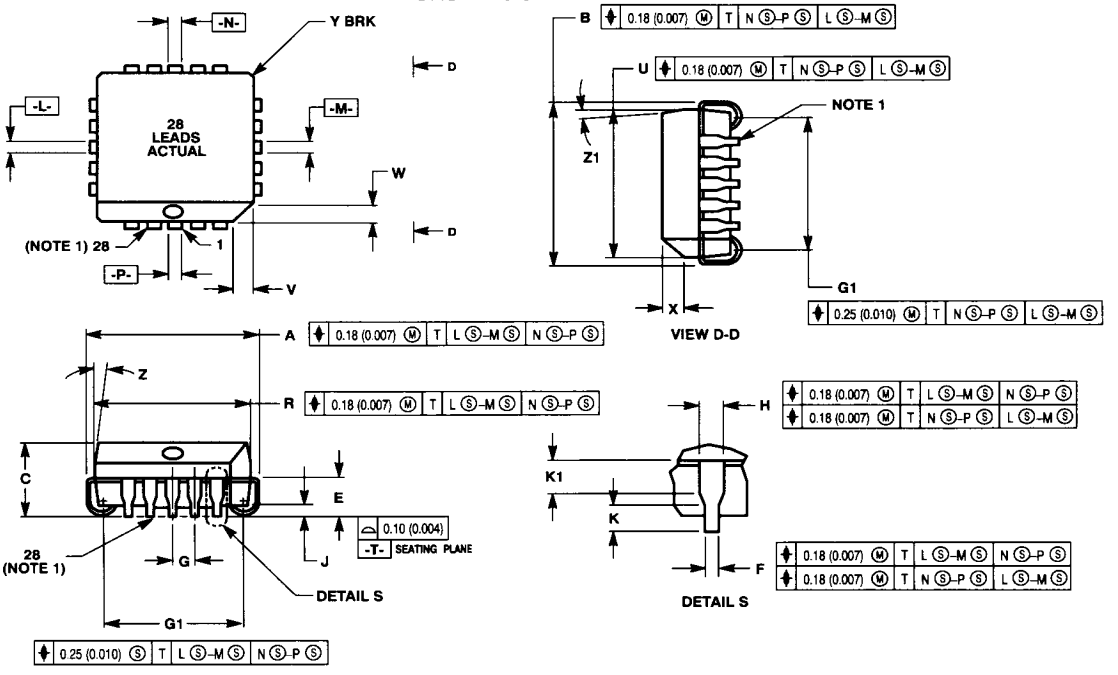
P PACKAGE
CASE 709-02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

FN PACKAGE
PLASTIC
CASE 776-02



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.