

MM54HC299/MM74HC299 8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes advanced silicon-gate CMOS technology. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HC299/MM74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines S0 and S1 high. This places the TRI-STATE outputs in a high impedance state, which

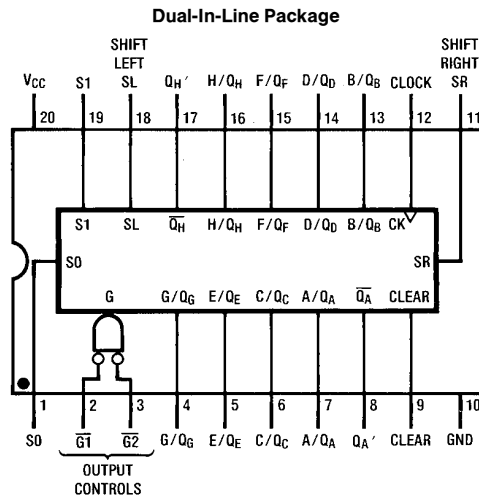
permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency 40 MHz
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HC)
- High output drive for bus applications
- Low quiescent current: 1 μA maximum

Connection Diagram



TOP VIEW

TL/F/5207-1

Order Number MM54HC299 or MM74HC299

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{CD})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA (Q_A , Q_H) ± 35 mA (others)
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN} , V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r , t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			Units	
				Typ	74HC $T_A = -40$ to $85^\circ C$	54HC $T_A = -55$ to $125^\circ C$		
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V	
			4.5V	3.15	3.15	3.15	V	
			6.0V	4.2	4.2	4.2	V	
V_{IL}	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V	
			4.5V	1.35	1.35	1.35	V	
			6.0V	1.8	1.8	1.8	V	
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
	Q_A ' & Q_H ' Outputs	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
	A/ Q_A thru H/ Q_H Outputs	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V
6.0V	5.7	5.48	5.34	5.2	V			
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	Q_A ' and Q_H ' Outputs	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
	A/ Q_A thru H/ Q_H Outputs	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V
6.0V	0.2	0.26	0.33	0.4	V			
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\bar{G} = V_{IH}$	6.0V		± 0.5	± 0.5	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst-case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6\text{ ns}, C_L=45\text{ pF}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		40	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A' or Q_H'		25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A' or Q_H'		39	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A-Q_H	$C_L = 45\text{ pF}$	25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A-Q_H	$C_L = 45\text{ pF}$	28	40	ns
t_{PZL}, t_{PZH}	Maximum Enable Time	$C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$	10	35	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time	$C_L = 5\text{ pF}$ $R_L = 1\text{ k}\Omega$	18	25	ns
t_S	Minimum Setup Time	Select		20	ns
		Data		20	ns
t_H	Minimum Hold Time	Select		0	ns
		Data		0	ns
t_W	Minimum Pulse Width		12	20	ns
t_{REM}	Clear Removal Time			10	ns

AC Electrical Characteristics $C_L = 50\text{ pF}, t_r = t_f = 6\text{ ns}$ unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^{\circ}C$		74HC	54HC	Units
				Typ	Guaranteed Limits		$T_A = -40\text{ to }85^{\circ}C$	
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	3.5	MHz	
			4.5V	25	20	18	MHz	
			6.0V	29	23	20	MHz	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A' or Q_H'		2.0V	15	170	210	240	ns
			4.5V	27	38	48	54	ns
			6.0V	25	35	44	49	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A' or Q_H'		2.0V	70	200	250	280	ns
			4.5V	30	44	55	62	ns
			6.0V	26	38	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A-Q_H	$C_L = 50\text{ pF}$	2.0V	65	170	210	240	ns
			$C_L = 150\text{ pF}$	2.0V	100	206	260	295
		$C_L = 50\text{ pF}$	4.5V	27	38	48	54	ns
			$C_L = 150\text{ pF}$	4.5V	34	46	57	66
		$C_L = 50\text{ pF}$	6.0V	25	35	44	49	ns
			$C_L = 150\text{ pF}$	6.0V	31	39	49	55
t_{PHL}	Maximum Propagation Delay, Clear to Q_A-Q_H	$C_L = 50\text{ pF}$	2.0V	70	200	250	280	ns
			$C_L = 150\text{ pF}$	2.0V	110	236	295	325
		$C_L = 50\text{ pF}$	4.5V	30	44	55	62	ns
			$C_L = 150\text{ pF}$	4.5V	37	52	65	75
		$C_L = 50\text{ pF}$	6.0V	26	38	46	52	ns
			$C_L = 150\text{ pF}$	6.0V	32	46	57	64

AC Electrical Characteristic (Continued) $C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$ unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ\text{C}$		74HC $T_A = -40 \text{ to } 85^\circ\text{C}$		54HC $T_A = -55 \text{ to } 125^\circ\text{C}$		Units
				Typ	Guaranteed Limits					
t_{PZH} , t_{PZL}	Maximum Output Enable	$R_L = 1 \text{ k}\Omega$								
		$C_L = 50 \text{ pF}$	2.0V	70	160	200		225		ns
		$C_L = 150 \text{ pF}$	2.0V	90	220	275		310		ns
		$C_L = 50 \text{ pF}$	4.5V	22	32	40		45		ns
		$C_L = 150 \text{ pF}$	4.5V	30	44	55		62		ns
		$C_L = 50 \text{ pF}$	6.0V	19	28	34		38		ns
		$C_L = 150 \text{ pF}$	6.0V	24	47	47		51		ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1 \text{ k}\Omega$	2.0V	70	160	200		225		ns
		$C_L = 50 \text{ pF}$	4.5V	22	32	40		45		ns
			6.0V	19	28	34		38		ns
t_S	Minimum Setup Time, Data Select S_L or S_R		2.0V		100	125		140		ns
			4.5V		20	25		28		ns
			6.0V		17	21		25		ns
t_H	Minimum Hold Time, Data Select S_L or S_R		2.0V		0	0		0		ns
			4.5V		0	0		0		ns
			6.0V		0	0		0		ns
t_{REM}	Minimum Clear Removal Time		2.0V		10	10		10		ns
			4.5V		10	10		10		ns
			6.0V		10	10		10		ns
t_W	Minimum Pulse Width, Clock and Clear		2.0V		100	125		140		ns
			4.5V		20	25		28		ns
			6.0V		17	21		25		ns
t_r , t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000		100		ns
			4.5V		500	500		500		ns
			6.0V		400	400		400		ns
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Time, Clock		2.0V		60	75		90		ns
			4.5V		12	15		18		ns
			6.0V		10	13		15		ns
C_{PD}	Power Dissipation Capacitance	Outputs Enabled		240						pF
		Outputs Disabled		110						pF
C_{IN}	Maximum Input Capacitance Capacitance			5	10	10		10		pF
C_{OUT}	Maximum TRI-STATE Output Capacitance			15	20	20		20		pF

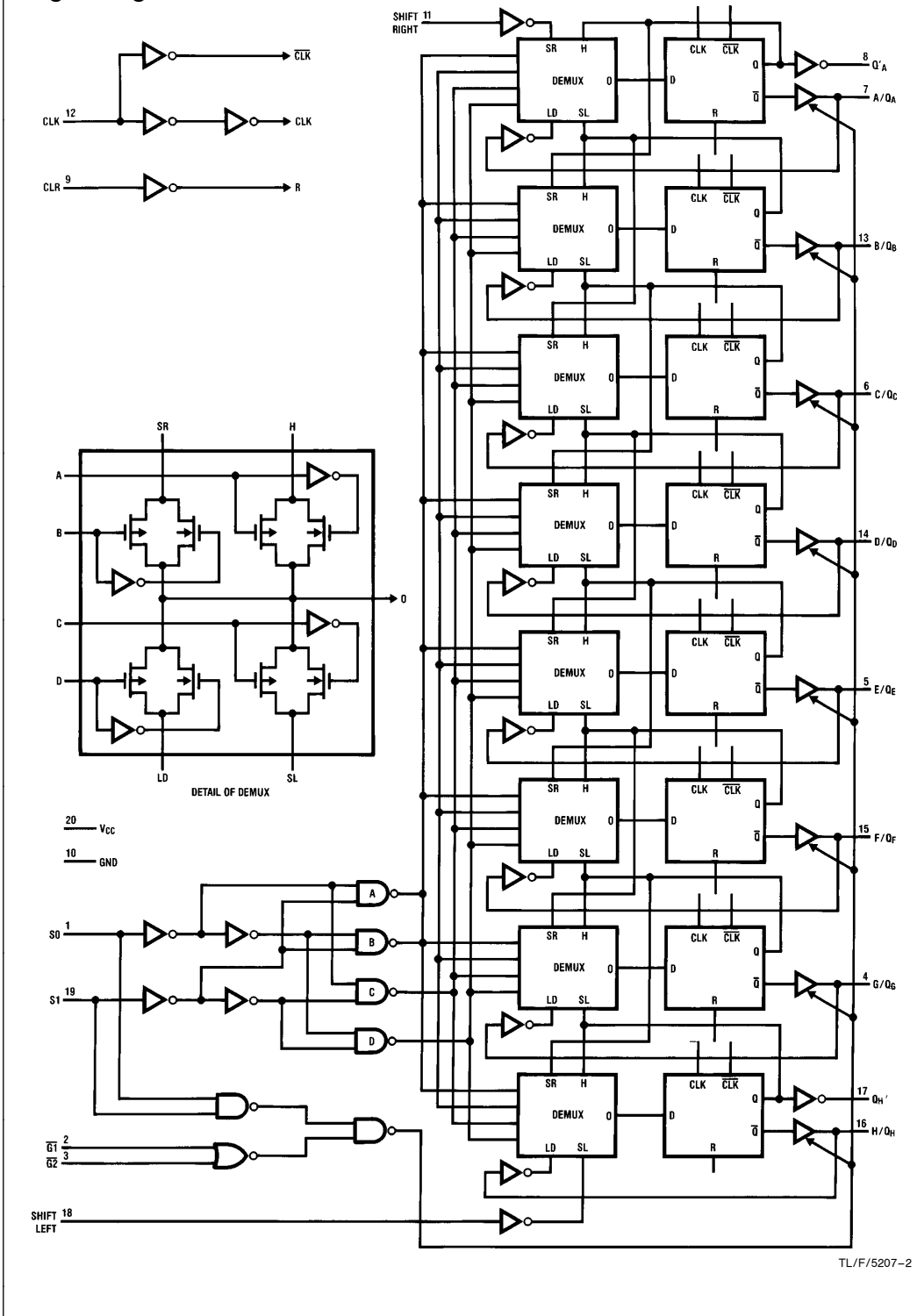
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Function Table

Mode	Inputs						Inputs/Outputs								Outputs			
	Clear	Function Select		Output Control		Clock	Serial		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '
		S1	S0	$\overline{G1}^\dagger$	$\overline{G2}^\dagger$		SL	SR	L	L	L	L	L	L	L	L	L	L
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
	H	X	X	L	L	L or H	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{GN}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{GN}
Shift Left	H	H	L	L	L	↑	H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

† When one or both controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

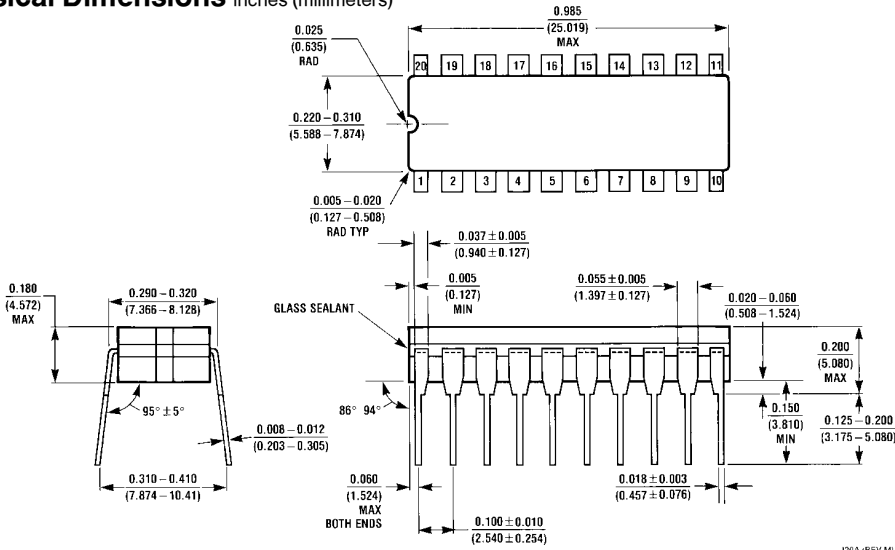
Logic Diagram



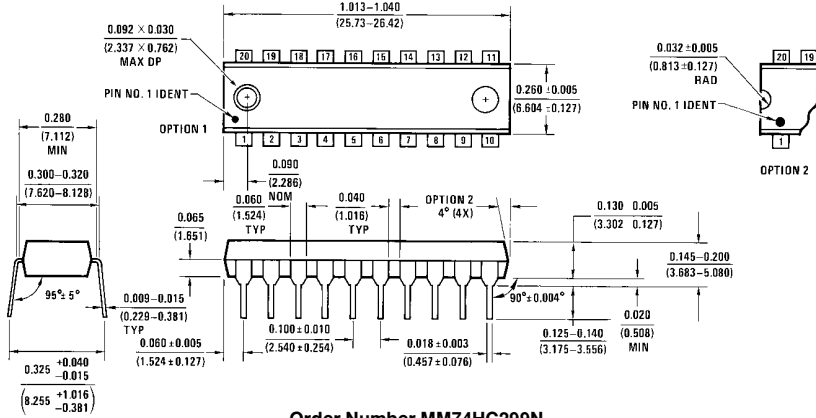
TL/F/5207-2

MM54HC299/MM74HC299 8-Bit TRI-STATE Universal Shift Register

Physical Dimensions inches (millimeters)



Order Number MM54HC299J or MM74HC299J
NS Package J20A



Order Number MM74HC299N
NS Package N20A

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