

## Product Brief

MPC555PB/D  
Rev. 2.1, 12/2002

MPC555 Microcontroller  
Product Brief



This document provides an overview of the MPC555 microcontroller, including a block diagram showing the major modular components and sections that list the major features.

# 1 Features

- MPC555 core with floating-point unit
- 26 Kbytes fast RAM and 6 Kbytes TPU microcode RAM
- 448 Kbytes Flash EEPROM with 5-V programming
- 5-V I/O system
- Serial system: queued serial multi-channel module (QSMCM), dual CAN 2.0B controller modules (TouCAN™)
- 50-channel timer system: dual time processor units (TPU3), modular I/O system (MIOS1)
- 32 analog inputs: dual queued analog-to-digital converters (QADC64)
- Submicron HCMOS (CDR1) technology
- 272-pin plastic ball grid array (PBGA) packaging
- 40-MHz operation, -40 °C to 125 °C with dual supply (3.3 V, 5 V) (-55 °C to 125 °C for the suffix A device)
- 32-Bit architecture (compliant with PowerPC Architecture Book 1)
- Core performance measured at 52.7-Kbyte Dhrystone (v2.1) @ 40 MHz
- Fully static, low power operation
- Integrated double-precision floating-point unit
- Precise exception model
- Extensive system development support
  - On-chip watchpoints and breakpoints
  - Program flow tracking
  - BDM on-chip emulation development interface

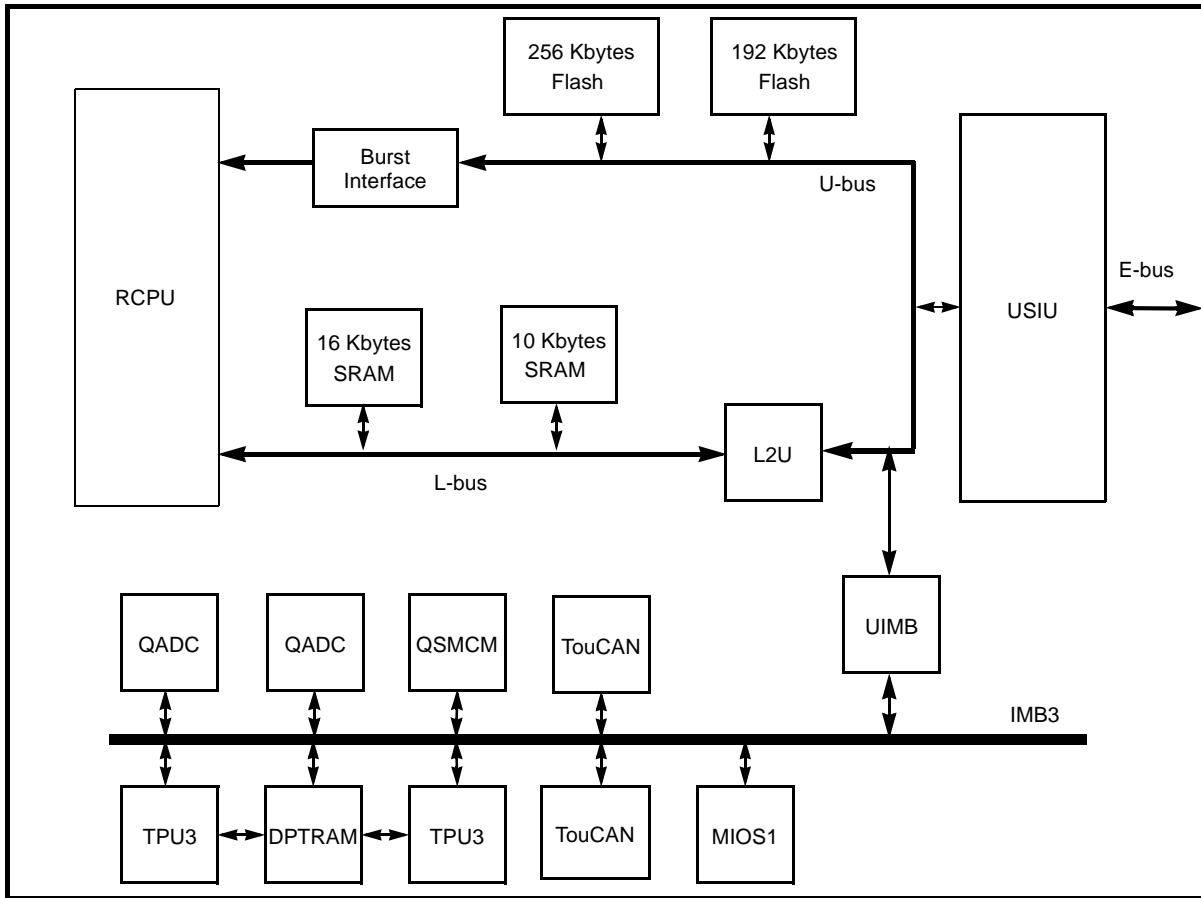


Figure 1. RISC MCU Central Processing Unit (RCPU)

## 2 Four-Bank Memory Controller

- Works with SRAM, EPROM, flash EEPROM, and other peripherals
- Byte write enables
- 32-bit address decodes with bit masks

## 3 U-Bus System Interface Unit (USIU)

- Clock synthesizer
- Power management
- Reset controller
- MPC555 decremter and time base
- Real-time clock register
- Periodic interrupt timer
- Hardware bus monitor and software watchdog timer
- Interrupt controller that supports up to eight external and eight internal interrupts
- IEEE 1149.1 JTAG test access port

- External bus interface
  - 24 address pins, 32 data pins
  - Supports multiple master designs
  - Four-beat transfer bursts, two-clock minimum bus transactions
  - Supports 5V inputs, provides 3.3-V outputs

## 4 Flexible Memory Protection Unit

- Four instruction regions and four data regions
- 4-Kbyte to 16-Mbyte region size support
- Default attributes available in one global entry
- Attribute support for speculative accesses

## 5 448-Kbyte Flash EEPROM Memory

- One 256-Kbyte and one 192-Kbyte module
- Page read mode
- Block (32-Kbyte) erasable
- External 4.75-V to 5.25-V program and erase power supply

## 6 26-Kbytes of Static RAM

- One 16-Kbyte and one 10-Kbyte module
- Fast (one-clock) access
- Keep-alive power
- Soft defect detection (SDD)

## 7 General-Purpose I/O Support

- Address (24) and data (32) pins can be used for general-purpose I/O in single-chip mode
- Nine general-purpose I/O pins in MIOS1 unit
- Many peripheral pins can be used for general-purpose I/O when not used for primary function
- 5-V tolerant inputs/outputs

## 8 Two Time Processor Units (TPU3)

- Each TPU3 module provides these features:
  - A dedicated micro-engine operates independently of the RCPU
  - 16 independent programmable channels and pins
  - Each channel has an event register consisting of a 16-bit capture register, a 16-bit compare register and a 16-bit comparator
  - Nine pre-programmed timer functions are available

- Any channel can perform any time function
- Each timer function can be assigned to more than one channel
- Two timer count registers with programmable prescalers
- Each channel can be synchronized to one or both counters
- Selectable channel priority levels
- 5-V tolerant inputs/outputs
- 6-Kbyte dual port TPU RAM (DPTRAM) is shared by the two TPU3 modules for TPU microcode

## **9 18-Channel Modular I/O System (MIOS1)**

- Ten double action submodules (DASM)
- Eight dedicated PWM sub-modules (PWMSM)
- Two 16-bit modulus counter submodules (MCSM)
- Two parallel port I/O submodules (PIOSM)
- 5-V tolerant inputs/outputs

## **10 Two Queued Analog-to-Digital Converter 2 Modules (QADC64)**

Each QADC provides:

- Up to 16 analog input channels, using internal multiplexing
- Up to 41 total input channels, using internal and external multiplexing
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of 10  $\mu$ s (100,000 samples per second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
  - External edge trigger/level gate
  - Software command
- 64 result registers
- Output data that is right- or left-justified, signed or unsigned
- 5-V reference and range

## **11 Two CAN 2.0B Controller Modules (TouCAN™)**

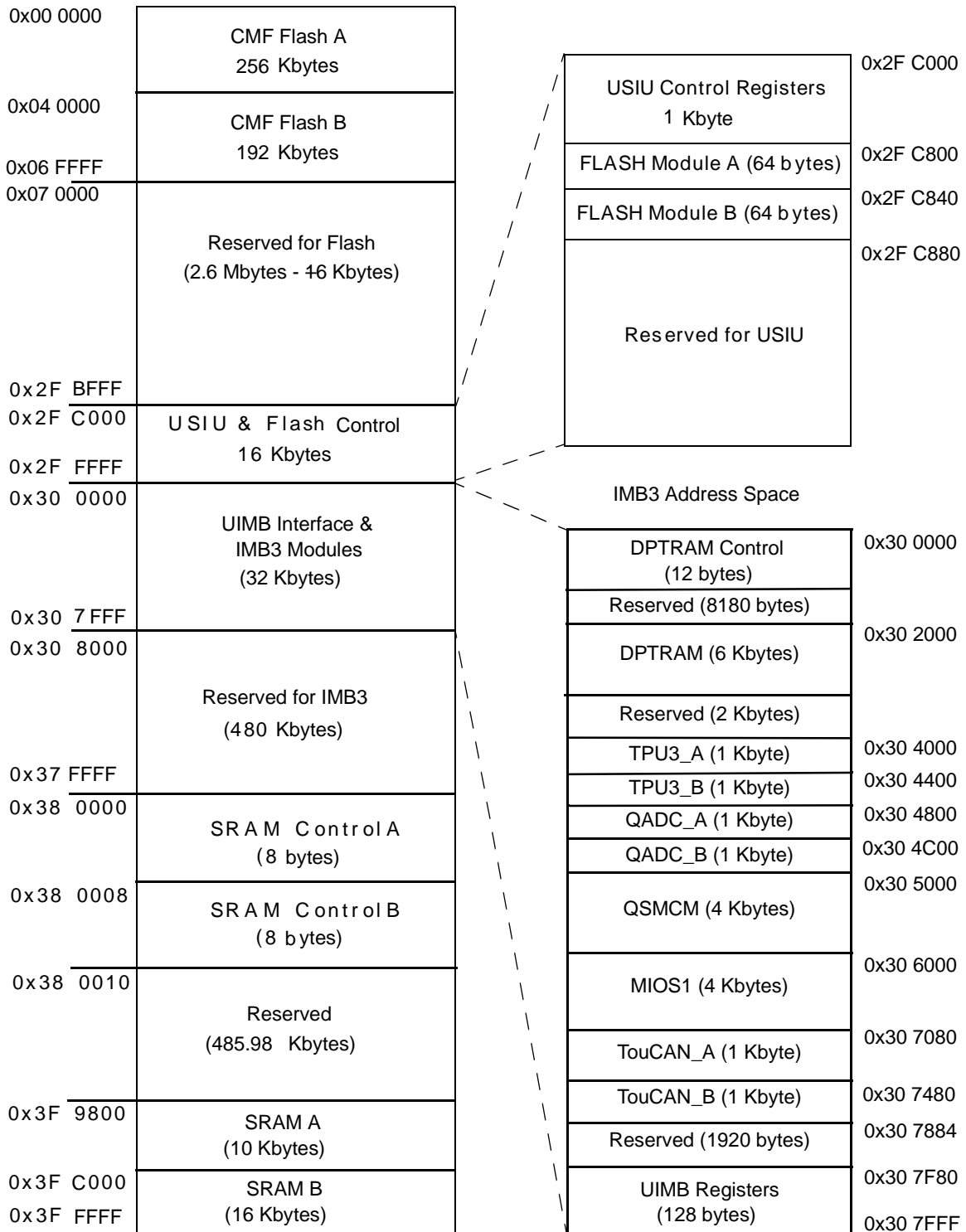
Each TouCAN™ provides these features:

- Full implementation of CAN protocol specification, version 2.0A and 2.0B
- Each module has 16 receive/transmit message buffers of 0 to 8 bytes data length
- Global mask register for message buffers 0 to 13
- Independent mask registers for message buffers 14 and 15
- Programmable transmit-first scheme: lowest ID or lowest buffer number

- 16-bit free-running timer for message time-stamping
- Low power sleep mode with programmable wake-up on bus activity
- Programmable I/O modes
- Maskable interrupts
- Independent of the transmission medium (external transceiver is assumed)
- Open network architecture
- Multimaster concept
- High immunity to EMI
- Short latency time for high-priority messages
- Low power sleep mode with programmable wakeup on bus activity

## 12 Queued Serial Multi-Channel Module (QSMCM)

- Queued serial peripheral interface (QSPI)
  - Provides full-duplex communication port for peripheral expansion or interprocessor communication
  - Up to 32 preprogrammed transfers, reducing overhead
  - 160-byte queue buffer
  - Programmable transfer length: from 8 to 16 bits, inclusive
  - Synchronous interface with baud rate of up to system clock divided by 4
  - Four programmable peripheral-select pins support up to 16 devices
  - Wrap-around mode allows continuous sampling for efficient interfacing to serial peripherals (e.g., – serial A/D converters, I/O latches, etc.)
- Two serial communications interfaces (SCI). Each SCI offers these features:
  - UART mode provides NRZ format and half-or full-duplex interface
  - 16 register receive buffer and 16 register transmit buffer (SCI1 only)
  - Advanced error detection and optional parity generation and detection
  - Word length programmable as 8 or 9 bits
  - Separate transmitter and receiver enable bits and double buffering of data
  - Wakeup functions allow the CPU to run uninterrupted until either a true idle line is detected or a new address byte is received
  - External source clock for baud generation
  - Multiplexing of transmit data pins with discrete outputs and receive data pins with discrete inputs, allowing realization of a low-speed serial protocol



**Figure 2. MPC555 Internal Memory Map**



## 13 Ordering Information

**Table 1. MPC555 Package Information**

Device Name	Order Part Number	Package Info	Temp. Range
MPC555	MPC555LFMZP40	272 PBGA	-40 to +125 °C
MPC555	MPC555LFCZP40	272 PBGA	-40 to +85 °C
MPC555	MPC555AZP40	272 PBGA	-55 to +125 °C
MPC555	MPC555LFMZP40R2	272 PBGA Shipped in tape and reel media	-40 to +125 °C
MPC555	MPC555LFCZP40R2	272 PBGA Shipped in tape and reel media	-40 to +85 °C

Table 2 lists the documents that provide a complete description of the MPC555 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola Semiconductor documentation page on the Internet (the source for the latest information).

**Table 2. Available Documentation**

Document Number	Title
MPC555UM/AD	MPC555/556 User's Manual
AN1282/D	Board Strategies for Ensuring Optimum Frequency Synthesizer Performance.
AN1778/D	Using the MIOS on the MPC555 Evaluation Board
AN1821/D	Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family
AN1837/D	Non-Volatile Memory Technology Overview
AN2001/D	Designing Expansion Boards for the Motorola EVB555/ETAS ES200.
AN2109/D	MPC555 Interrupts.
AN2127/D	EMC Guidelines for MPC500-Based Automotive Powertrain Systems

## 14 Revision History

**Table 3. Revision History**

Rev. No.	Substantive Changes	Date of Release
2	Existing Document.	September 2001
2.1	Added temperature range for suffix A device.	11 December 2002



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