MSM6242B

DIRECT BUS CONNECTED CMOS REAL TIME CLOCK/CALENDAR

DESCRIPTION

The MSM6242B is a silicon gate CMOS Real Time Clock/Calendar for use in direct bus-connection Microprocessor/Microcomputer applications. An on-chip 32.768 kHz crystal oscillator time base is divided to provide addressable 4-bit I/O data for SECONDS, MINUTES, HOURS, DAY OF WEEK, DATE, MONTH and YEAR. Data access is controlled by 4-bit address, chip selects ($\overline{CS0}$, CS1), $\overline{WRITE}$, $\overline{READ}$, and ALE. Control Registers D, E and F provide for 30 SECOND error adjustment, INTERRUPT REQUEST (IRQ FLAG) and BUSY status bits, clock STOP, HOLD, and RESET FLAG bits, 4 selectable INTERRUPTS rates are available at the STD.P (STANDARD PULSE) output utilizing Control Register inputs T0, T1 and the ITRPT/STND (INTERRUPT/STANDARD). Masking of the interrupt output (STD.P) can be accomplished via the MASK bit. The MSM6242B can operate in a 12/24 hour format and Leap Year timing is automatic.

The MSM6242B normally operates from a 5 V ±10% supply at –40 to +85°C. Battery backup operation down to 2.0 V allows continuation of time keeping when main power is off. The MSM6242B is offered in a 18-pin plastic DIP and a 24-pin plastic Small Outline package.

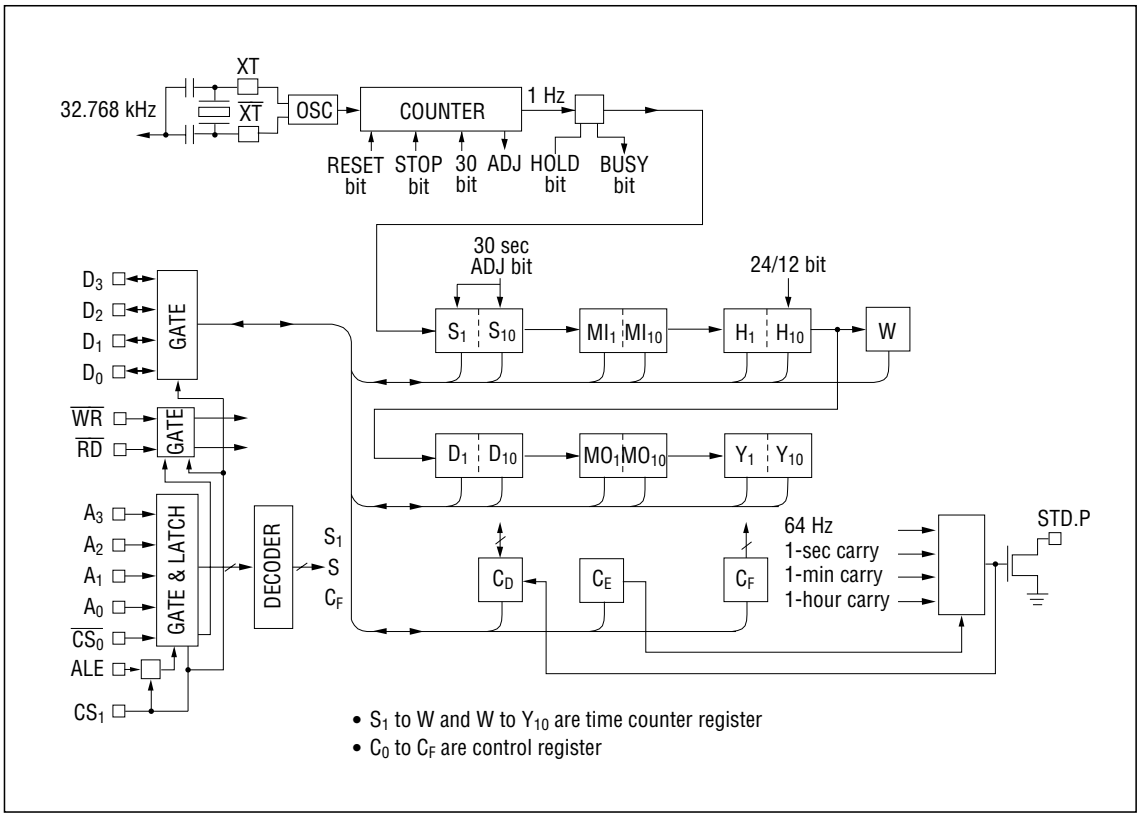
FEATURES

DIRECT MICROPROCESSOR/MICROCONTROLLER BUS CONNECTION

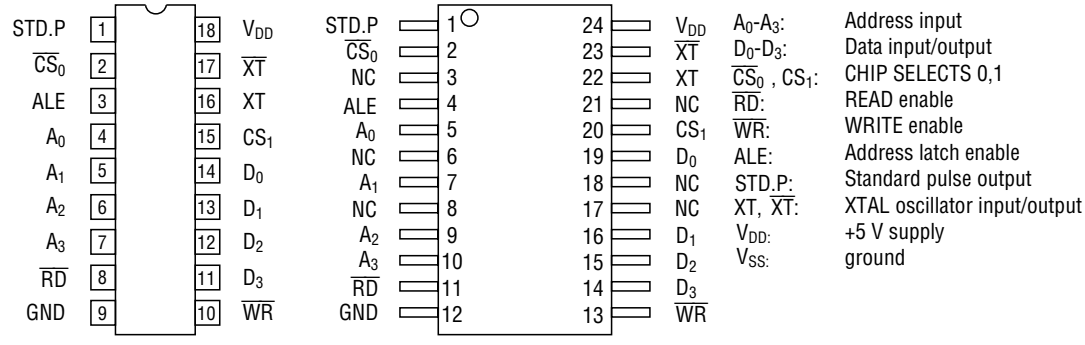
TIME	MONTH	DATE	YEAR	DAY OF WEEK
23:59:59	12	31	80	7

- 4-bit data bus
- 4-bit address bus
- $\overline{READ}$, $\overline{WRITE}$, ALE and CHIP SELECT INPUTS
- Status registers – IRQ and BUSY
- Selectable interrupt outputs – 1/64 second, 1 second, 1 minute, 1 hour
- Interrupt masking
- 32.768 kHz crystal controlled operation
- 12/24 hour format
- Auto leap year
- ±30 second error correction
- Single 5 V supply
- Battery backup down to V_{DD} = 2.0 V
- Low power dissipation:
  20 µW max at V_{DD} = 2 V
  150 µW max at V_{DD} = 5 V
- Package: 18-pin plastic DIP (DIP18-P-300-2.54) (MSM6242BRS)
  24-pin plastic SOP (SOP24-P-430-1.27-K) (MSM6242BGS-K)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



REGISTER TABLE

Address Input	Address Input				Register Name	Data				Count Value	Description
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0		
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	0 to 9	1-second digit register
1	0	0	0	1	S_{10}	*	S_{40}	S_{20}	S_{10}	0 to 5	10-second digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 to 9	1-minute digit register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 to 5	10-minute digit register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	0 to 9	1-hour digit register
5	0	1	0	1	H_{10}	*	PM/ AM	h_{20}	h_{10}	0 to 2 or 0 to 1	PM/AM, 10-hour digit register
6	0	1	1	0	D_1	d_8	d_4	d_2	d_1	0 to 9	1-day digit register
7	0	1	1	1	D_{10}	*	*	d_{20}	d_{10}	0 to 3	10-day digit register
8	1	0	0	0	MO_1	mo_8	mo_4	mo_2	mo_1	0 to 9	1-month digit register
9	1	0	0	1	MO_{10}	*	*	*	MO_{10}	0 to 1	10-month digit register
A	1	0	1	0	Y_1	y_8	y_4	y_2	y_1	0 to 9	1-year digit register
B	1	0	1	1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 to 9	10-year digit register
C	1	1	0	0	W	*	w_4	w_2	w_1	0 to 6	Week register
D	1	1	0	1	C_D	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	—	Control Register D
E	1	1	1	0	C_E	t_1	t_0	ITRPT/ STND	MASK	—	Control Register E
F	1	1	1	1	C_F	TEST	24/12	STOP	REST	—	Control Register F

REST = RESET
ITRPT/STND = INTERRUPT/STANDARD

Note 1) — Bit * does not exist (unrecognized during a write and held at "0" during a read).
Note 2) — Be sure to mask the AM/PM bit when processing 10's of hour's data.
Note 3) — BUSY bit is read only. The IRQ FLAG bit can only be set to a "0". Setting the IRQ FLAG to a "1" is done by hardware.
Note 4) — PM at 1 and AM at 0 for PM/AM bit.

Figure 1 Register Table

OSCILLATOR FREQUENCY DEVIATIONS

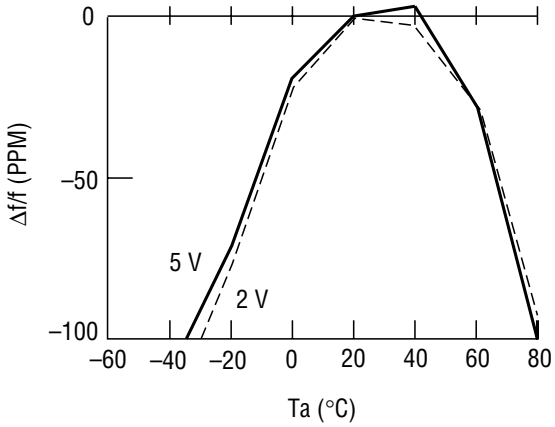


Figure 2 Frequency Deviation (PPM) vs Temperature

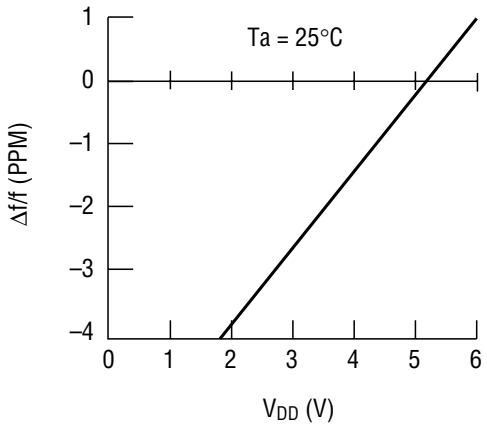
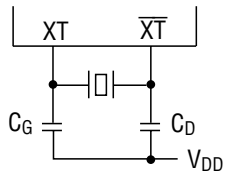


Figure 3 Frequency Deviation (PPM) vs Voltage

Note: 1. The graghs above showing frequency deviation vs temperature/voltage are primarily characteristic of the MSM6242B with the oscillation circuit described below.



Crystal: Type N_0, P_3 by kinseki (32.768 kHz)

C_G, C_D: 22 pF (Temperature Characteristics: 0)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7	V
Input Voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output Voltage	V_O		–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	4 to 6	V
Standby Supply Voltage	V_{BAK}	—	2 to 6	
Crystal Frequency	$f_{(XT)}$	—	32.768	kHz
Operating Temperature	T_{OP}	—	–40 to +85	°C

DC Characteristics

(V_{DD} = 5 V ±10%, Ta = –40 to +85)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable Terminal
"H" Input Voltage	$V_{IH}1$	—		2.2	—	—	V	All input terminals except CS_1, XT
"L" Input Voltage	$V_{IL}1$	—		—	—	0.8		
Input Leak Current	$I_{LK}1$	$V_I = V_{DD}/0$ V		—	—	1/–1	µA	Input terminals other than D_0 to D_3, XT
Input Leak Current	$I_{LK}2$			—	—	10/–10		D_0 to D_3
"L" Output Voltage	$V_{OL}1$	I_{OL} = 2.5 mA		—	—	0.4	V	D_0 to D_3
"H" Output Voltage	V_{OH}	I_{OH} = –400 µA		2.4	—	—		
"L" Output Voltage	$V_{OL}2$	I_{OL} = 2.5 mA		—	—	0.4	V	STD.P
OFF Leak Current	I_{OFFLK}	V = $V_{DD}/0$ V		—	—	10	µA	
Input Capacitance	C_I	Input frequency 1 MHz		—	5	—	pF	All input terminals
Current Consumption	$I_{DD}1$	$f_{(xt)}$ = 32.768 kHz $CS_1 \approx 0$	V_{DD} = 5 V	—	—	30	µA	V_{DD}
Current Consumption	$I_{DD}2$		V_{DD} = 2 V	—	—	10		
"H" Input Voltage	$V_{IH}2$	V_{DD} = 2 to 5.5 V		4/5V_{DD}	—	—	V	CS_1
"L" Input Voltage	$V_{IL}2$			—	—	1/5V_{DD}		

SWITCHING CHARACTERISTICS

(1) WRITE mode (ALE = V_{DD})

(V_{DD} = 5 V ±10% Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
CS_1 Hold Time	t_{C1H}	—	1000	—	
Address Stable before WRITE	t_{AW}	—	20	—	
Address Stable after WRITE	t_{WA}	—	10	—	
WRITE Pulse Width	t_{WW}	—	120	—	
Data Set up Time	t_{DS}	—	100	—	
Data Hold Time	t_{DH}	—	10	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	

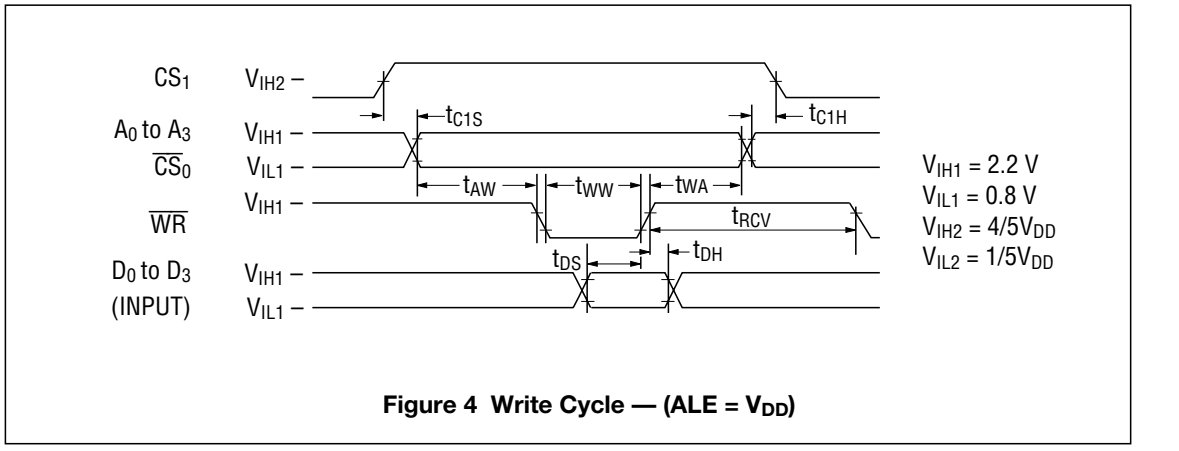


Figure 4 Write Cycle — (ALE = V_{DD})

(2) WRITE mode (With use of ALE)

(V_{DD} = 5 V ±10%, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
Address Set up Time	t_{AS}	—	25	—	
Address Hold Time	t_{AH}	—	25	—	
ALE Pulse Width	t_{AW}	—	40	—	
ALE before WRITE	t_{ALW}	—	10	—	
WRITE Pulse Width	t_{WW}	—	120	—	
ALE after WRITE	t_{WAL}	—	20	—	
Data Set up Time	t_{DS}	—	100	—	
Data Hold Time	t_{DH}	—	10	—	
CS_1 Hold Time	t_{C1H}	—	1000	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	

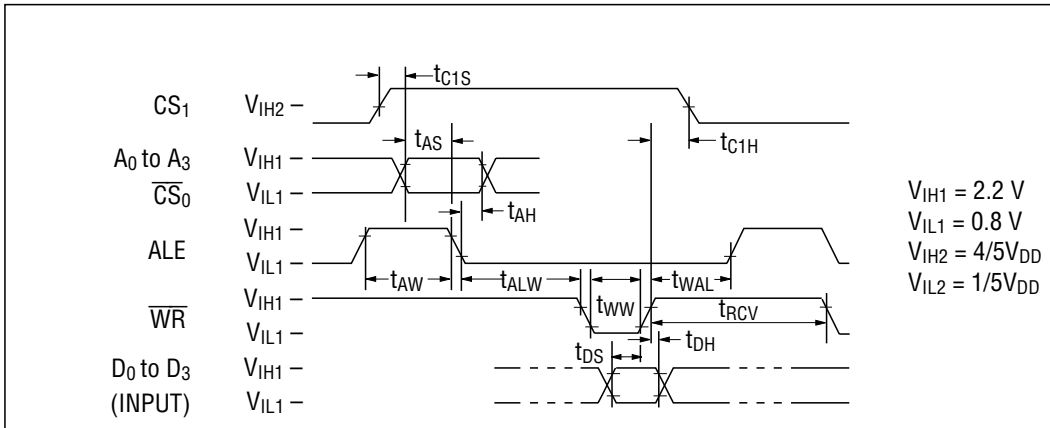


Figure 5 Write Cycle — (With Use of ALE)

(3) READ mode (ALE = V_{DD})

(V_{DD} = 5 V ±10%, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
CS_1 Hold Time	t_{C1H}	—	1000	—	
Address Stable before READ	t_{AR}	—	20	—	
Address Stable after READ	t_{RA}	—	0	—	
$\overline{RD}$ to Data	t_{RD}	C_L = 150 pF	—	120	
Data Hold	t_{DR}	—	0	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	

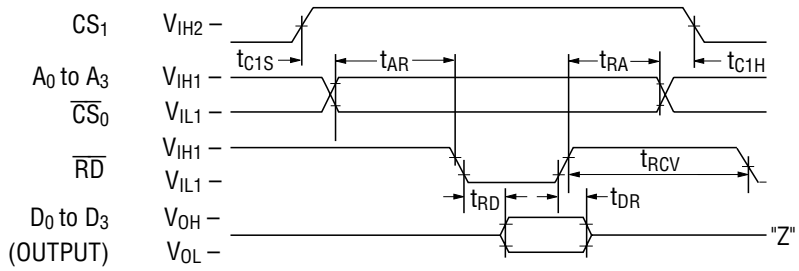


Figure 6 Read Cycle — (ALE = V_{DD})

(4) READ mode (With use of ALE)

(V_{DD} = 5 V ±10%, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
Address Set up Time	t_{AS}	—	25	—	
Address Hold Time	t_{AH}	—	25	—	
ALE Pulse Width	t_{AW}	—	40	—	
ALE before READ	t_{ALR}	—	10	—	
ALE after READ	t_{RAL}	—	10	—	
$\overline{RD}$ to Data	t_{RD}	C_L = 150 pF	—	120	
Data Hold	t_{DR}	—	0	—	
CS_1 Hold Time	t_{C1H}	—	1000	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	

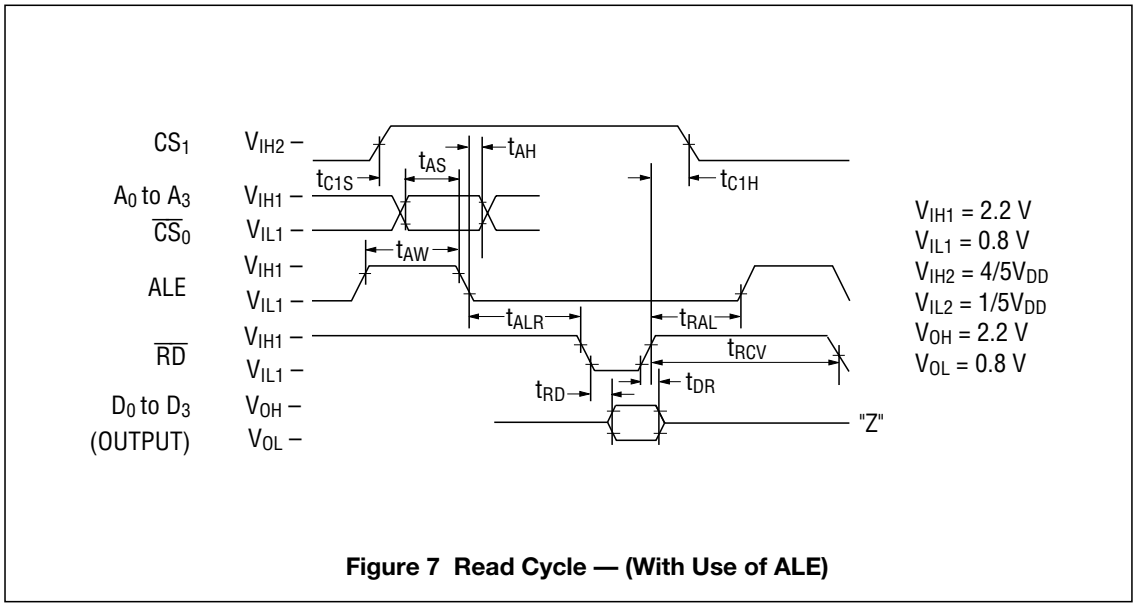
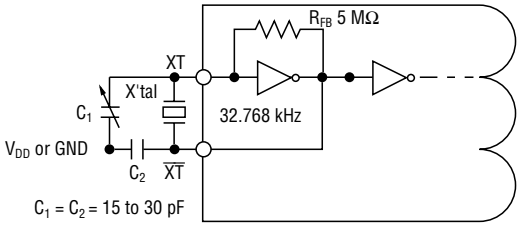


Figure 7 Read Cycle — (With Use of ALE)

PIN DESCRIPTION

Name	Pin No.		Description
	RS	GS-K	
D_0	14	19	Data Input/Output pins to be directly connected to a microcontroller bus for reading and writing of the clock/calendar's registers and control registers. D0 = LSB and D3 = MSB.
D_1	13	16	
D_2	12	15	
D_3	11	14	
A_0	4	5	Address input pin for use by a microcomputer to select internal clock/calendar's registers and control registers for Read/Write operations (See Function Table Figure 1). Address input pins A0-A3 are used in combination with ALE for addressing registers.
A_1	5	7	
A_2	6	9	
A_3	7	10	
ALE	3	4	Address Latch Enable pin. This pin enables writing of address data when ALE = 1 and $\overline{CS_0}$ = 0; address data is latched when ALE = 0 Microcontroller/Microprocessors having an ALE output should connect to this pin; otherwise it should be connected at V_{DD}
$\overline{WR}$	10	13	Writing of data is performed by this pin. When CS_1 = 1 and $\overline{CS_0}$ = 0, D_0 to D_3 data is written into the register at the rising edge of $\overline{WR}$.
$\overline{RD}$	8	11	Reading of register data is accomplished using this pin. When CS_1 = 1, $\overline{CS_0}$ = 0 and $\overline{RD}$ = 0, the data of this register is output to D_0 to D_3. If both $\overline{RD}$ and $\overline{WR}$ are set at 0 simaltaneously, $\overline{RD}$ is to be inhibited.
$\overline{CS_0}$	2	2	Chip Select pins. These pins enable/disable ALE, $\overline{RD}$ and $\overline{WR}$ operation. $\overline{CS_0}$ and ALE work in combination with one another, while CS_1 work independent with ALE. CS_1 must be connected to power failure detection as shown in Figure 18.
CS_1	15	20	
STD.P	1	1	Output pin of N-CH OPEN DRAIN type. The output data is controlled by the D_1 data content of C_E register. This pin has a priority to $\overline{CS_0}$ and CS_1. Refer to Figure 9 and FUNCTIONAL DESCRIPTION OF REGISTERS.
XT	16	22	32.768 kHz crystal is to be connected to these pins. When an external clock of 32.768 kHz is to be used for MSM6242B's oscillation source, either CMOS output or pull-up TTL output is to be input from XT, while $\overline{XT}$ should be left open.
$\overline{XT}$	17	23	
V_{DD}	18	24	Power supply pin. +2 to +6 V power is to be applied to this pin.
GND	9	12	Ground pin.



The impedance of the crystal should be less than 30 kΩ

Figure 8 Oscillator Circuit

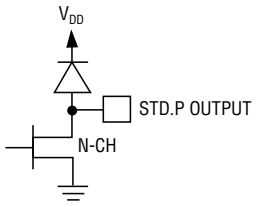


Figure 9

FUNCTIONAL DESCRIPTION OF REGISTERS

S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, MO_1, MO_{10}, Y_1, Y_{10}, W

a) These are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. These values are in BCD notation.

b) All registers are logically positive. For example, (S8, S4, S2, S1) = 1001 which means 9 seconds.

c) If data is written which is out of the clock register data limits, it can result in erroneous clock data being read back.

d) PM/AM, h_{20}, h_{10}
In the mode setting of 24-hour mode, PM/AM bit is ignored, while in the setting of 12-hour mode h_{20} is to be set. Otherwise it causes a discrepancy. In reading out the PM/AM bit in the 24-hour mode, it is continuously read out as 0. In reading out h_{20} bit in the 12-hour mode, 0 is written into this bit first, then it is continuously read out as 0 unless 1 is being written into this bit.

e) Registers Y1, Y10, and Leap Year. The MSM6242B is designed exclusively for the Christian Era and is capable of identifying a leap year automatically. The result of the setting of a non-existant day of the month is shown in the following example: If the date February 29 or November 31, 1985, was written, it would be changed automatically to March 1, or December 1, 1985 at the exact time at which a carry pulse occurs for the day's digit.

f) The Register W data limits are 0 – 6 (Tabel 1 shows a possible data definition).

Table 1

W_4	W_2	W_1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

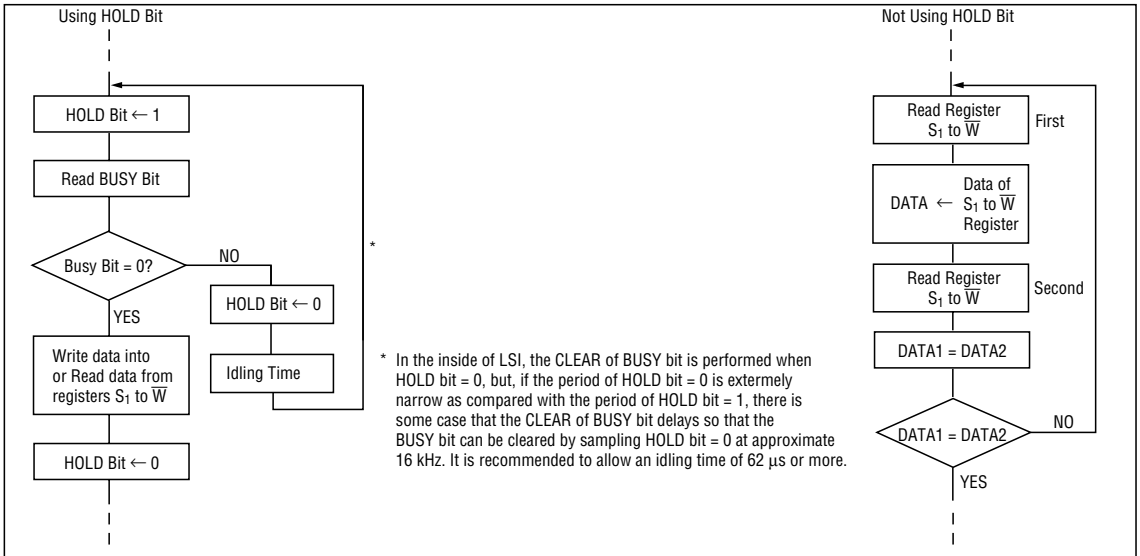
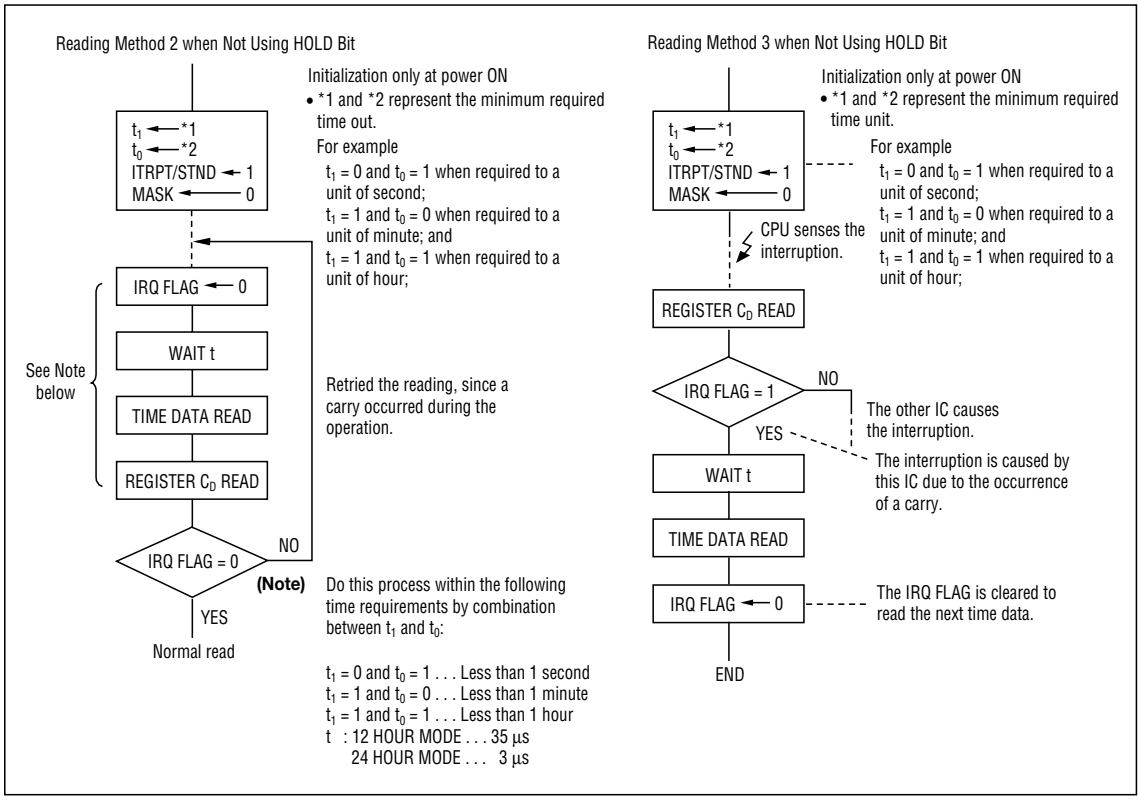


Figure 10 Reading and Writing of Registers S_1 to $\overline{W}$



CD REGISTER (Control D Register)

a) HOLD (D0) – Setting this bit to a "1" inhibits the 1Hz clock to the S1 counter, at which time the Busy status bit can be read. When Busy = 0, register's S_1 to $\overline{W}$ can be read or written. During this procedure if a carry occurs the S1 counter will be incremented by 1 second after HOLD = 0 (this condition is guaranteed as long as HOLD = 1 does not exceed 1 second in duration). If CS1 = 0 then HOLD = 0 irrespective of any condition.

b) BUSY (D1) – Status bit which shows the interface condition with microcontroller/microprocessors. As for the method of writing into and reading from S_1 to $\overline{W}$ (address ϕ to C), refer to the flow chart described in Figure 10.

c) IRQ FLAG (D2) – This status bit corresponds to the output level of the STD.P output. When STD.P = 0, then IRQ = 1; when STD.P = 1, then IRQ = 0. The IRQ FLAG indicates that an interrupt has occurred to the microcomputer if IRQ = 1. When D0 of register C_E (MASK) = 0, then the STD.P output changes according to the timing set by D3 (t_1) and D2 (t_0) of register E. When D1 of register E (ITRPT/STND) = 1 (interrupt mode), the STD.P output remains low until the IRQ FLAG is written to a "0". When IRQ = 1 and timing for a new interrupt occurs, the new interrupt is ignored. When ITRPT/STND = 0 (Standard Pulse Output mode) the STD.P output remains low until either "0" is written to the IRQ FLAG; otherwise, the IRQ FLAG automatically goes to "0" after 7.8125 ms. When writing the HOLD or 30 second adjust bits of register D, it is necessary to write the IRQ FLAG bit to a "1".

d) ±30 ADJ (D3) – When 30-second adjustment is necessary, a "1" is written to bit D3 during which time the internal clock registers should not be read from or written to 125 µs after bit D3 = 1 it will automatically return to a "0", and at that time reading or writing of registers can occur.

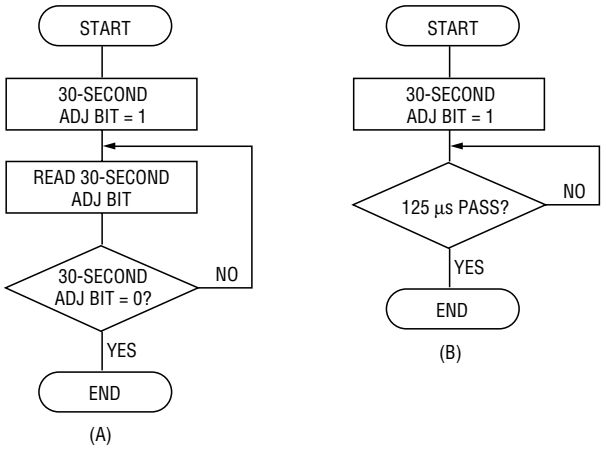


Figure 11 Writing 30-Second Adj. bit (Two Ways A, B)

CE REGISTER (Control E Register)

a) MASK (D0) – This bit controls the STD.P output. When MASK = 1, then STD.P = 1 (open); when MASK = 0, then STD.P = output mode. The relationship between the MASK bit and STD.P output is shown Figure 12.

b) ITRPT/STND (D1) – The ITRPT/STND input is used to switch the STD.P output between its two modes of operation, interrupt and Standard timing waveforms. When ITRPT/STND = 0 a fixed cycle waveform with a low-level pulse width of 7.8125 ms is present at the STD.P output. At this time the MASK bit must equal 0, while the period in either mode is determined by T0 (D2) and T1 (D3) of Register E.

c) T0 (D2), T1 (D3) – These two bits determine the period of the STD.P output in both interrupt and Fixed timing waveform modes. The tables below show the timing associated with the T0, T1 inputs as well as their relationship to INTRPT/STND and STD.P.

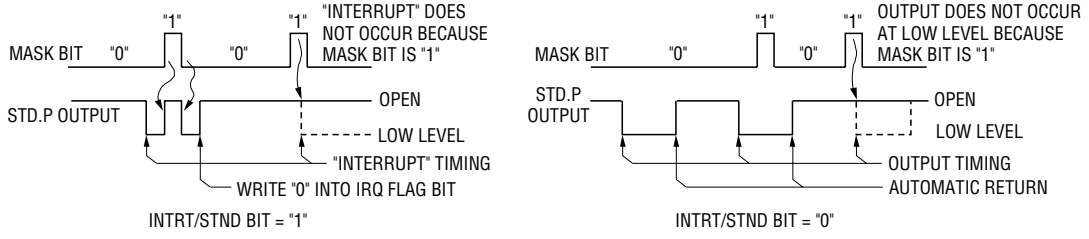
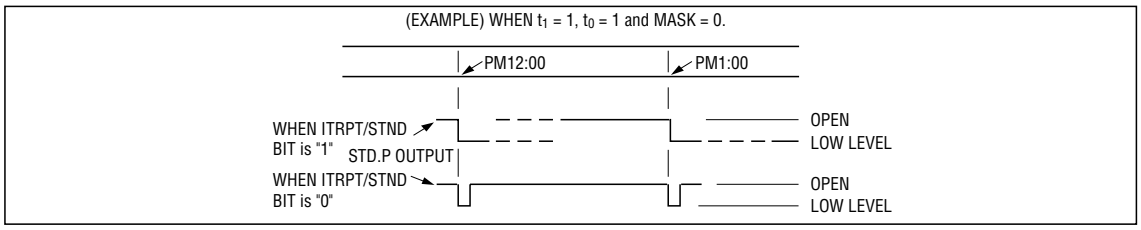


Figure 12

Table 2

t_1	t_0	Period	Duty CYCLE of "0" level when ITRPT/STND bit is "0".
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

The timing of the STD.P output designated by T1 and T0 occurs the moment that a carry occurs to a clock digit.



d) The low-level pulse width of the fixed cycle waveform (ITRPT/STND = 0) is 7.8125 ms independent of T0/T1 inputs.

e) The fixed cycle waveform mode can be used for adjustment of the oscillator frequency time base. (See Figure 14).

f) During ±30 second adjustment a carry can occur that will cause the STD.P output to go low when T0/T1 = 1, 0 or 1, 1. However, when T1/T0 = 0, 0 and ITRPT/STND = 0, carry does not occur and the STD.P output resumes normal operation.

g) The STD.P output is held (frozen) at the point at which STOP = 1 while ITRPT/STND = 0.

h) No STD.P output change occurs as a result of writing data to registers S1 to H1.

C_F REGISTER (Control F Register)

a) REST (D0) – "RESET" This bit is used to clear the clock's internal divider/counter of less than a second. When REST = 1, the counter is Reset for the duration of REST. In order to release this counter from Reset, a "0" must be written to the REST bit. If CSI = 0 then REST = 0 automatically.

b) STOP (D1) – The STOP FLAG Only inhibits carries into the 8192 Hz divider stage. There may be up to 122 µs delay before timing starts or stops after changing this flag; 1 = STOP/0 = RUN.

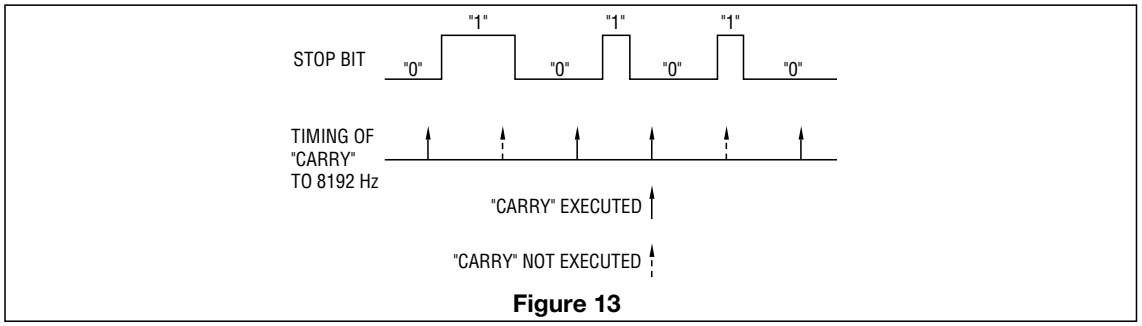


Figure 13

c) 24/12 (D2) – "24/HOUR/12 HOUR" This bit is for selection of 24/12 hour time modes. If D2 = 1–24 hour mode is selected and the PM/AM bit is invalid. If D2 = 0–12 hour mode is selected and the PM/AM bit is valid.

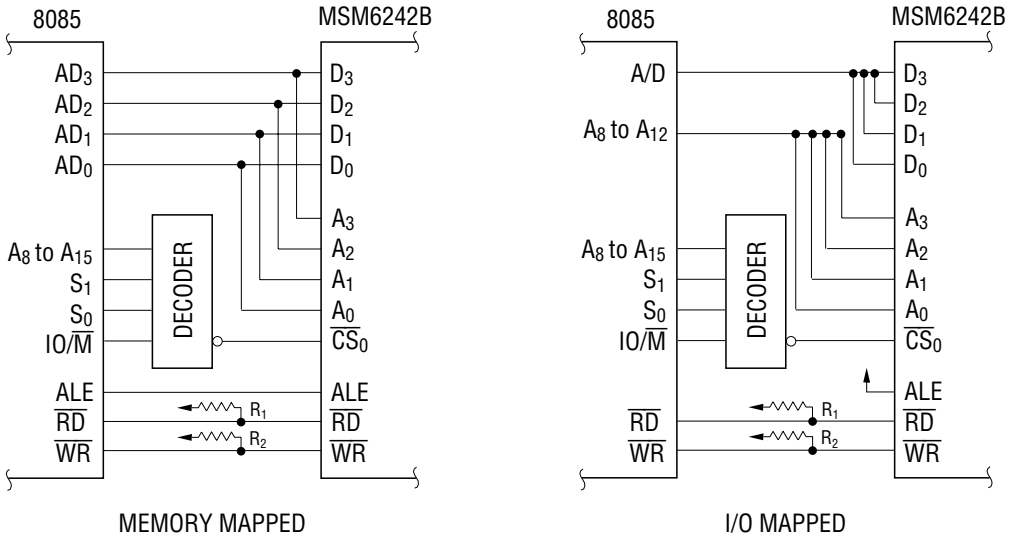
Setting of the 24/12 hour bit is as follows:

1) REST bit = 1
2) 24/12 hour bit = 0 or 1
3) REST bit = 0

* REST bit must = 1 to write to the 24/12 hour bit.

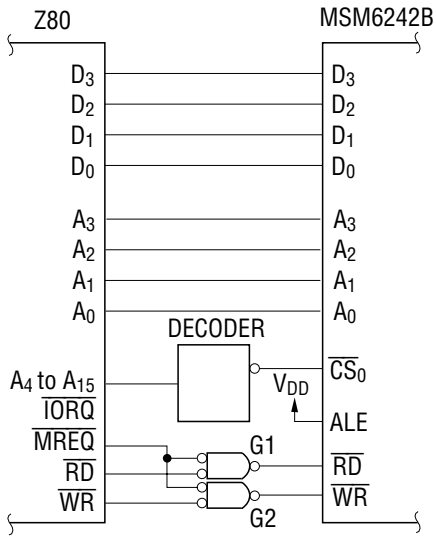
d) TEST (D3) – When the TEST flag is a "1", the input to the SECONDS counter comes from the counter/divider stage instead of the 15th divider stage. This makes the SECONDS counter count at 5.4163 kHz instead of 1 Hz. When TEST = 1 (Test Mode) the STOP & REST (Reset) flags do not inhibit internal counting. When Hold = 1 during Test (Test = 1) internal counting is inhibited; however, when the HOLD FLAG goes inactive (Hold = 0) counter updating is not guaranteed.

TYPICAL APPLICATION INTERFACE WITH MSM6242B AND MICROCONTROLLERS



Note : If 8085 does not enter into the state of HALT or HOLD during CS_1 = "H" of MSM6242B, R_1 and R_2 are not required.

Figure 15



Note : It depends upon the switching characterisrics decided by a X'tal used for a Z80 that either of $\overline{IORQ}$ and $\overline{MREQ}$ is used.

Figure 16

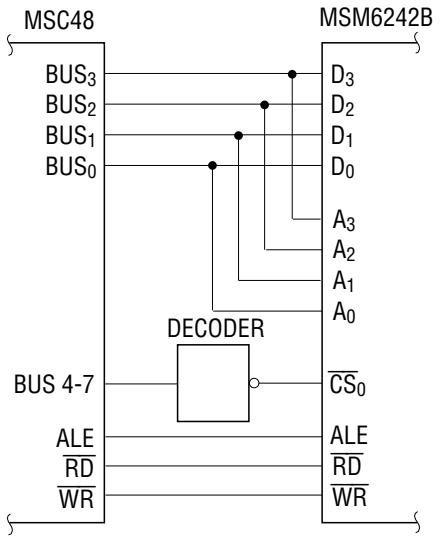


Figure 17

TYPICAL APPLICATIONS — INTERFACE WITH MSM80C49

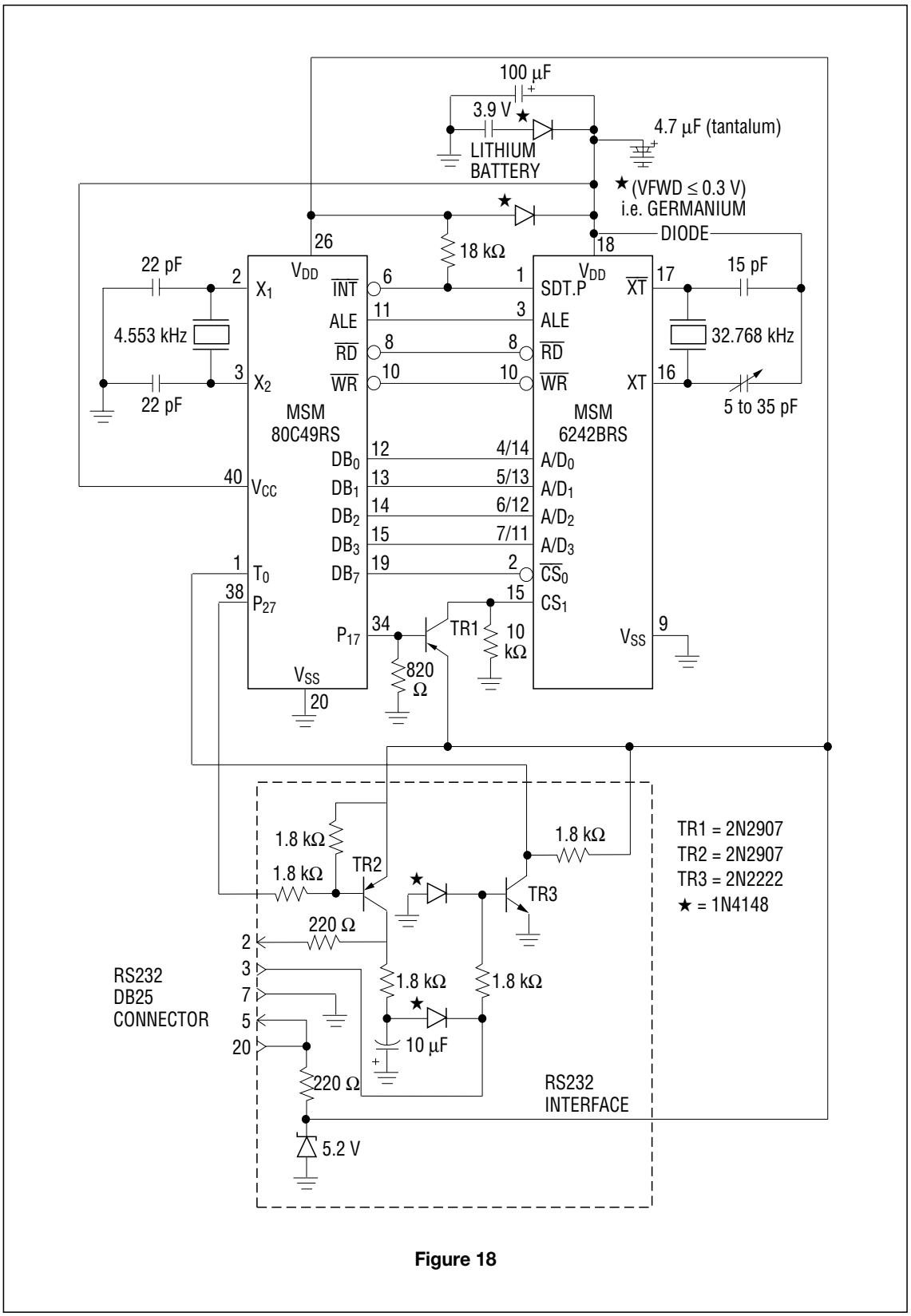
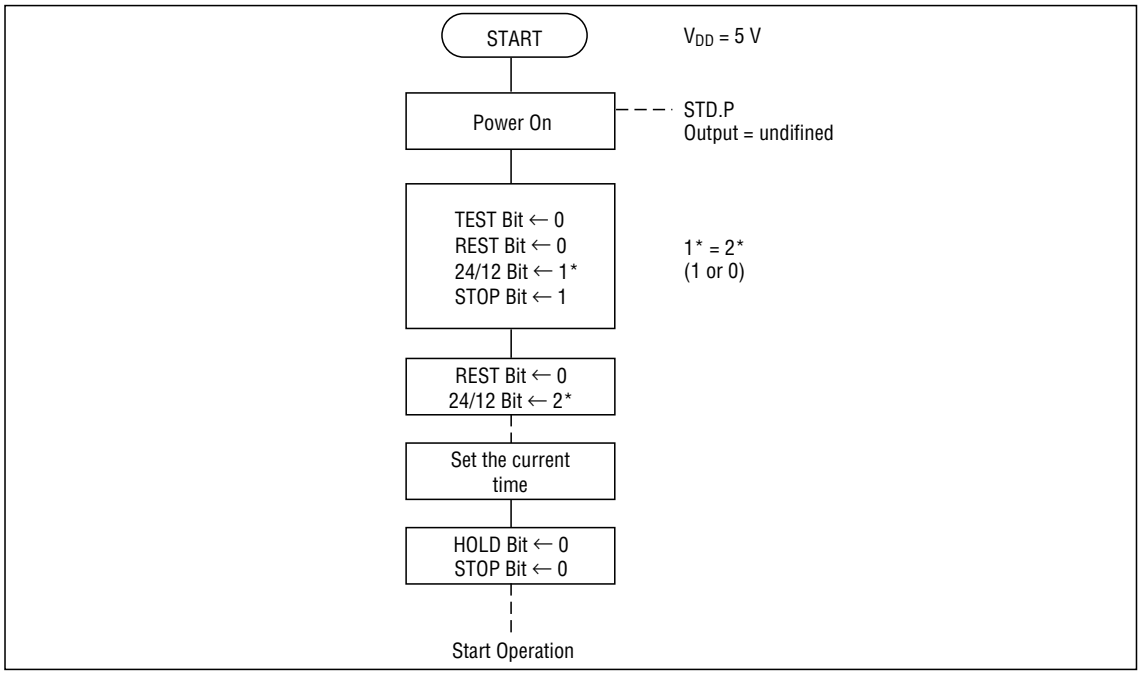


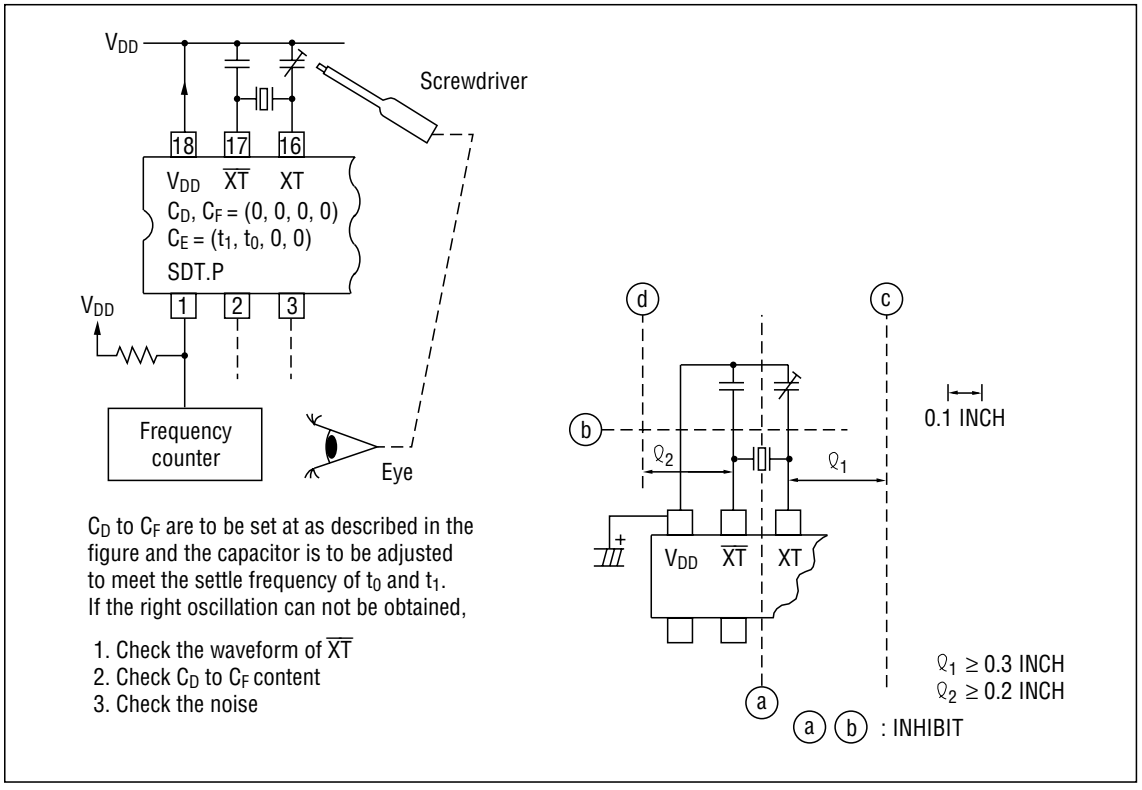
Figure 18

APPLICATION NOTE

1. Power Supply



2. Adjustment of Frequency



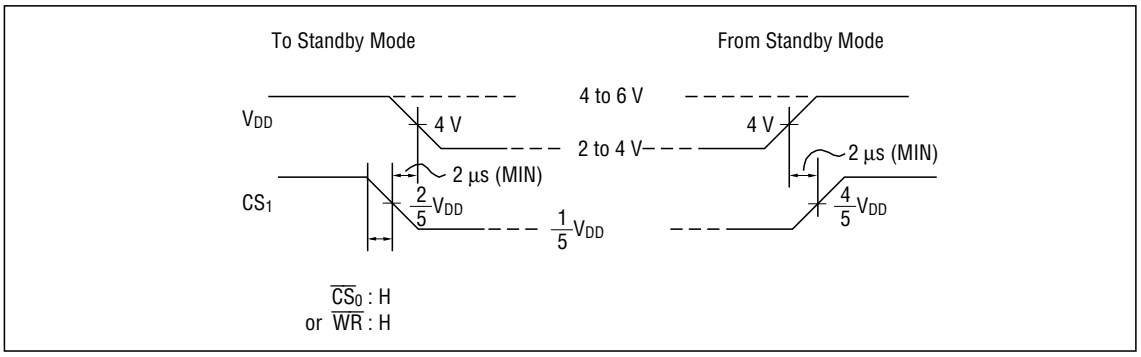
3. CH_1 (Chip Select)

V_{IH} and V_{IL} of CH_1 has 3 functions.

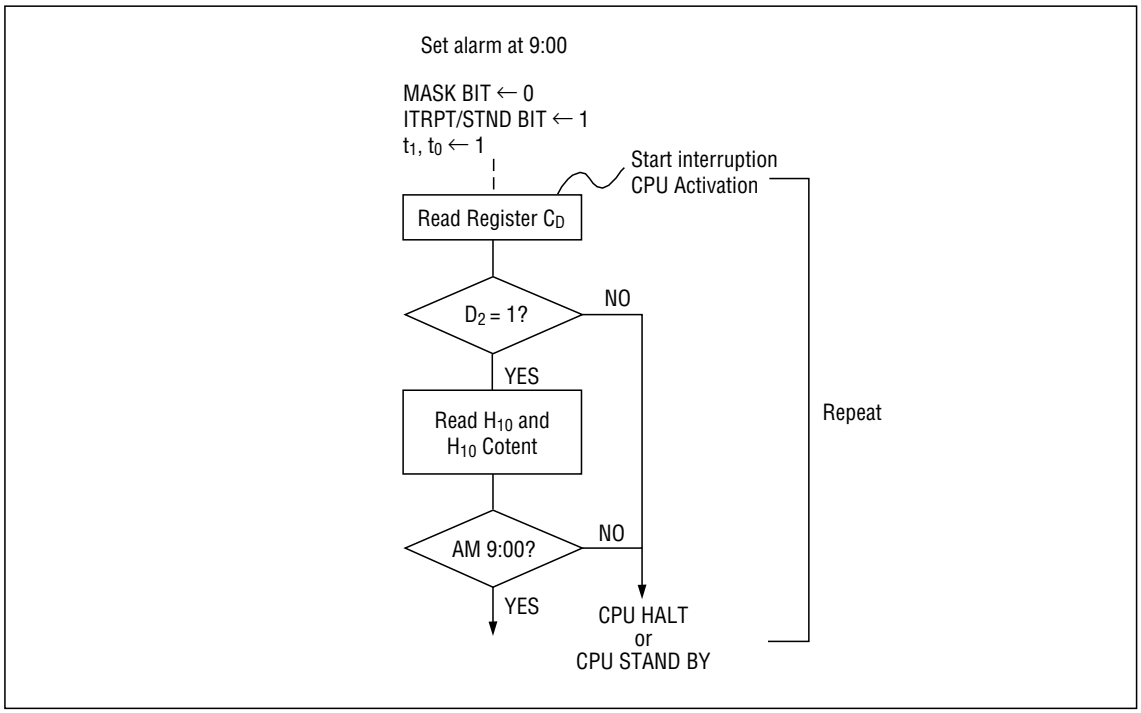
a) To accomplish the interface with a microcontroller/microprocessor.
b) To inhibit the control bus, data bus and address bus and to reduce input gate pass current in the stand-by mode.
c) To protect internal data when the mode is moved to and from standby mode.

To realize the above functions:

a) More than 4/5 V_{DD} shoud be applied to the MSM6242B for the interface with a microcontroller/microprocessor in 5 V operation.
b) In moving to the standby mode, 1/5 V_{DD} should be applied so that all data buses should be disabled. In the standby mode, approx. 0 V should be applied.
c) To and from the standby mode, obey following Timing chart.



4. Set SDT.P at Alarm Mode



TYPICAL APPLICATION — POWER SUPPLY CIRCUIT

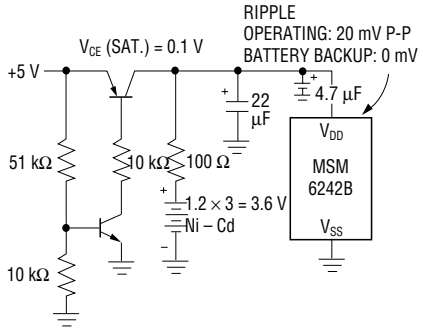


Figure 19

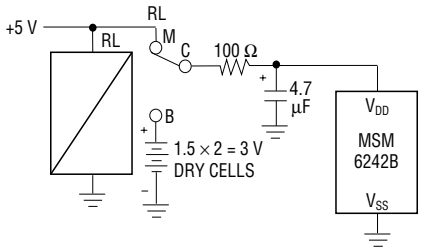


Figure 20

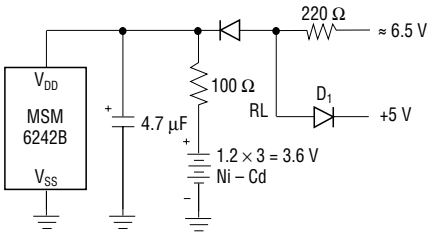


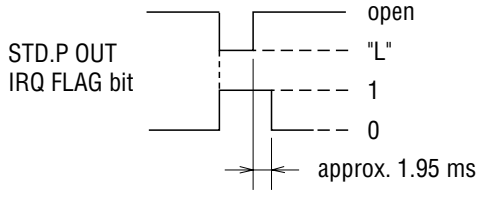
Figure 21

4.7 µF: tantalum

SUPPLEMENTARY DESCRIPTION

- When "0" is written to the IRQ FLAG bit, the IRQ FLAG bit is cleared. However, if "0" is assigned to the IRQ FLAG bit when written to the other bits, the 30-sec ADJ bit and the HOLD bit, the IRQ FLAG = 1 and was generated before the writing and IRQ FLG = 1 generated in a moment then will be cleared. To avoid this, always set "1" to the IRQ FLAG unless "0" is written to it intentionally. By writing "1" to it, the IRQ FLAG bit does not become "1".
- Since the IRQ FLAG bit becomes "1" in some cases when rewriting either of the t_1, t_0, or ITRPT/STND bit of register C_E, be sure to write "0" to the IRQ FLAG bit after writing to make valid the IRQ FLAG = 1 to be generated after it.

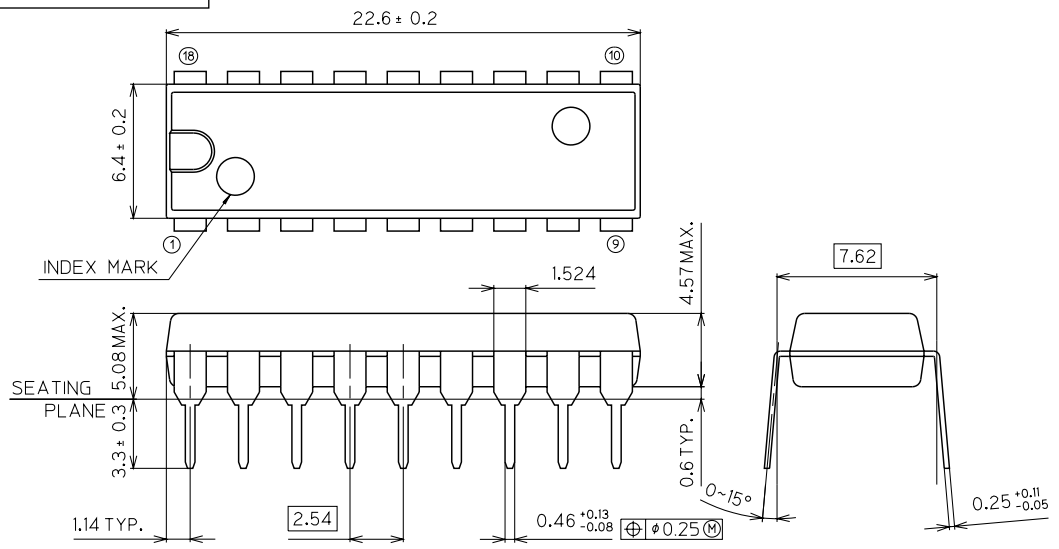
* The relationship between SDT.P OUT and IRQ FLAG bit is shown below:



PACKAGE DIMENSIONS

(Unit : mm)

DIP18-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	1.30 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

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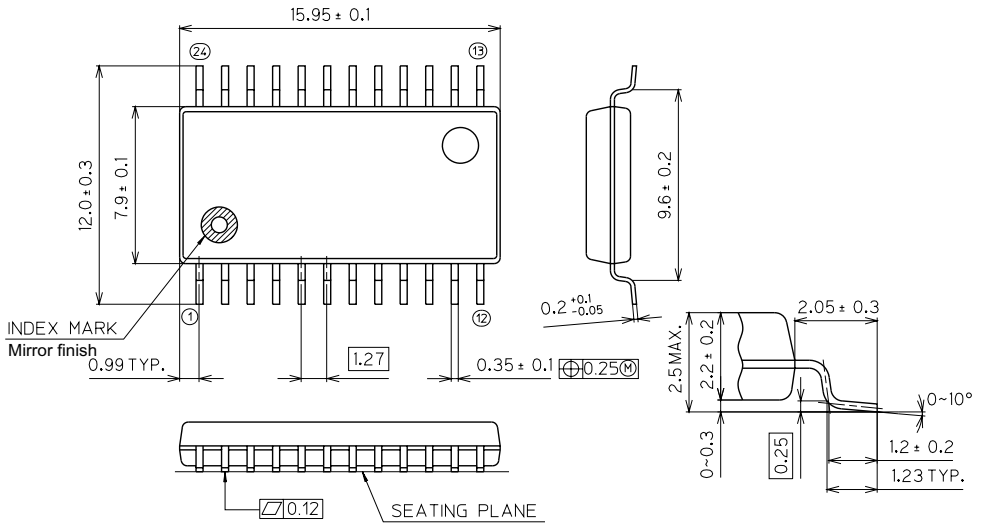
(Unit : mm)

SOP24-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5 μm)
Package weight (g)	0.58 TYP.
Rev. No./Last Revised	5/Oct. 13, 1998

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
—	Apr. 1995	—	—	First edition
FEDL6242B-02	Jun. 17, 2002	1	1	Partially changed contents of "Package" of the FEATURES section.
		—	20	Added the Package Dimensions section and the Contents.
		—	21	

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