APPLICATION NOTE

O K I A S I C P R O D U C T S

0.5μm Technology Clock Skew Management

October 1994

OKI Semiconductor

INTRODUCTION

This application note explains the need for clock skew management and how to apply OKI's clock skew management scheme. OKI offers a solution to clock skew problems for today's high frequency timing sensitive circuits. OKI has developed a clock tree structure which guarantees skew times as low as 0.5 ns. This clock skew management scheme is available on our high speed 0.5μm ASIC products.

CLOCK SKEW MANAGEMENT

As technology advances, the operational frequency of ICs increase. The clock signal becomes one of the most timing sensitive and critical signals in a circuit. It is quite common to have a system clock driving over 1000 flip-flops in a design. With the traditional clock tree structure, clock skew is difficult to avoid.

A traditional tri-level clock tree structure is shown in *Figure 1*. Imbalance of routing and loading in each level of the clock tree can easily contribute up to 5 ns of RC skew time. Although careful balancing of fan-out and manual placement of each latch can minimize the skew, it is time consuming and impractical.

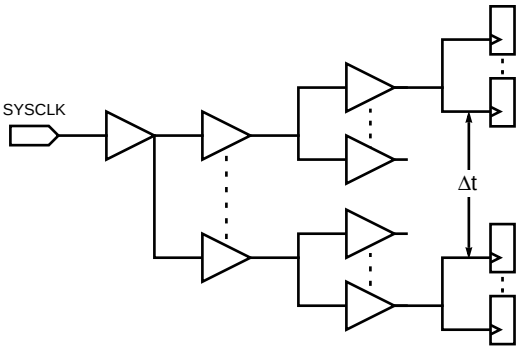

Figure 1. Traditional Tri-Level Clock Tree

FEATURES

- Clock skew < 0.5 ns
- Automatic fan-out balancing
- Dynamic sub-trunk allocation
- Single clock tree driver logic symbol
- Single level clock drivers
- Automatic branch length minimization
- Dynamic driver placement
- Up to four clock trunks allowed

TECHNICAL BRIEF

The basic structure of OKI's clock tree scheme is shown in *Figure 2*. Depending on loading and the array size, an optimized number of clock drivers are paralleled to drive the main clock trunk. When connecting the clock drivers in a paralleled configuration, loads are shared among the drivers, which minimizes clock skew. Sub-trunks are connected to the main trunk, with branches connecting each clocked cell to a sub-trunk.

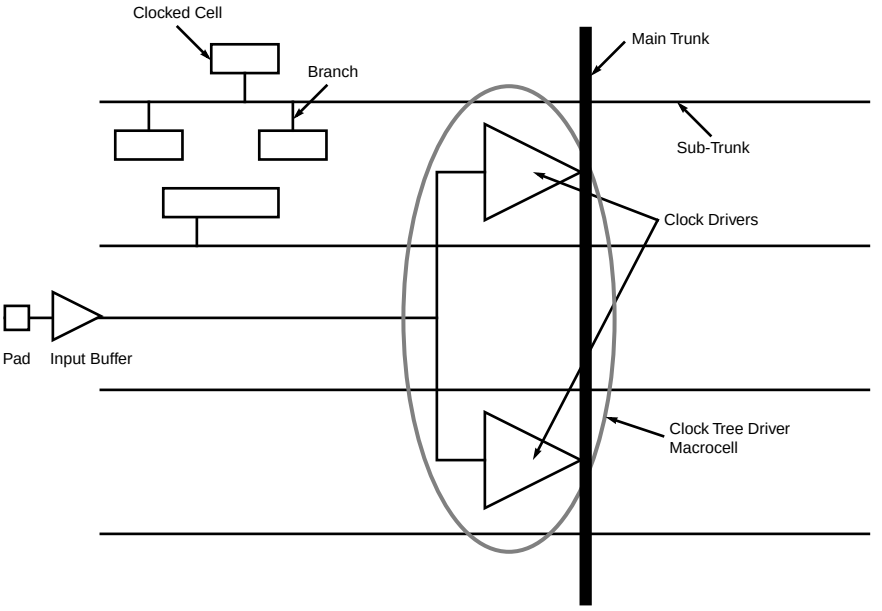

Figure 2. OKI's Clock Tree Structure

Latches and other clocked cells within the same functional logic module usually are directly or indirectly connected to each other. In auto-placement, these cells are placed near each other to maximize routeability. This concentration of clocked cells can imbalance the loading on the clock sub-trunks.

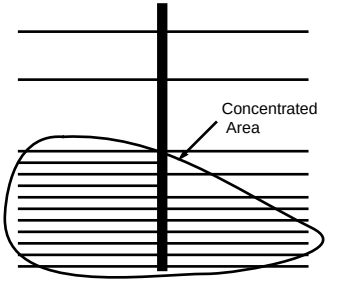

Figure 3. Dynamic Sub-Trunk Allocation

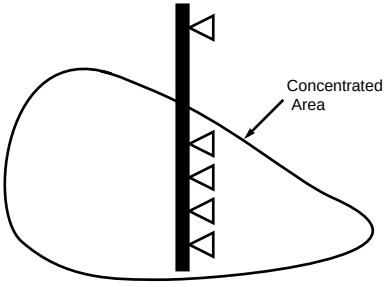

Figure 4. Dynamic Sub-Trunk Allocation

Figure 3 and *Figure 4* show how OKI's clock scheme accommodates this problem. To balance the skew, OKI's placement software dynamically allocates more sub-trunks for the clustered areas, as shown in *Figure 3*. In addition, clock drivers are also dynamically placed to balance the loads of the clustered areas, as shown in *Figure 4*.

In the placement process, multiple clocked cells are assigned to a sub-trunk. Each sub-trunk is assigned approximately the same amount of loads. OKI's placement software further improves the placement of each clocked cell by moving each cell as close as possible to its assigned sub-trunk. Therefore, each sub-trunk is well balanced with minimum branch routing. *Figure 5* and *Figure 6* describe this feature.

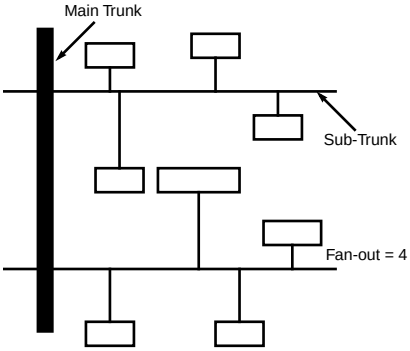

Figure 5. Automatic Sub-Trunk Load Balancing

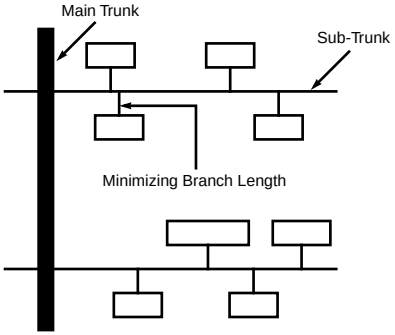

Figure 6. Automatic Branch Length Minimization

APPLICATION GUIDELINES

In general, the clock skew management scheme should be applied in designs whenever the possibility of uncontrollable clock skew exists. Some of the conditions that could warrant the use of a clock tree are:

1. Less than 4 ns hold-time margin in timing simulations
2. Clocks with over 50 fan-outs
3. Clock operation frequency above 25 MHz with uncontrolled placement

Please note that problems due to clock skew are design specific and may exist even when none of the above conditions apply. For further guidelines contact OKI's ASIC Applications Department.

Clock tree drivers are physically paralleled drivers, represented by a single logic symbol. A logic designer simply uses a clock tree driver macrocell during schematic capture and does not have to build a traditional clock tree. OKI's clock tree software will automatically build the clock tree.

Two examples of the physical clock tree driver macrocells and their logic symbols are shown in *Figure 7*.

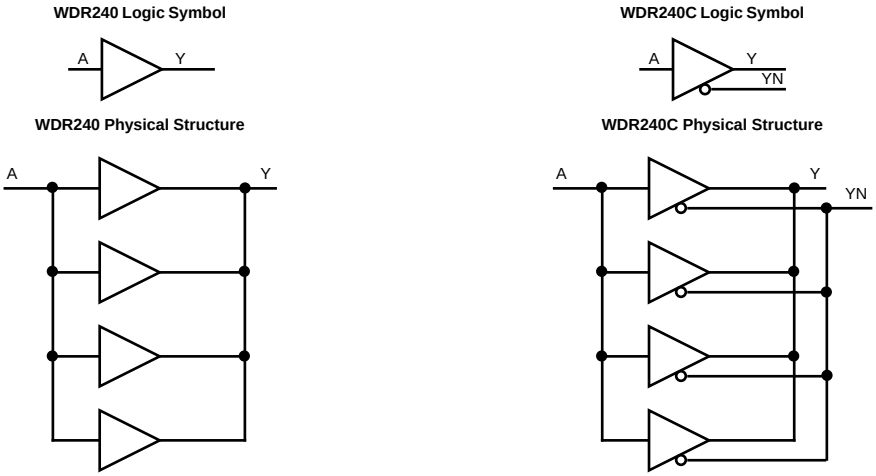

Figure 7. Physical Clock Tree Driver Macrocell and Logic Symbol

A list of available clock tree drivers is shown in *Table 1*.

Table 1. Available Clock Tree Drivers

Clock Tree Driver Macro	Function
WDR220(C)	20X Drive Clock Tree Driver (with complement output)
WDR240(C)	40X Drive Clock Tree Driver (with complement output)
WDR260(C)	60X Drive Clock Tree Driver (with complement output)
WDR280(C)	80X Drive Clock Tree Driver (with complement output)
WDR2100(C)	100X Drive Clock Tree Driver (with complement output)
WDR2120(C)	120X Drive Clock Tree Driver (with complement output)
WDR2140(C)	140X Drive Clock Tree Driver (with complement output)

Due to the dynamic placement of the clock drivers, OKI recommends the use of an input buffer or an internal driver to drive the clock tree driver macro. This will minimize the wire length capacitance loading effect at the input terminal of the clock tree driver macrocell.

The maximum fan-out capability of each clock tree driver varies, depending on the size of the chosen array. In a larger array, the clock tree structure is more extensive; therefore, a larger clock tree driver should be used. The smaller clock tree drivers are restricted to the smaller arrays unless floor planning is utilized to restrict the clock tree area. In this case, floorplanning must limit the clock tree area to the number of rows specified in *Tables 3*, *4*, and *5*. Caution should be used not to select too large of a clock tree driver, as this may adversely affect the routability of a design.

Besides the array size and the fan-out of the clock signal, the designer should also consider the clock frequency. The higher the clock frequency, the narrower the clock pulse; hence, a larger clock tree driver macrocell is needed for fast Tr and Tf.

Maximum skew times for each array and maximum fan-out capabilities for each array at different frequency ranges are listed in *Table 2*, *3*, *4*, and *5*.

Table 2. Maximum Skew Time

MSM10R/13R	MSM98R	Skew Time
0170, 0350, 0560, 0790, 1070	020X020 ~ 072X072	0.5 ns
1750, 2850, 3930	076X076 ~ 112X112	0.8 ns
4990, 7730	118X118 ~ 156X156	Under evaluation

Table 3. Maximum Fan-Out (Frequency < 60 MHz)

MSM98R	MSM10R MSM13R	WDR220(C)	WDR240(C)	WDR260(C)	WDR280(C)	WDR2100(C)	WDR2120(C)	WDR2140(C)
020x020	—	470	960	1440	1930	2420	2900	3390
024x024	—	460	930	1410	1880	2360	2840	3310
026x026	0170	460	930	1400	1880	2350	2830	3300
030x030	—	450	920	1390	1860	2330	2800	3270
032x032	—	450	920	1390	1860	2330	2790	3260
036x036	0350	440 [1]	910	1370	1840	2310	2770	3240
038x038	—	440 [1]	900	1370	1830	2300	2760	3230
040x040	—	440 [1]	900	1360	1830	2290	2750	3220
042x042	—	430 [1]	900	1360	1820	2280	2740	3200
044x044	0560	430 [1]	890	1350	1810	2270	2730	3190
048x048	—	430 [1]	880	1340	1800	2250	2710	3170
050x050	—	420 [1]	880	1330	1790	2250	2700	3160
052x052	0790	420 [1]	870	1330	1780	2240	2690	3140
056x056	—	410 [1]	870	1320	1770	2220	2670	3120
060x060	1070	410 [1]	860	1310	1750	2200	2650	3100
064x064	—	380 [1]	800	1220	1640	2060	2480	2900
068x068	—	370 [1]	790 [2]	1210	1630	2040	2460	2880
072x072	—	370 [1]	780 [2]	1200	1610	2020	2440	2850
076x076	1750	360 [1]	770 [2]	1190	1600	2010	2420	2830
080x080	—	360 [1]	770 [2]	1170	1580	1990	2400	2810
084x084	—	350 [1]	760 [2]	1160	1570	1970	2380	2780
088x088	—	350 [1]	750 [2]	1150	1550	1960	2360	2760
092x092	—	340 [1]	740 [2]	1140	1540	1940	2340	2740
096x096	2850	340 [1]	730 [2]	1130	1520	1920	2320	2710
100x100	—	330 [1]	720 [2]	1120 [3]	1510	1900	2290	2690
104x104	—	320 [1]	710 [2]	1100 [3]	1490	1880	2280	2670
108x108	—	320 [1]	710 [2]	1090 [3]	1480	1870	2250	2640
112x112	3930	310 [1]	700 [2]	1080 [3]	1470	1850	2230	2620

[1] Clock tree area must be restricted to 106 rows.

[2] Clock tree area must be restricted to 213 rows.

[3] Clock tree area must be restricted to 320 rows.

Table 4. Maximum Fan-Out (60 MHz < Frequency < 75 MHz)

MSM98R	MSM10R MSM13R	WDR220(C)	WDR240(C)	WDR260(C)	WDR280(C)	WDR2100(C)	WDR2120(C)	WDR2140(C)
020x020	—	370	760	1150	1540	1930	2310	2700
024x024	—	360	740	1110	1490	1870	2250	2620
026x026	0170	360	730	1110	1480	1860	2240	2610
030x030	—	350	720	1100	1470	1840	2210	2590
032x032	—	350	720	1090	1460	1830	2210	2580
036x036	0350	340 [1]	710	1080	1450	1820	2180	2550
038x038	—	340 [1]	710	1070	1440	1810	2170	2540
040x040	—	340 [1]	700	1070	1430	1800	2160	2530
042x042	—	340 [1]	700	1060	1430	1790	2150	2520
044x044	0560	330 [1]	690	1060	1420	1780	2140	2500
048x048	—	330 [1]	690	1050	1400	1760	2120	2480
050x050	—	320 [1]	680	1040	1400	1750	2110	2470
052x052	0790	320 [1]	680	1030	1390	1750	2100	2460
056x056	—	320 [1]	670	1020	1370	1730	2080	2430
060x060	1070	310 [1]	660	1010	1360	1710	2060	2410
064x064	—	280 [1]	600	930	1250	1570	1890	2210
068x068	—	280 [1]	590 [2]	910	1230	1550	1870	2190
072x072	—	270 [1]	590 [2]	900	1220	1530	1850	2170
076x076	1750	260 [1]	580 [2]	890	1200	1520	1830	2140
080x080	—	260 [1]	570 [2]	880	1190	1500	1810	2120
084x084	—	250 [1]	560 [2]	870	1170	1480	1790	2090
088x088	—	250 [1]	550 [2]	860	1160	1460	1770	2070
092x092	—	240 [1]	540 [2]	840	1150	1450	1750	2050
096x096	2850	240 [1]	530 [2]	830	1130	1430	1730	2020
100x100	—	230 [1]	530 [2]	820 [3]	1120	1410	1700	2000
104x104	—	230 [1]	520 [2]	810 [3]	1100	1390	1690	1980
108x108	—	220 [1]	510 [2]	800 [3]	1090	1380	1660	1950
112x112	3930	220 [1]	500 [2]	790 [3]	1070	1360	1640	1930

[1] Clock tree area must be restricted to 106 rows.

[2] Clock tree area must be restricted to 213 rows.

[3] Clock tree area must be restricted to 320 rows.

Table 5. Maximum Fan-Out (75 MHz < Frequency < 100 MHz)

MSM98R	MSM10R MSM13R	WDR220(C)	WDR240(C)	WDR260(C)	WDR280(C)	WDR2100(C)	WDR2120(C)	WDR2140(C)
020x020	—	270	560	850	1140	1430	1720	2010
024x024	—	260	540	820	1100	1380	1660	1930
026x026	0170	260	540	810	1090	1370	1650	1920
030x030	—	250	530	800	1080	1350	1620	1900
032x032	—	250	520	800	1070	1340	1620	1890
036x036	0350	250 [1]	510	780	1050	1320	1590	1860
038x038	—	240 [1]	510	780	1050	1320	1580	1850
040x040	—	240 [1]	510	770	1040	1310	1570	1840
042x042	—	240 [1]	500	770	1030	1300	1560	1830
044x044	0560	230 [1]	500	760	1020	1290	1550	1820
048x048	—	230 [1]	490	750	1010	1270	1530	1790
050x050	—	230 [1]	490	740	1000	1260	1520	1780
052x052	0790	220 [1]	480	740	1000	1250	1510	1770
056x056	—	220 [1]	470	730	980	1240	1490	1740
060x060	1070	210 [1]	460	720	970	1220	1470	1720
064x064	—	180 [1]	410	630	850	1080	1300	1530
068x068	—	180 [1]	400 [2]	620	840	1060	1280	1500
072x072	—	170 [1]	390 [2]	610	820	1040	1260	1480
076x076	1750	170 [1]	380 [2]	600	810	1030	1240	1460
080x080	—	160 [1]	370 [2]	580	800	1010	1220	1430
084x084	—	160 [1]	360 [2]	570	780	990	1200	1410
088x088	—	150 [1]	360 [2]	560	770	970	1180	1380
092x092	—	140 [1]	350 [2]	550	750	950	1160	1360
096x096	2850	140 [1]	340 [2]	540	740	940	1140	1340
100x100	—	130 [1]	330 [2]	530 [3]	720	920	1110	1310
104x104	—	130 [1]	320 [2]	520 [3]	710	900	1100	1290
108x108	—	120 [1]	310 [2]	500 [3]	690	880	1070	1260
112x112	3930	120 [1]	300 [2]	490 [3]	680	870	1050	1240

[1] Clock tree area must be restricted to 106 rows.

[2] Clock tree area must be restricted to 213 rows.

[3] Clock tree area must be restricted to 320 rows.

Examples

Two examples for selecting a correct clock tree driver are shown in *Table 6*.

Table 6. Clock Tree Driver Selection

Function	Example 1	Example 2
Clock frequency	66 MHz	33 MHz
Fan-out	500	2300
Array chosen	MSM10R0350	MSM10R1750
Complement output	Needed	Not needed
Correct clock tree driver	**WDR240C**	**WDR2120**

Delay Calculation

Clock tree driver delays are calculated in the same way as other logic gates, using the delay equation:

$$tpd\left[\frac{LH}{HL}\right] = \left[tpd0\left[\frac{LH}{HL}\right] + \alpha\left[\frac{LH}{HL}\right] * \Sigma FO + \gamma\left[\frac{LH}{HL}\right] * CL + tpc\left[\frac{LH}{HL}\right]\right] * \delta$$

Where -

tpd	=	Propagation delay time (ns)
tpd0	=	Intrinsic or base delay (ns)
ΣFO	=	Sum of fan-in factors of macrocells being driven
CL	=	Interconnect capacitance loading (pF)
tpc	=	Propagation delay constant (ns) (0.13 ns for low-to-high propagation delays) (0.17 ns for high-to-low propagation delays)
α	=	Fan-out propagation delay factor (ns / FO)
γ	=	Interconnect capacitance propagation delay factor (ns / pF)
δ	=	Process, temperature, and voltage variation factor

For clock tree nets, estimated interconnect capacitance (Cnet) must be calculated using the formula below. Clock tree net parameters Cmtx, Csthx, and #st are shown in *Table 7* and *Table 8*.

$$Cnet = Cmtx + [2 * Csthx * \#st] + [Cspan * \#span]$$

Where -

Cnet	=	Estimated capacitance of clock tree net (pF)
Cmtx	=	Main-trunk capacitance (pF)
Csthx	=	Half-sub-trunk capacitance (pF)
#st	=	Number of sub-trunks
Cspan	=	Span capacitance factor (pF / span) (0.029 for MSM10R / 13R / 98R)
#span	=	Number of spans (flip-flops)

Table 7. Array Parameters (pF)

MSM98R	MSM10R/13R	Cmtx	Csthx
020x020	—	0.83	0.05
024x024	—	1.03	0.16
026x026	0170	1.11	0.18
030x030	—	1.31	0.21
032x032	—	1.41	0.22
036x036	0350	1.60	0.26
038x038	—	1.70	0.27
040x040	—	1.80	0.29
042x042	—	1.90	0.30
044x044	0560	2.00	0.32
048x048	—	2.18	0.35
050x050	—	2.28	0.36
052x052	0790	2.38	0.38
056x056	—	2.57	0.41
060x060	1070	2.77	0.44
064x064	—	2.97	0.47
068x068	—	3.16	0.50
072x072	—	3.36	0.54
076x076	1750	3.54	0.56
080x080	—	3.74	0.60
084x084	—	3.94	0.63
088x088	—	4.13	0.66
092x092	—	4.33	0.69
096x096	2850	4.51	0.72
100x100	—	4.71	0.75
104x104	—	4.91	0.78
108x108	—	5.10	0.81
112x112	3930	5.30	0.85

Table 8. Number of Sub-Trunks

WDR220(C)	WDR240(C)	WDR260(C)	WDR280(C)	WDR2100(C)	WDR2120(C)	WDR2140(C)
4	8	12	16	20	24	28

Since the placement of the clock drivers is dynamically determined, routing to the clock drivers is subject to wide variations. OKI recommends the use of high-drive input buffer / driver macrocells to minimize the interconnect capacitance effects. Estimated minimum / maximum capacitance values for the **input net**

driving a clock tree driver are shown in *Table 9*. These values are used to calculate propagation delays for the gate preceding the clock tree driver macrocell.

Table 9. Estimated Input Net Capacitance for Clock Tree Driver Macrocells (pF)

MSM98R	MSM10R/13R	Min	Max
020x020	—	0.070	0.436
024x024	—	0.087	0.642
026x026	0170	0.095	0.698
030x030	—	0.100	0.823
032x032	—	0.103	0.883
036x036	0350	0.110	1.001
038x038	—	0.113	1.064
040x040	—	0.116	1.126
042x042	—	0.118	1.189
044x044	0560	0.122	1.252
048x048	—	0.125	1.367
050x050	—	0.131	1.429
052x052	0790	0.136	1.492
056x056	—	0.139	1.611
060x060	1070	0.142	1.733
064x064	—	0.145	1.858
068x068	—	0.150	1.976
072x072	—	0.155	2.101
076x076	1750	0.160	2.217
080x080	—	0.165	2.342
084x084	—	0.170	2.467
088x088	—	0.175	2.582
092x092	—	0.181	2.707
096x096	2850	0.187	2.826
100x100	—	0.190	2.951
104x104	—	0.194	3.073
108x108	—	0.198	3.192
112x112	3930	0.202	3.317

Delay Example

Given

100K gate, 3-layer metal, SOG design

2000 flip-flops (FD1A type, rising-edge triggered)

66 MHz

Worst case = worst case process, 3V, 85° C (δ = 1.74, *from the MSM10R0000 Family 0.5μm Sea of Gates Design Manual)*

Selections

MSM10R1750 (114,130 usable gates)

WDR2140 (MSM10R1750, 60 MHz to 75 MHz, maximum fan-out = 2140)

IC4A input buffer (symmetrical tpLH / tpHL)

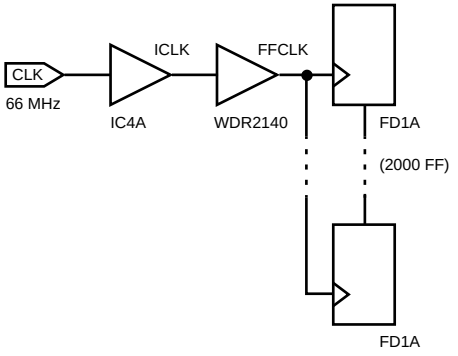

Figure 8. Delay Example

IC4A (Maximum Fan-Out = 75)

From	To	LH/HL	tpd0 (ns)	α (ns/FO)	γ (ns/pF)
A	Y	LH	0.302	0.008	0.164
		HL	0.459	0.009	0.176

WDR2140 (Fan-In = 21.8)

From	To	LH/HL	tpd0 (ns)	α (ns/FO)	γ (ns/pF)
A	Y	LH	0.2452	0.0001	0.0025
		HL	0.3642	0.0003	0.0054

Note: This data was based on the MSM10R0000 Family 0.5μm Sea of Gates Macrocell Library.

Path Delay Calculations (LH)

Path delay calculations (LH) are shown below.

Clock-Tree net capacitance

= Cmtx + Csthx * 2 * #st + 0.029 * fan-out
= 3.54 + 0.56(2)(28) + 0.029(2000)
= 92.9 pF

tpLH-IC4A (ICLK net with maximum capacitance)

= tpd0[LH] + α[LH] * $\sum$FO + γ[LH] * CL + tpc[LH]
= 0.302 + 0.008(21.8) + 0.164(2.217) + 0.13
= 0.970 ns

tpLH-WDR2140 (FFCLK net)

= tpd0[LH] + α[LH] * $\sum$FO + γ[LH] * CL + tpc[LH]
= 0.2452 + 0.0001(2000) + 0.0025(92.9) + 0.13
= 0.807 ns

tpLH-pin-to-FF (typical)

= tpLH-IC4A + tpLH-WDR2140
= 0.970 + 0.807
= 1.777 ns

tpLH-pin-to-FF (worst case)

= tpLH-pin-to-FF (typical) * δ
= 1.777(1.74)
= 3.092 ns

OKI ASSISTANCE

For questions or further assistance on clock skew management, please contact OKI's ASIC Application Department at (408) 720-1900 (west coast) or (617) 279-0293 (east coast).