MITEL

ISO-CMOS **MT4325**
Programmable Keypad Pulse Dialer

FEB. 1985

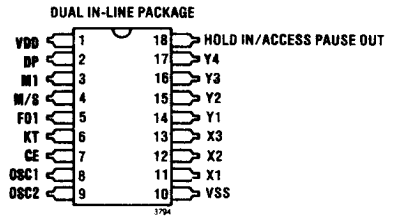
Features

- Last number redial
- Multiple access pause programming
- Any valid keypad input or HOLD IN causes exit from access pause
- Oscillator start up controlled from keypad input
- Oscillator power down whilst not dialing
- 300Hz Key Tone indicates valid key
- 2.0V to 7.0V supply voltage operating range
- Stores up to 20 digits and access pauses
- Digit memory retained down to 1.5V at 1µA
- Selectable mark/space ratio 66⅔:33⅓ or 60:40
- 10Hz dialing speed (932Hz fast test)

Applications

- Pushbutton telephones with last number redial
- Repertory dialers
- Tone to pulse converters

Pin Connections



Ordering Information

MT4325AC	18-Pin Cerdip DIP
MT4325AE	18-Pin Plastic DIP

Description

The Mitel MT4325 Keypad Pulse Dialer contains all the logic necessary to interface a 2 of 7 keypad and convert this key information to control and mute pulses simulating a telephone rotary dial. The MT4325 has programmable access pause capability to provide automatic interruption of dialing needed when accessing the toll network, WATS line or public network via a PABX. The device is fabricated using Mitel ISO-CMOS™ technology which enables functionality down to 2.0V making the device ideal for long loop operation.

The MT4325 will accept up to 20 digits and access pauses and will redial stored information at a later time by activation of # key. Device current in standby is less than 1µA at 1.5V.

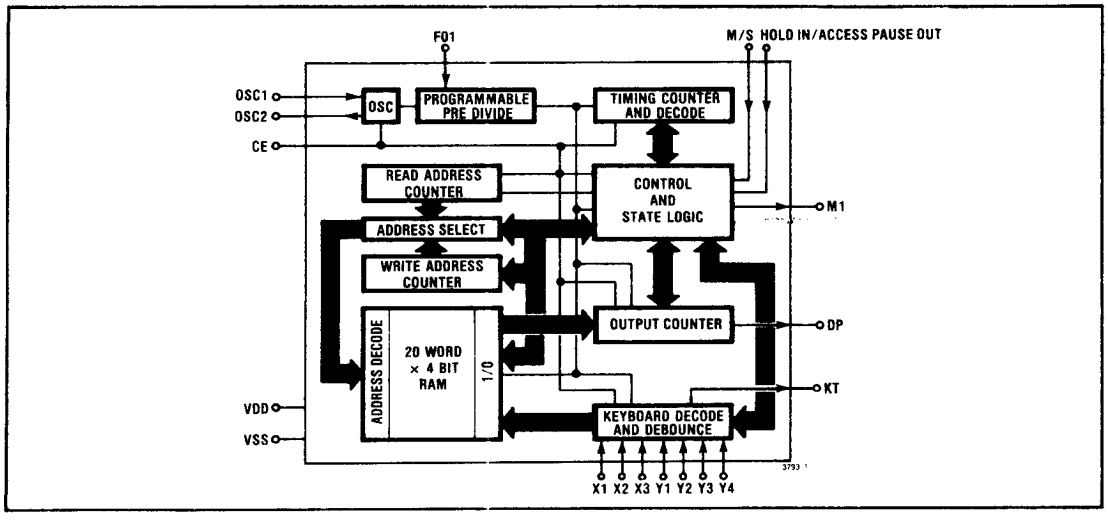


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings#

	MIN	MAX
$V_{DD}-V_{SS}$	−0.3V	10V
Voltage on any pin	V_{SS} −0.3V	V_{DD} +0.3V
Current at any pin		10mA
Operating Temperature	−40 °C	+85 °C
Storage Temperature (C Package)	−65 °C	+150 °C
Power Dissipation (C Package) #		1000mW

#Derate 16mW/ °C above 75 °C. All leads soldered to PC board.

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

DC Electrical Characteristics

All voltages referenced to V_{SS} unless otherwise noted.

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS UNLESS NOTED V_{DD} = 3.0V, T_A = 25 °C f_{CLK} = 3.579545 MHz	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.0		7.0	V		
2	SUPPLY	Standby Supply Current		I_{DDS}		1.0	3.0	μA	CE = M/S = F01 = HOLD IN = V_{SS}, V_{DD} = 1.5V	
3	SUPPLY	Operating Supply Current		I_{DD}		125	250	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	−0.5	−3.0	−8.0	μA	V_{IN} = V_{SS}	X_1, X_2, X_3
5	INPUT	Input Leakage Current		I_{IH}		0.1		nA	V_{IN} = V_{DD}	Y_1, Y_2, Y_3, Y_4
6	INPUT	Input Leakage Current		I_{IL}		−0.1		nA	V_{IN} = V_{SS}	M/S, F01
7	INPUT	Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	100	μA	V_{IN} = V_{DD}	
8	INPUT	Input Low Level Voltage		V_{IL}			0.9	V	All inputs	
9	INPUT	Input High Level Voltage		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11	OUTPUT	Voltage Levels	High-level	V_{OH}	2.99	3		V	No Load	
12	OUTPUT	Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M_1, KT
13	OUTPUT	Drive Current	N-Channel Sink	I_{OL}	0.2	0.5		mA	V_{OUT} = 0.5V	DP, M_1, KT
14	OUTPUT	Drive Current	P-Channel Source	I_{OH}	−0.8	−2.0		mA	V_{OUT} = 0.7V	DP, M_1, KT
15	OUTPUT	Drive Current	P-Channel Source	I_{OH}	−0.2	−0.5		mA	V_{OUT} = 2.5V	DP, M_1, KT
16	IN/OUTPUT	Input Low Level Voltage		V_{IL}			0.9	V		
17	IN/OUTPUT	Input High Level Voltage		V_{IH}	2.1			V		
18	IN/OUTPUT	Output Low Level Current		I_{OL}	8	15		μA	V_{OUT} = 0.5V	CE, HOLD IN/ACCESS PAUSE OUT
19	IN/OUTPUT	Output High Level Current		I_{OH}	5	−12		μA	V_{OUT} = 2.5V	CE, HOLD IN/ACCESS PAUSE OUT
20	IN/OUTPUT	Input Force High Current (from V_{OL})		I_{FH}		55	100	μA	V_{IN} = 2.5V	CE, HOLD IN/ACCESS PAUSE OUT
21	IN/OUTPUT	Input Force Low Current (from V_{OH})		I_{FL}		−70	−100	μA	V_{IN} = 0.5V	CE, HOLD IN/ACCESS PAUSE OUT

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

AC Electrical Characteristics

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS UNLESS NOTED V_{DD} = 3.0V, T_A = 25°C f_{CLK} = 3.579545 MHz
1	DYNAMIC	Output Rise Time	t_R		1.0		µs	DP, M_1
2		Output Fall Time	t_F		1.0		µs	C_L = 50pF
3		Maximum Clock Frequency	f_{CLK}	3.58			MHz	3.579545 MHz Crystal
4		Mark to Space Ratio (DP Output)	M/S		2:1			M/S = O/C (V_{SS})
5					3:2			M/S = V_{DD}
6		System Clock Frequency (Internal)			300		Hz	F01 = V_{SS}
7		Impulsing Rate = I/T			10		Hz	F01 = V_{SS}
8		Fast Test Impulsing Rate			932		Hz	F01 = V_{DD}
9		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE ↑ '1'
10		Input Capacitance	C_{in}		5.0		pF	Any Input

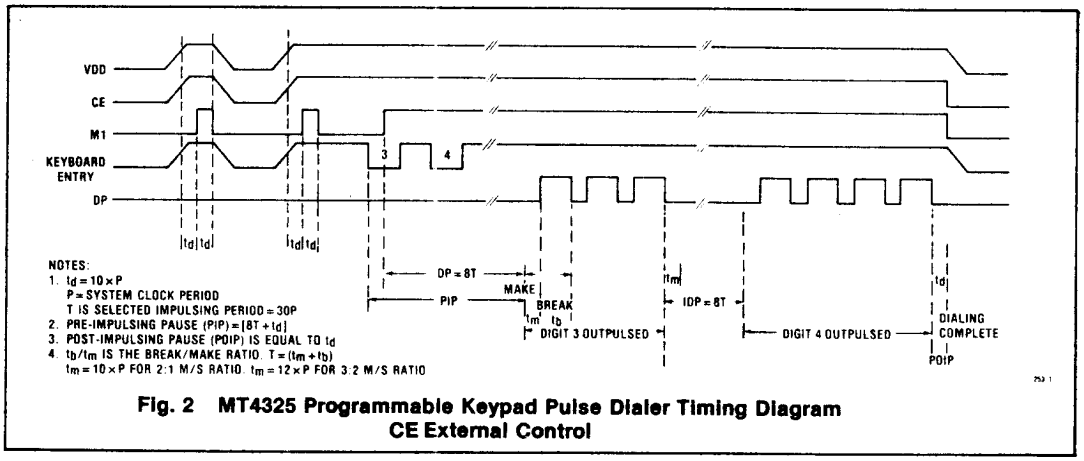


Fig. 2 MT4325 Programmable Keypad Pulse Dialer Timing Diagram
CE External Control

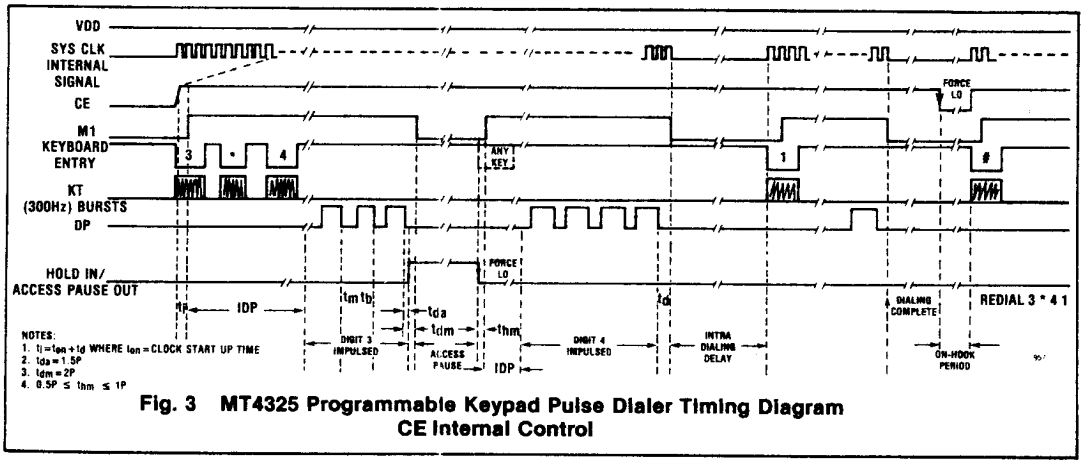


Fig. 3 MT4325 Programmable Keypad Pulse Dialer Timing Diagram
CE Internal Control

TABLE 1

PIN FUNCTION	DESCRIPTION
V_{DD}	Positive voltage supply
DP	Dial Pulsing Output Buffer
M1	Mute Output Buffer
M/S	Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}. O/C = 2:1; V_{DD} = 3:2. Note: O/C = Open Circuit
F01	Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}. * Assumes f_{CLK} = 3.579545MHz.

F01	Nominal Impulsing Rate	Actual* Inpulsing Rate	System Clock frequency
O/C	10Hz	10.13Hz	303.9Hz
V_{DD}	932Hz	932.17Hz	27,965.1Hz

CE	Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.		
XTAL IN	Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.		
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.		
V_{SS}	System ground		
X_1, X_2, X_3	Column keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.		
Y_1, Y_2, Y_3, Y_4	Row keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.		
HOLD IN/ ACCESS PAUSE OUT	INPUT/OUTPUT	O/C	Normal Operation
	INPUT	V_{DD}	No impulsing. If activated during impulsing, hold occurs when the current digit is complete.
	OUTPUT	V_{DD}	Logic "1" level output indicates access pause condition.
KT	300Hz		Square wave bursts indicate valid keypad input.

TABLE 2 KEYPAD INPUT CODE

No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
# RE-DIAL		1	1	1	0	1	1	0
* ACCESS PAUSE		1	1	1	0	0	1	1

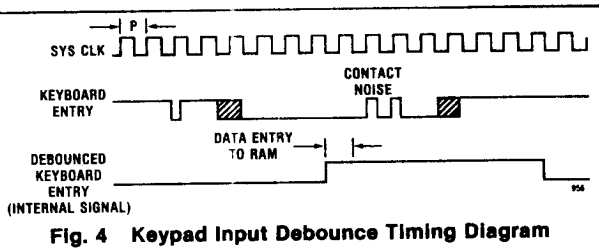


Fig. 4 Keypad Input Debounce Timing Diagram

Functional Description

The Mitel MT4325 programmable keypad pulse dialer is optimized for use in key-operated pulse dialing telephone sets and contains features which make it particularly suitable for applications where redial of last number dialed and repertory dial facilities are required.

The MT4325 accepts keypad information directly from a dual contact keypad having two single pole switches per key; one switch common to the column and one switch common to the row. The common row contacts are connected Y1 to Y4 and the common column contacts connected X1 to X3. The other side of each switch is connected to a common VSS line. The keypad code is shown in Table 2.

The MT4325 will accept up to 20 digits and access pauses; e.g., 18 digits plus 2 access pauses or alternately 19 digits plus 1 access pause. Prior to a keypad input being accepted contact bounce is eliminated by a circuit which ensures that any input which is valid for less than 10 ms is rejected and any input valid for greater than 17 ms is accepted as a valid key input. This circuit operates similarly on the trailing edge of a valid key input preventing multiple digit recognition in the presence of noise. Debounce operation is shown in Fig. 4.

The first key entered in any dialing sequence initiates the oscillator on the MT4325 by internally taking CE high. The oscillator signal is divided down to the System Clock (SYS CLK) frequency by a programmable pre-divide circuit. This internal SYS CLK signal is used for all input and output timing. Digits may be entered asynchronously from the keypad. Dialing and mute functions are output as shown in Fig. 2 and Fig. 3. Fig. 2 shows use of the MT4325 with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialer circuit. In this mode the pulse occurring on M1 when CE is taken high with no keypad input can be used to initiate the bistable latching relay.

Fig. 3 shows the timing diagram of the MT4325 including access pause and redial mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously and dialing commences after recognition of the leading edge of the first valid key input. When an access pause is reached M1 goes low and Hold In/Access Pause Out goes high, indicating the device is in an access pause. This output signal can be used to enable an external dial tone recognition circuit. Exit from the access pause is achieved by one of two methods. One method is by the next valid key operation. If a valid digit is entered, the digit will be entered in the next consecutive storage location in the digit memory. If the key # is activated, redialing of the number in memory will occur only if the device is in the redial mode. The alternative method to exit from an access pause is to pulse Hold In/Access Pause Out low resetting the output latch associated with this input/output pin.

Fig. 3 shows a pause in dialing between the completion of dialing digit "4" and keying digit "1". In this condition, the oscillator powers down to minimize power consumption and interfering signals, whilst CE remains high. On recognition of the next digit, the digit is entered in the next consecutive memory location and dialing resumes.

The end of a key entry sequence is indicated to the MT4325 by externally pulsing or clamping CE low. This causes the on chip latch holding CE high to reset.

If the first key entered after a CE low period is #, redial of the last number dialed will occur. Access pause operation is as previously described. In the standby condition, the MT4325 dissipates typically less than 1.5 μW.

Applications

Keypad Pulse Dialing Telephone With Redial Capability

The MT4325 provides all of the signals required to implement a keypad pulse dialing telephone. The circuit in Figure 5 shows how the MT4325 is interfaced to the telephone line and 500 type network to provide the following capabilities:

(1) Operation independant of TIP to RING D.C. polarity.
(2) High voltage transient protection.
(3) Present a minimum A.C. impedence of 270K ohm during dialing break periods.
(4) Operation on line impedences up to 1275 ohm driving into 150 ohm D.C. load from 900 ohm source impedence.
(5) Power-on-reset.
(6) On-hook memory retention of last number dialed (for redial).
(7) Draw less than 5µA on-hook.
(8) Insensitivity to keypad depressions on-hook.
(9) Insensitivity to hook switch bounce or sequencing.

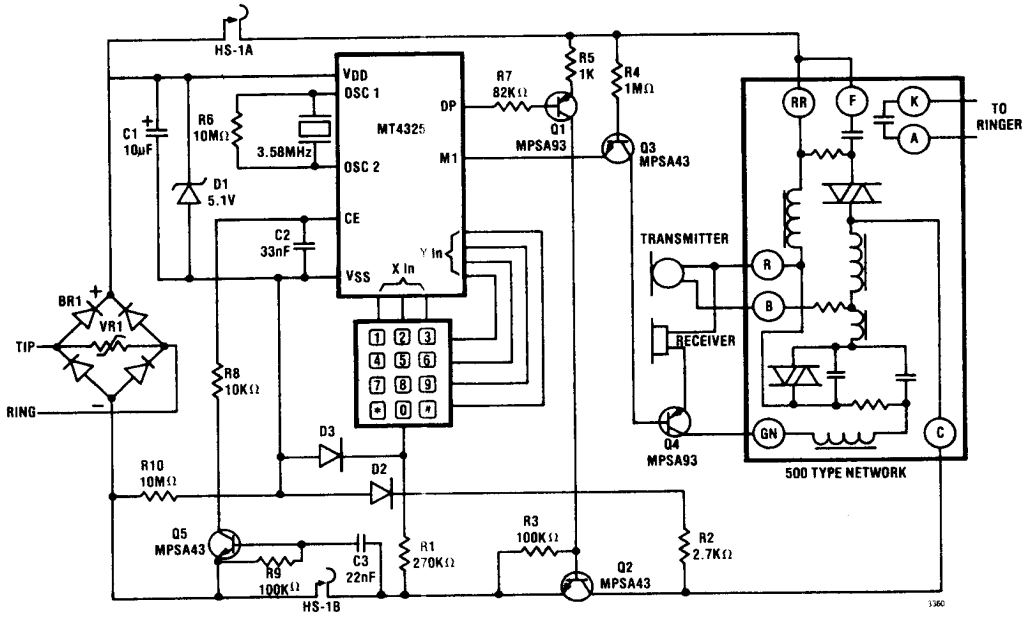


Fig. 5 MT4325 Based Pulse Dialing Telephone Circuit

Protection against TIP to RING polarity reversal and voltage transients is provided by diode bridge BR1 and varistor VR1 respectively, and aided by diode D1 and capacitor C1.

When DP is low, transistor Q1 is turned on, providing base current to Q2. In this condition, loop current flows from BR1 +, through the speech network and Q2 to BR1 −. During outpulsing, a high level at the DP output turns Q1 off, removing base drive from Q2 which in turn blocks the loop current. Muting is provided by transistor Q4 which presents a high impedance in series with the receiver whenever M1 (or M2) is high.

In the loop condition (Q2 on), the supply current for the MT4325 flows from BR1 +, through the device and returns to BR1 − via D2, R2 and Q2. During a loop break (Q2 off), the supply current returns to BR1 − via R1 only. The value of this resistor ensures a high A.C. impedance during loop breaks. Capacitor C1 provides auxiliary supply curent during these periods. Diode D2 prevents the speech network and R2 from shorting the MT4325 supply. Under the various conditions of loop state and line length, the V_{DD} to V_{SS} voltage is limited by zener diode D1 and smoothed by capacitor C1.

The redial function of the MT4325 is enabled by resetting the CE latch and activated by pressing the key #. The latch is reset by momentarily pulling the CE pin low. The circuit shown connected around HS-1B performs this function and is activated by opening the hook-switch. As HS-1B opens, capacitor C3 charges via the base-emitter junction of Q5. This base current pulse causes Q5 to turn on momentarily, pulling CE low. R8 is a current limiting resistor.

An alternative method of resetting the CE latch is simply to connect an auxiliary, normally open hook-switch in parallel with C2 in Figure 5. Under normal dialing conditions, the switch is open and CE is allowed to function normally. When the phone is placed on-hook, this switch connects CE to V_{SS}, resetting the latch.

In the on-hook condition, memory retention of the last number dialed is assured by supplying power to the MT4325 via the 10 Mohm resistor R10. In this condition, the keypad is disabled by D3 which is reverse biased.

Bistable Relay Telephone Connection

In applications where no semiconductor components are allowed in the telephone loop during normal speech, a bistable relay may be used as shown in Figure 6 to isolate the MT4325 and associated devices. A keyboard common changeover switch is required to short circuit the telephone network during keying of the first digit. The positive transition of M1 pulses the bistable relay to ensure that the network is short ciruited for the remainder of the dialing period. When dialing is complete, the bistable relay is pulsed again, connecting the telephone network back into the loop and short circuiting the MT4325 via the keyboard common switch.

If the bistable relay is set such that the MT4325 is connected into the loop when the handset is lifted, a pulse on M1 resets the relay such that the network is reconnected. This pulse is a result of CE being pulled high by R10 in the absence of a keyboard input.

Impulsing is controlled by DP via transistors Q1 and Q2. Resistor R4 provides D.C. termination of the line during dialing to generate voltage for the MT4325 power supply.

The CE reset circuit connected around HS-1B is used to reset the on-chip latch should the hook-switch be flashed during dialing.

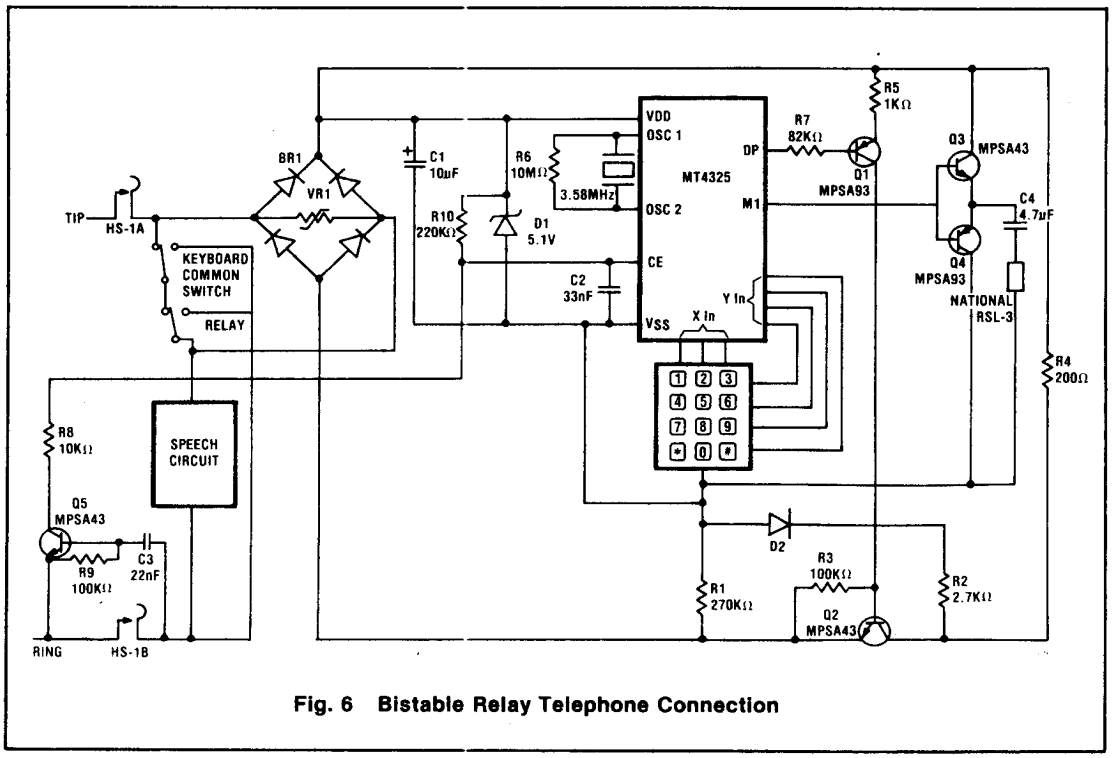


Fig. 6 Bistable Relay Telephone Connection

Single Contact Keyboard Interface

A single contact, matrix-type keyboard may be used with the MT4325 by the addition of the simple interface circuit shown in Figure 7. Depressing any key connects the on-chip pull-up transistor to the base of an external bipolar transistor. The corresponding row input (Y) is clamped to approximately 0.7V by the base-emitter junction of the external transistor. The pull-up transistor on this row input supplies base drive to the bipolar transistor whose collector, in turn, clamps the column input (X) to approximately 0.2V. With these levels on the row and column inputs, a valid keypad entry is obtained.

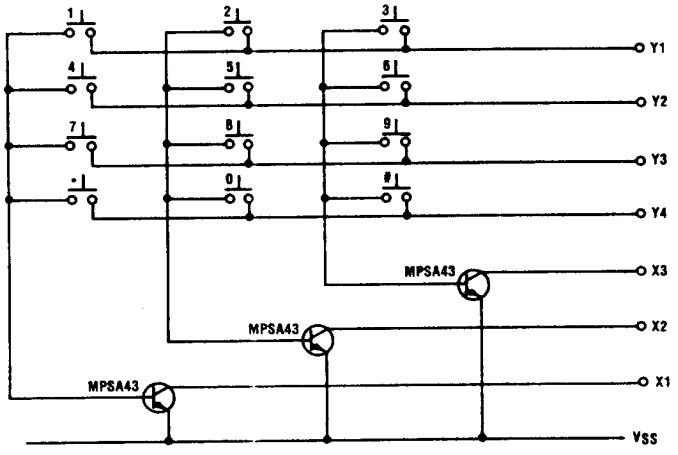


Fig. 7 Single Contact Keyboard Interface

Reset Delay Circuit

If a requirement exists such that the pulse dialer chip should not be reset for loop breaks less than 300ms in duration, then the circuit shown in Figure 8 should be used in place of the standard CE reset circuit. Resistor R2 is connected in series with the loop, with one end referenced to V_{DD} the positive supply of the MT4325. When loop current is flowing, sufficient foltage develops across R2 to turn Q1 on. Capacitor C1 charges to a voltage V_{DD}-V_{CESAT}. This voltage will be greater than the positive threshold of ST1, causing its output to go low and the output of ST2 to go high.

If a loop break occurs, Q1 turns off and C1 discharges via R1. The values of R1 and C1 are chosen such that the discharge time to the negative threshold of ST1 equals 300ms. As this threshold is crossed the output of ST2 goes low. This negative voltage transition is coupled by capacitor C2 and resets the CE latch. Diode D1 blocks positive voltage transitions that occur when loop current is initiated.

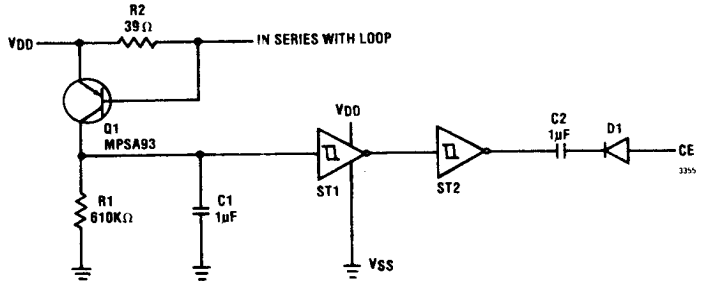


Fig. 8 CE Reset Delay Circuit

Automatic Access Pause Entry

The circuit shown in Figure 9 provides a method for loading access pauses automatically into the MT4325 memory. Upon recognition of the first valid key entry, M1 goes high and charges C1 via R1. When the voltage across C1 becomes greater than the positive threshold of schmitt trigger ST1, its output goes low and the output of ST2 goes high. If a pause in the dialing sequence occurs, (such as waiting for dial tone after the digit 9), then M1 goes low and C1 discharges via R1. When the negative threshold of ST1 is crossed, its output goes high, forcing the output of ST2 low. This negative voltage transistion is coupled via C2 to the keypad input X1 and Y4 causing an access pause to be loaded. The length of the dialing pause required to load an access pause is determined by the time constant R1C1.

When a number is redialed and an access pause state is entered, the Access Pause output goes high and M1 goes low. Transistor Q1 is used to buffer the Access Pause output and prevent loading of unwanted access pauses under these conditions. Diodes D1 and D2 provide isolation between the keypad inputs X1 and Y4.

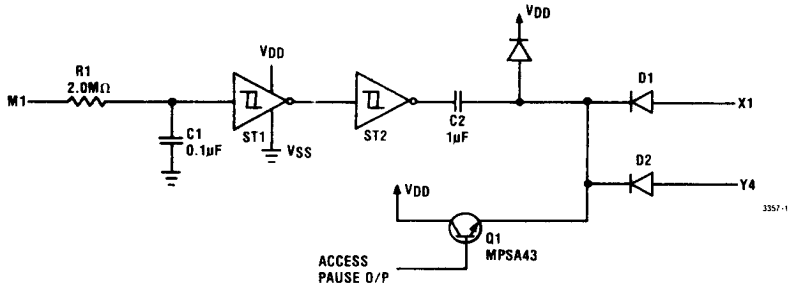


Fig. 9 Automatic Access Pause Entry

Automatic Access Pause Reset

Exiting from an access pause can be done by activating any valid key or alternatively by pulsing the Hold In/Access Pause Out pin low. The circuits of Figures 10 and 11 show two implementations of the latter technique.

In Figure 10, Hold In/Access Pause Out is used to enable a dial tone recognition circuit. This would normally consist of one or more bandpass filters, a level detector, and a pulse generating circuit. Once dial tone has been detected the output pulse is used to momentarily pull Hold-In/Access Pause Out low, resetting the on-chip latch and allowing dialing to continue.

The circuit of Figure 11 relies on the fact that M1 goes low when an access pause is entered. At the beginning of a dialing sequence, M1 goes high, charging C1 via D1. When the access pause is entered, M1 goes low and discharges C1 via R1. As the voltages across C1 drops below the negative threshold of ST1, its output goes high, forcing the output of ST2 low. This negative voltage transition pulls Hold-In/Access Pause Out low, allowing dialing to continue. Diode D2 prevents the output of ST2 from interrupting dialing by holding Hold In/Access Pause Out high whenever M1 is high.

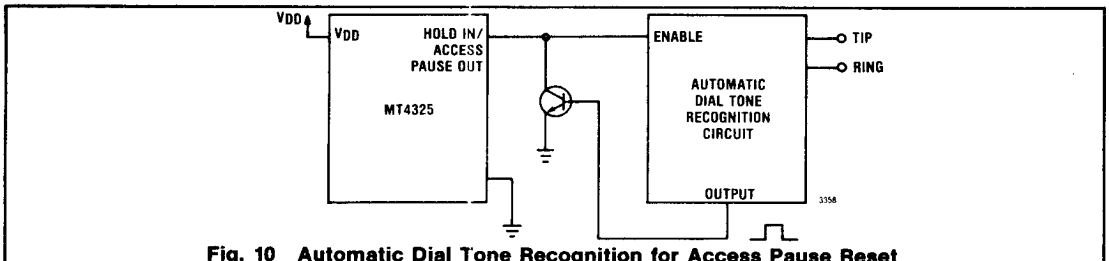


Fig. 10 Automatic Dial Tone Recognition for Access Pause Reset

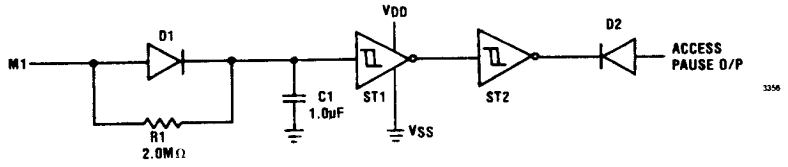


Fig. 11 Automatic Access Pause Reset

Tone to Pulse Converter

The MT4325 is ideally suited for use in various tone to pulse converter designs. A typical system is shown in the block diagram, Figure 12. The 20 digit on-chip, first in-first out memory serves as a buffer to allow asynchronous dialing into the converter and a tone dialing rate considerably faster than the nominal outpulsing rate (10 pulses per second with 800ms interdigit pause). All signals required to control the loop during outpulsing are provided by the MT4325.

The tone receiver portion of the converter is efficiently constructed with the MT8865 and MT8862, Mitel's 2-chip DTMF receiver. The output code of the MT8862 decoder is compatible with the input code of the MT4325 allowing direct interconnection of the two parts. (Q1 to Q4 of the MT8862 to Y1 to Y4 of the MT4325, and Q5 to Q7 of the MT8862 to X1 to X3 of the MT4325). A differential input stage interfaces the tone receiver to the telephone line. The steering output, STD from the tone receiver is fed into the control circuitry to control line splitting.

Off-hook detection, ringing voltage detection, and battery feed circuitry complete the converter, respectively providing signals for the timing circuitry and holding current during the line split condition.

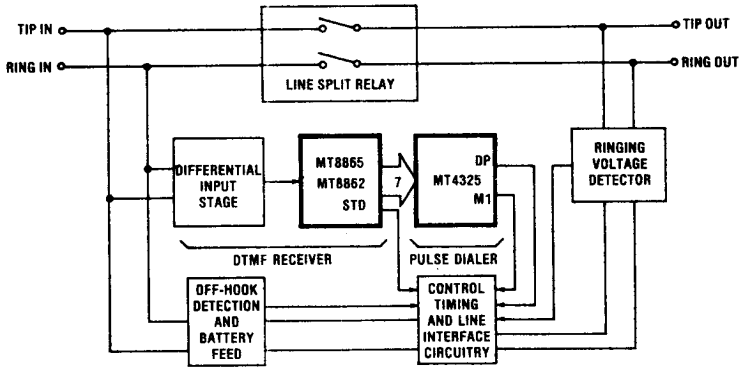


Fig. 12 Tone to Pulse Converter

Repertory Dialer

Figure 13 illustrates the use of the MT4325 in a keypad pulse dialing repertory dialer. The 20-digit on-chip memory of the MT4325 is useful as buffer storage to allow asynchronous loading of digits from the main telephone number memory. The main storage is provided by a 21C14, 24-word by 4-bit RAM. The 2-of-7 keyboard information is encoded to reduce the amount of RAM required. This information is then decoded by the MD74SC139 back to 2-of-7 format for the pulse dialer.

Three modes of operation (NORMAL, PROGRAM, and DIAL), are provided as selected by the MODE SWITCH. In the NORMAL mode, keypad data is fed directly to the MT4325 via the encode-decode loop. Dialing commences upon entry of the first digit.

When the PROGRAM mode is selected, the first two digits keyed in are interpreted as the telephone number address. These numbers are stored in BCD format to alleviate the need for a complex encoding scheme. As such, the capacity of the repertory dialer is limited to 48 16-digit numbers. Each subsequent digit entered, is stored in the main memory and causes the DIGIT ADDRESS COUNTER to be incremented. This is repeated until the entire number has been entered.

The DIAL mode is selected to dial a number from the main memory. Again the first two digits entered are interpreted as the telephone number address. In this mode, the second digit entered triggers the control circuitry to clock the DIGIT ADDRESS COUNTER, read the digits from the main memory, and load them into the buffer memory of the MT4325. These digits are immediately dialed out by the pulse dialer. Redialing of this number can be accomplished by returning to the NORMAL mode and activating the key "#". Access pauses, for use in PABX environments, are stored as any other digit. When an access pause is entered by the MT4325, the HOLD IN/ACCESS PAUSES OUT pin goes high. This signal is used by the control circuitry to interrupt loading of the digit stream until the access pause condition is reset. This prevents unwanted cancellation of the access pause by loading of subsequent digits.

The line interface and speech network control can be derived from the circuits shown in Figure 5. With selection of low power CMOS control circuitry, telephone line powering of the entire circuit becomes a possibility.

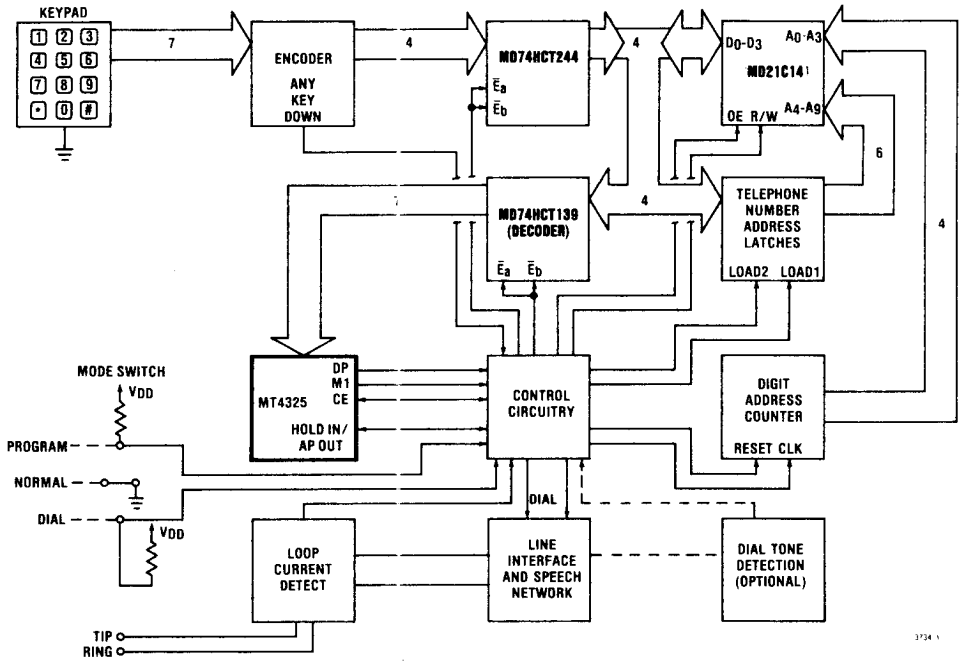


Fig. 13 Keypad Pulse Dialing Repertory Dialer