DESCRIPTION

The TTL/Monostable 9602 Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9602 has excellent immunity to noise on the V_{CC} and ground lines. The 9602 uses TTL inputs and outputs for high speed and high fanout capability and is compatible with all members of the Fairchild TTL family.

FEATURES

72 ns TO ∞ OUTPUT WIDTH RANGE

RETRIGGERABLE 0 TO 100% DUTY CYCLE

TTL INPUT GATING—LEADING OR TRAILING EDGE TRIGGERING

COMPLEMENTARY TTL OUTPUTS

OPTIONAL RETRIGGER LOCK-OUT CAPABILITY

PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS

RESETTABLE

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (dc) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is HIGH	−0.5 V to +V_{CC} value
Current Into Output When Output is LOW	50 mA

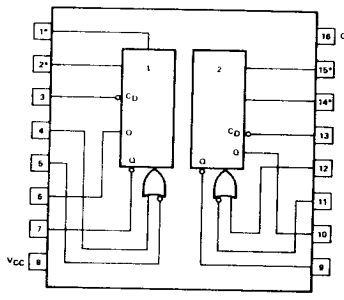
NOTES:

The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.

Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

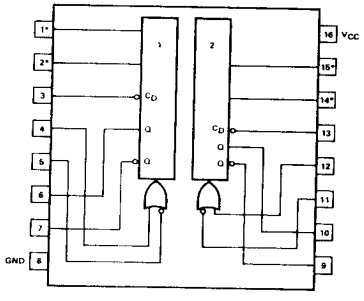
(Top View)

16 PIN DUAL-IN-LINE (B, F PACKAGES)



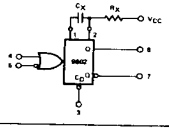
*Pins for external timing

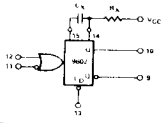
FLATPAK-W



*Pins for external timing

LOGIC DIAGRAM





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FUNCTIONAL DESCRIPTION

The 9602 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9602 and result in a continuous true output. The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by typing Q output to an active level LOW input or the Q output to the active level HIGH input.

OPERATION RULES

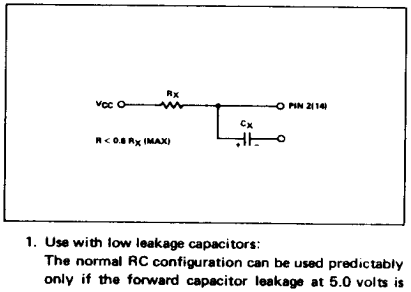
- An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
- The value of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to 75°C operation. The value of R_X may vary from 5.0 kΩ to 25 kΩ for −55 to +125°C operation.
- The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
- The output pulse with (t) is defined as follows:

$$t = 0.31\ R_X C_X \quad 1 + \left[\frac{1}{R_X}\right]$$

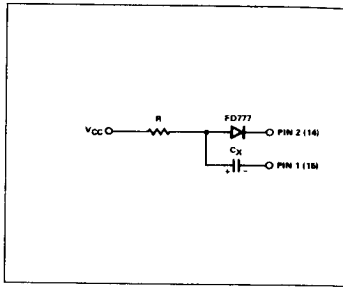
Where

R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see Fig. 14

- If electrolytic type capacitors are to be used, the following three configurations are recommended:

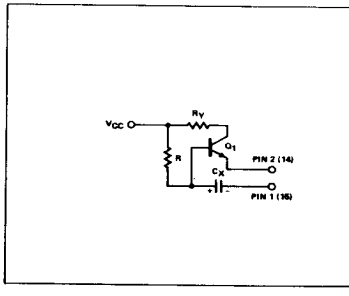


1. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3μA, and the inverse capacitor leakage at 1.0 volt is less than 5μA over the operational temperature range.



2. Use with high inverse leakage current ele
   capacitors:
   The diode in this configuration prevents hig
   leakage currents through the capacitor by p
   an inverse voltage across the capacitor. The u
   configuration is not recommended with retr
   operation.

$$t \approx 0.3\ RC_X$$



3. Use to obtain extended pulse widths:
   This configuration can be used to obtain e
   pulse widths, because of the larger timing
   allowed by beta multiplication. Electrolyti
   high inverse leakage currents can be used.

   $R < R_X$ (0.7) (h_{FE} Q_1) or < 2.5 MΩ whic
   is the lesser
   R_X (min) < R_Y < R_X (max) (5 ≤ R_Y ≤ 1
   is recommended)
   Q_1: NPN silicon transistor with h_{FE} requ
   ments of above equations, such as 2N
   or 2N5962

$$t \approx 0.3\ RC_X$$

This configuration is not recommended wit
triggerable operation.

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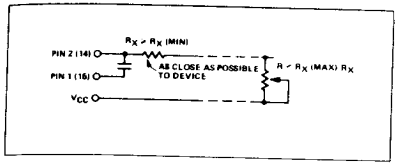
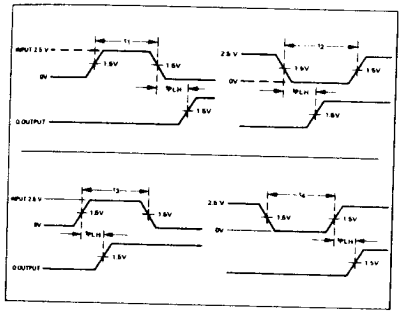
- To obtain variable pulse width by remote trimming, the following circuit is recommended:

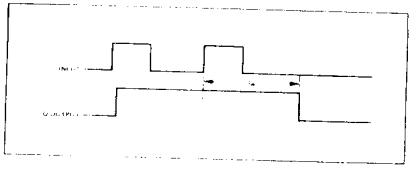


- Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
- Input Trigger Pulse Rules. See Triggering Truth Table, following pages.



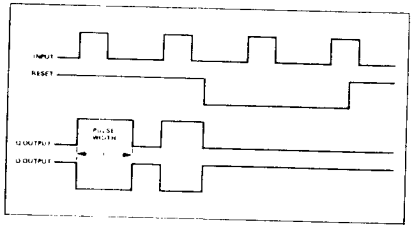
- The retriggerable pulse width is calculated as shown below:

$$t_w = t + t_{PLH} = 0.31\ R_X C_X \left(1 + \frac{1}{R_X}\right) + t_{PLH}$$



The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)

- Reset Operation. An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



- V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 9602 is recommended.

TABLE I - ELECTRICAL CHARACTERISTICS T_A = -55°C to 125°C, V_{CC} = 5 V ±10%

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS (NOTE 1)
		-55°C		+25°C			+125°C		
		MIN	MAX	MIN	TYP	MAX	MIN MAX		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4	Volts	V_{CC} = 4.5V, I_{OH} = -0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.4		0.2	0.4	0.4	Volts	V_{CC} = 4.5V, I_{OL} = 9.92 mA (Note 2)
									V_{CC} = 5.5V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	2.0		1.7			1.5	Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.90	0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current	-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5V, V_{IN} = 0.4V
		-1.24		-0.97	-1.24		-1.24	mA	V_{CC} = 4.5V, V_{IN} = 0.4V
I_{IH}	Input HIGH Current				10	60	60	μA	V_{CC} = 5.5V, V_{IN} = 4.5V

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ELECTRICAL CHARACTERISTICS (Cont'd)

I_{SC}	Short Circuit Current			-25		mA	V_{CC} = 5.5V, V_{OUT} = 1.0V (Note 2)
I_{PD}	Quiescent Power Supply Drain	45	39	45	45	mA	V_{CC} = 5.0V
t_{PLH}	Negative Trigger Input to True Output		25	35		ns	V_{CC} = 5.0V R_X = 5.0 kΩ C_X = 0, C_L = 15pF
t_{PHL}	Negative Trigger Input to Complement Output		29	43		ns	V_{CC} = 5.0V R_X = 5.0 kΩ C_X = 0, C_L = 15pF
$t_{(min)}$	Minimum True Output Pulse Width		72	90		ns	V_{CC} = 5.0V R_X = 5.0 kΩ
	Minimum Complement Output Pulse Width		78	100		ns	C_X = 0, C_L = 15pF
t	Pulse Width		3.08	3.42 3.76		μs	V_{CC} = 5.0V, R_X = 10 kΩ, C_X = 1000pF
C_{STRAY}	Maximum Allowable Wiring Cap (Pins 2 and 14)	50		50	50	pF	Pins 2 and 15 to Ground
R_X	Timing Resistor	5.0 25	5.0	25	5.0 25	kΩ	

TABLE II – ELECTRICAL CHARACTERISTICS T_A = 0°C to 75°C, V_{CC} = 5 V ±5%.

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS (NOTE 1)
		0°C		+25°C			+75°C		
		MIN	MAX	MIN	TYP	MAX	MIN MAX		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.4		2.4	Volts	V_{CC} = 4.75 V, I_{OH} = -0.96m (Note 2)
V_{OL}	Output LOW Voltage		0.45		0.2	0.45	0.45	Volts	V_{CC} = 4.75V, I_{OL} = 11.3mA (Note 2) V_{CC} = 5.25V, I_{OL} = 12.8mA
V_{IH}	Input HIGH Voltage	1.9		1.8			1.65	Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.85	0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		-1.6		-10	-1.6	-1.6	mA	V_{CC} = 5.25V, V_{IN} = 0.45V
			-1.41			-1.41	-1.41	mA	V_{CC} = 4.75V, V_{IN} = 0.45V
I_{IH}	Input HIGH Current				10	60	60	μA	V_{CC} = 5.25V, V_{IN} = 4.5V
I_{SC}	Short Circuit Current					-35		mA	V_{CC} = 5.25V, V_{OUT} = 1.0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		52		39	50	52	mA	V_{CC} = 5.0V, Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				25	40		ns	V_{CC} = 5.0V R_X = 5.0 kΩ C_X = 0, C_L = 15pF
t_{PHL}	Negative Trigger Input to Complement Output				29	48		ns	V_{CC} = 5.0V R_X = 5.0 kΩ C_X = 0, C_L = 15pF
$t_{(min)}$	Minimum True Output Pulse Width				72	100		ns	V_{CC} = 5.0V R_X = 5.0 kΩ
	Minimum Complement Output Pulse Width				78	110		ns	C_X = 0, C_L = 15pF

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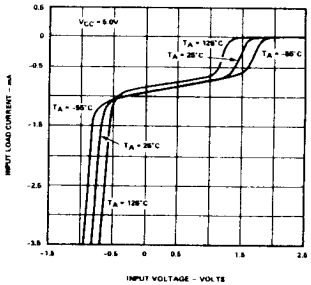
ELECTRICAL CHARACTERISTICS (Cont'd)

t	Pulse Width			3.08	3.42	3.76	μs	V_{CC} = 5.0V, R_X = 10 kΩ, C_X = 1000pF
C_{STRAY}	Maximum Allowable Wiring Cap, (Pins 2 and 14)		50		50	50	pF	Pins 2 and 14 to Ground
R_X	Timing Resistor	5.0	50	5.0	50	5.0 50	kΩ	

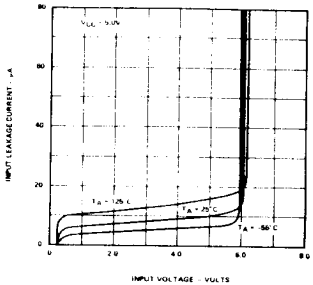
NOTES:
1. Unless otherwise noted, 10 kΩ resistor placed between Pin 2 (14) and V_{CC}, for all tests (R_X).
2. Ground Pin 1 (15) for V_{OL} on Pin 7 (9), or for V_{OH} on Pin 6 (10), or for I_{SC} on Pin 6 (10), also apply momentary ground to Pin 4 (12). Open Pin 1 (15) for V_{OL} on Pin 6 (10), or for V_{OH} on Pin 7 (9), or for I_{SC} on Pin 7 (9).

CHARACTERISTIC CURVES

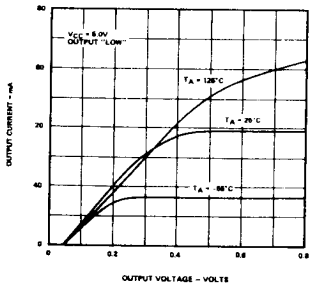
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



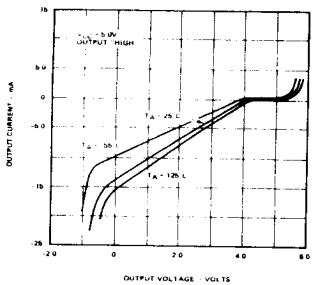
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



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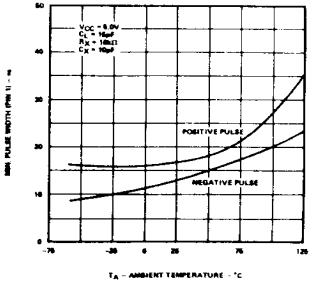
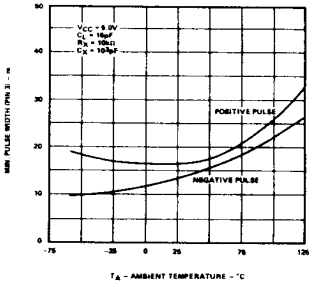
CHARACTERISTIC CURVES (Cont'd)

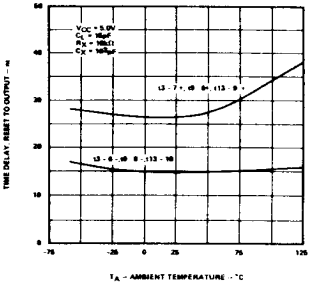
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)



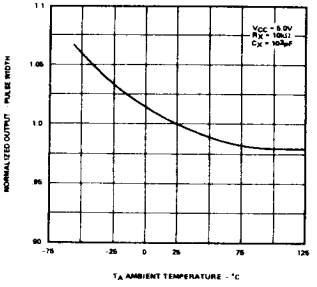
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)



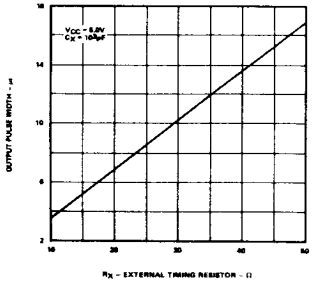
MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE



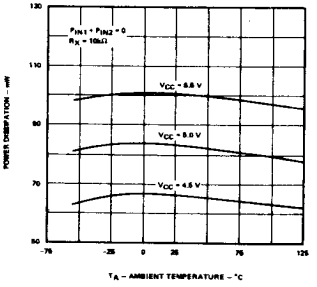
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



PULSE WIDTH VERSUS TIMING RESISTOR



POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



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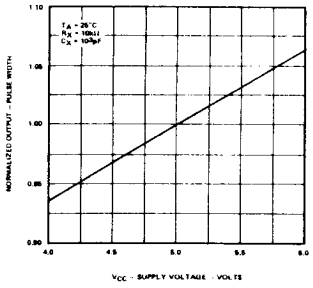
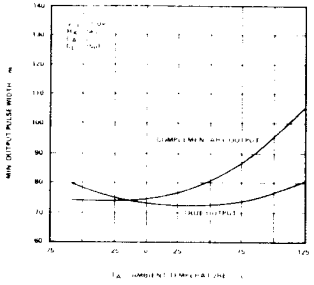
CHARACTERISTIC CURVES (Cont'd)

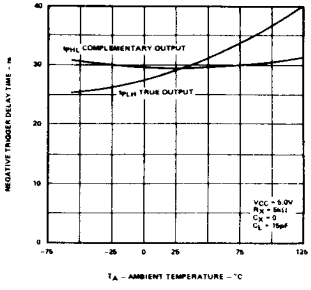
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



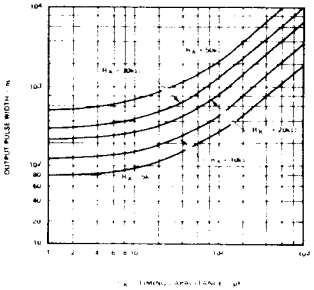
MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF



TRIGGERING TRUTH TABLE

PIN NUMBERS			OPERATION
5 (11)	4 (12)	3 (13)	
H → L	L	H	Trigger
H	H → L	H	Trigger
X	X	L	Trigger

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Don't Care
H→L = HIGH to LOW Voltage Level Transition
L→H = LOW to HIGH Voltage Level Transition

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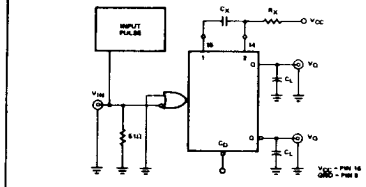
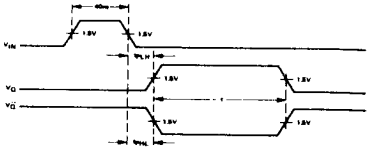
SWITCHING CIRCUITS AND WAVEFORM





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