

# 128 × 8-bit/256 × 8-bit static RAMs with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

## GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I<sup>2</sup>C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8570C which has an alternative slave address for memory extension up to 16 devices.

## Features

- Operating supply voltage            2.5 V to 6 V
- Low data retention voltage        min. 1.0 V
- Low standby current                max. 15 μA
- Power saving mode                 typ. 50 nA
- Serial input/output bus (I<sup>2</sup>C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

## Applications

- Telephony                            RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications) channel presets
- Radio and television                channel presets
- Video cassette recorder            channel presets
- General purpose                     RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

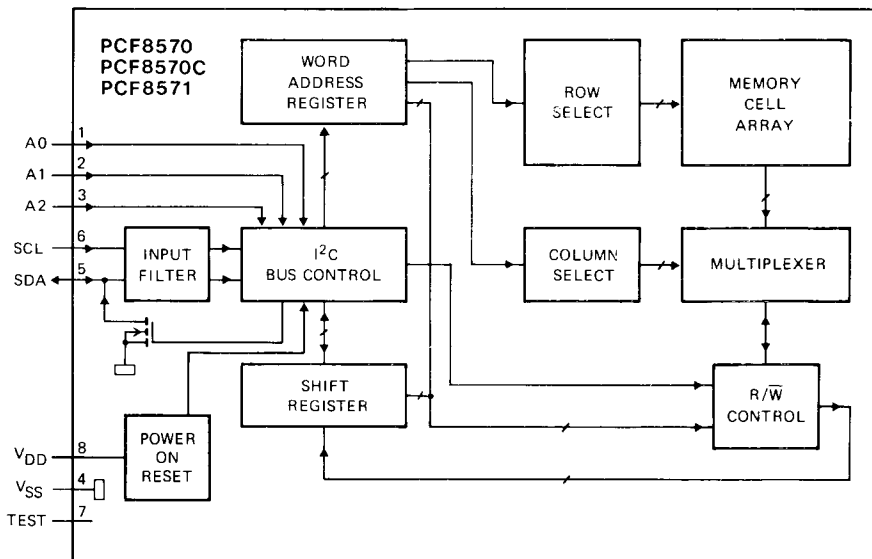


Fig.1 Block diagram.

7290775.3

## PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).  
 PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

# 128 × 8-bit/256 × 8-bit static RAMs with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

## PINNING

1 to 3	A0 to A2	address inputs	
4	V <sub>SS</sub>	negative supply	
5	SDA	serial data line	I <sup>2</sup> C-bus
6	SCL	serial clock line	
7	TEST	test input for test speed-up; must be connected to V <sub>SS</sub> when not in use (power saving mode, see Figs 12 and 13)	
8	V <sub>DD</sub>	positive supply	

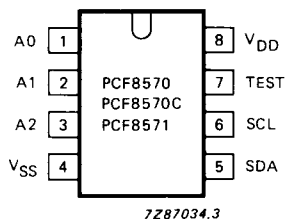


Fig.2 Pinning diagram.

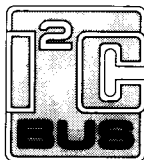
## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V <sub>DD</sub>	-0.8	+8.0	V
Input voltage range	V <sub>I</sub>	-0.8	V <sub>DD</sub> + 0.8	V
DC input current	± I <sub>I</sub>	-	10	mA
DC output current	± I <sub>O</sub>	-	10	mA
V <sub>DD</sub> or V <sub>SS</sub> current	± I <sub>DD</sub> ; ± I <sub>SS</sub>	-	50	mA
Total power dissipation	P <sub>tot</sub>	-	300	mW
Power dissipation per output	P <sub>O</sub>	-	50	mW
Operating ambient temperature range	T <sub>amb</sub>	-40	+85	°C
Storage temperature range	T <sub>stg</sub>	-65	+150	°C

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').



Purchase of Philips' I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C-system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips.

128 × 8-bit/256 × 8-bit static RAMs  
with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

**CHARACTERISTICS**
 $V_{DD} = 2.5$  to  $6$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $+85$  °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
<b>Supply</b>						
Supply voltage		$V_{DD}$	2.5	—	6.0	V
Supply current operating	$V_I = V_{DD}$ or $V_{SS}$ $f_{SCL} = 100$ kHz	$I_{DD}$	—	—	200	$\mu$ A
standby	$f_{SCL} = 0$ Hz $T_{amb} = -25$ to $+70$ °C	$I_{DDO}$	—	—	15	$\mu$ A
		$I_{DDO}$	—	—	5	$\mu$ A
Power-on reset level	note 1	$V_{POR}$	1.5	1.9	2.3	V
<b>Inputs, input/output SDA</b>						
Input voltage LOW	note 2	$V_{IL}$	-0.8	—	$0.3 V_{DD}$	V
Input voltage HIGH	note 2	$V_{IH}$	$0.7 V_{DD}$	—	$V_{DD} + 0.8$	V
Output current LOW	$V_{OL} = 0.4$ V	$I_{OL}$	3	—	—	mA
Leakage current	$V_I = V_{DD}$ or $V_{SS}$	$ I_{LI} $	—	—	1	$\mu$ A
<b>Inputs A0 to A2; TEST</b>						
Input leakage current	$V_I = V_{DD}$ or $V_{SS}$	$\pm I_{LI}$	—	—	250	nA
<b>Inputs SCL; SDA</b>						
Input capacitance	$V_I = V_{SS}$	$C_I$	—	—	7	pF
<b>LOW <math>V_{DD}</math> data retention</b>						
Supply voltage for data retention		$V_{DDR}$	1	—	6	V
Supply current	$V_{DDR} = 1$ V	$I_{DDR}$	—	—	5	$\mu$ A
Supply current	$V_{DDR} = 1$ V; $T_{amb} = -25$ to $+70$ °C	$I_{DDR}$	—	—	2	$\mu$ A
<b>Power saving mode</b>						
	see Figs 12 and 13					
Supply current	TEST = $V_{DD}$ ; $T_{amb} = 25$ °C					
PCF8570/PCF8570C		$I_{DDR}$	—	50	400	nA
PCF8571		$I_{DDR}$	—	50	200	nA
Recovery time		$t_{HD2}$	—	50	—	$\mu$ s

**Notes to the characteristics**

1. The power-on reset circuit resets the I<sup>2</sup>C-bus logic when  $V_{DD} < V_{POR}$ . The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage  $V_{DD}$  or  $V_{SS}$  an input current will flow: this current must not exceed  $\pm 0.5$  mA.

# 128 × 8-bit/256 × 8-bit static RAMs with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

## CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

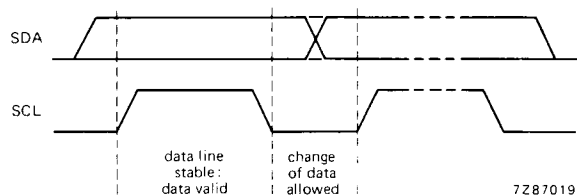


Fig.3 Bit transfer.

### Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

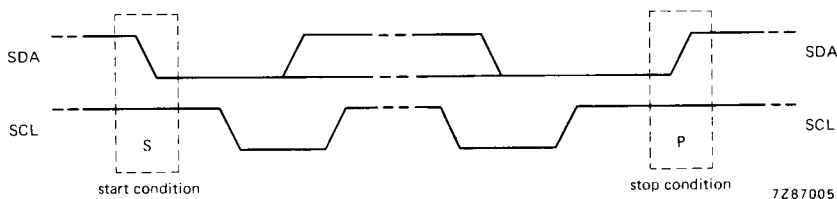


Fig.4 Definition of start and stop conditions.

# 128 × 8-bit/256 × 8-bit static RAMs with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

## System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

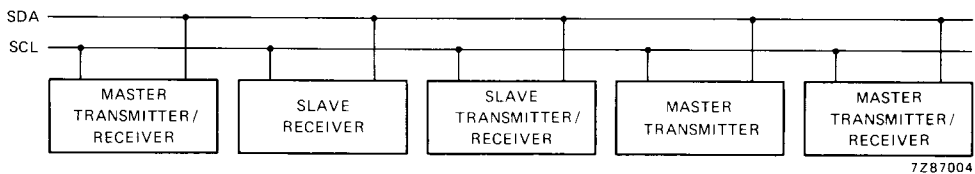


Fig.5 System configuration.

## Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

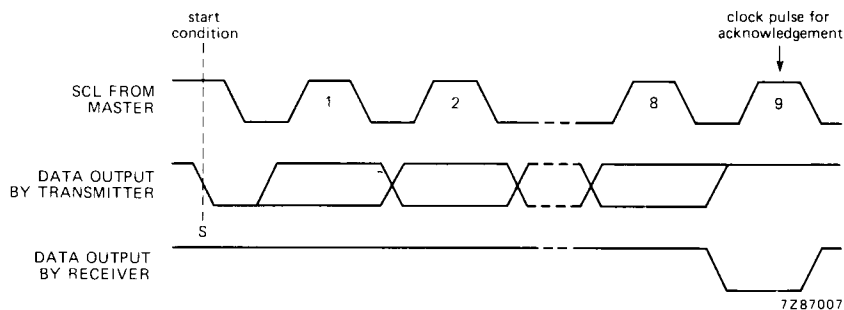


Fig.6 Acknowledgement on the I<sup>2</sup>C-bus.

128 × 8-bit/256 × 8-bit static RAMs  
with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

**Timing specifications**

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V<sub>IL</sub> and V<sub>IH</sub> with an input voltage swing of V<sub>SS</sub> to V<sub>DD</sub>.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f <sub>SCL</sub>	—	—	100	kHz
Tolerable spike width on bus	t <sub>SW</sub>	—	—	100	ns
Bus free time	t <sub>BUF</sub>	4.7	—	—	μs
Start condition set-up time	t <sub>SU; STA</sub>	4.7	—	—	μs
Start condition hold time	t <sub>HD; STA</sub>	4.0	—	—	μs
SCL LOW time	t <sub>LOW</sub>	4.7	—	—	μs
SCL HIGH time	t <sub>HIGH</sub>	4.0	—	—	μs
SCL and SDA rise time	t <sub>r</sub>	—	—	1.0	μs
SCL and SDA fall time	t <sub>f</sub>	—	—	0.3	μs
Data set-up time	t <sub>SU; DAT</sub>	250	—	—	ns
Data hold time	t <sub>HD; DAT</sub>	0	—	—	ns
SCL LOW to data out valid	t <sub>VD; DAT</sub>	—	—	3.4	μs
Stop condition set-up time	t <sub>SU; STO</sub>	4.0	—	—	μs

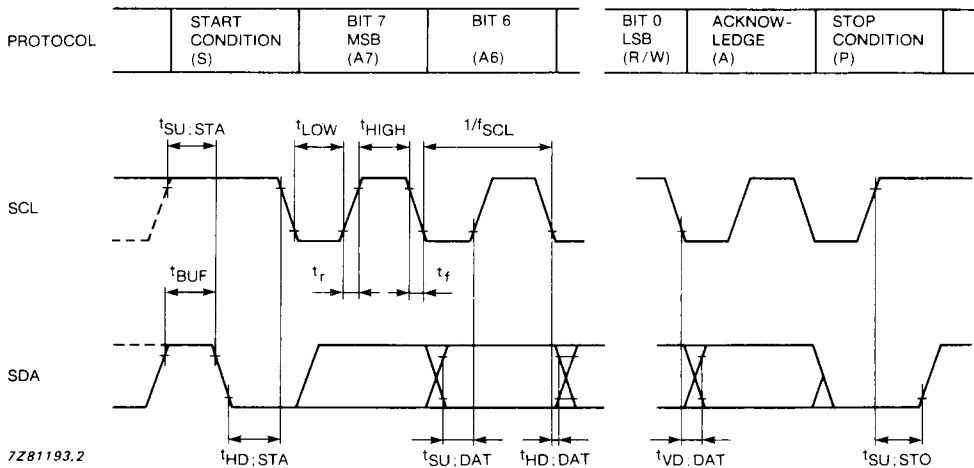


Fig.7 I<sup>2</sup>C-bus timing diagram.

128 × 8-bit/256 × 8-bit static RAMs  
with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

**Bus protocol**

Before any data is transmitted on the I<sup>2</sup>C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I<sup>2</sup>C-bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig.8.

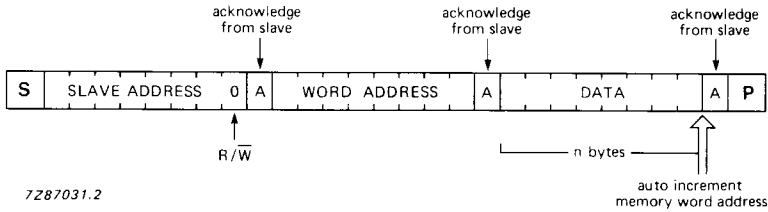


Fig.8(a) Master transmits to slave receiver (WRITE mode).

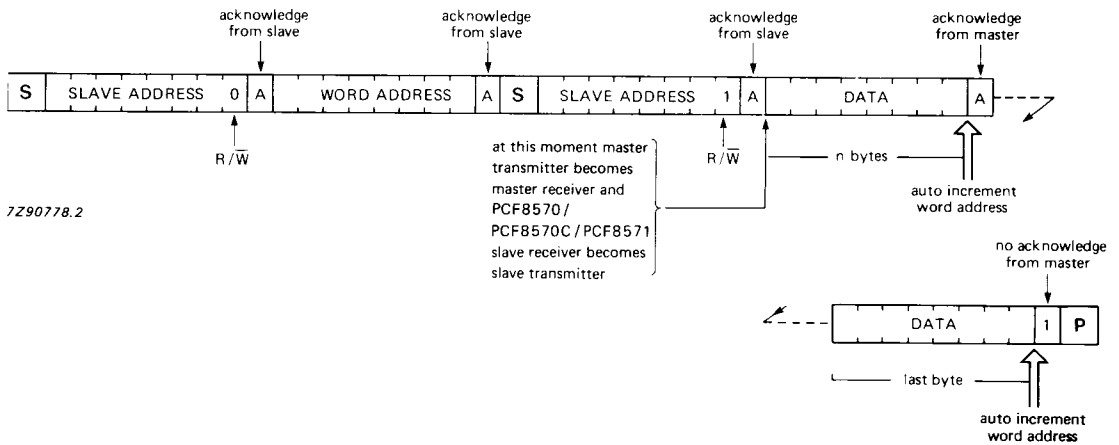


Fig.8(b) Master reads after setting word address (WRITE word address; READ data).

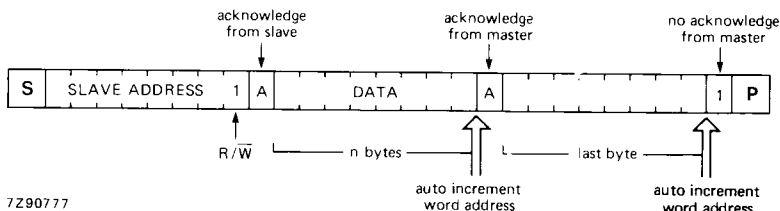


Fig.8(c) Master reads slave immediately after first byte (READ mode).

# 128 × 8-bit/256 × 8-bit static RAMs with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

## APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig.9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig.10).

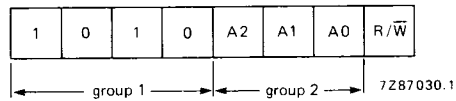


Fig.9 PCF8570 and PCF8571 address.

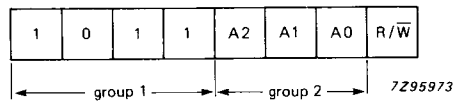


Fig.10 PCF8570C address.

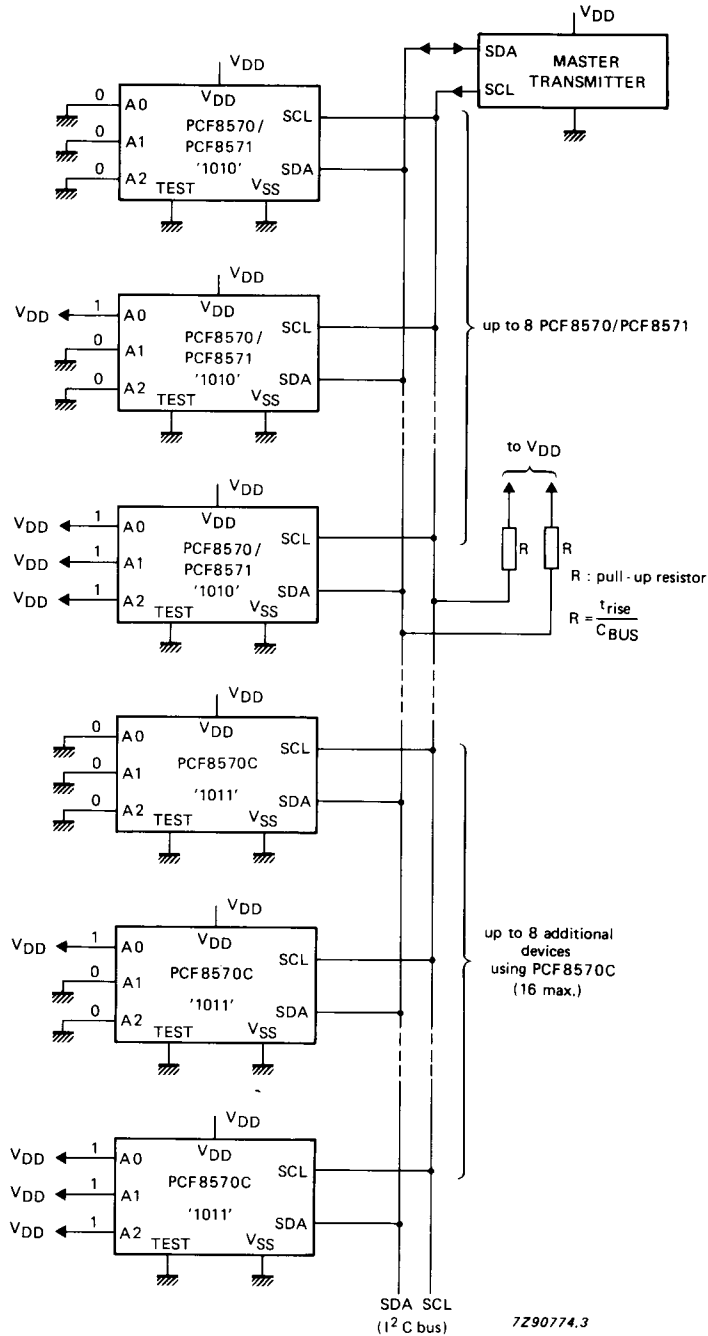
### Note

A0, A1, and A2 inputs must be connected to V<sub>DD</sub> or V<sub>SS</sub> but not left open-circuit.



128 × 8-bit/256 × 8-bit static RAMs  
with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571



It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V<sub>DD</sub> and V<sub>SS</sub>.

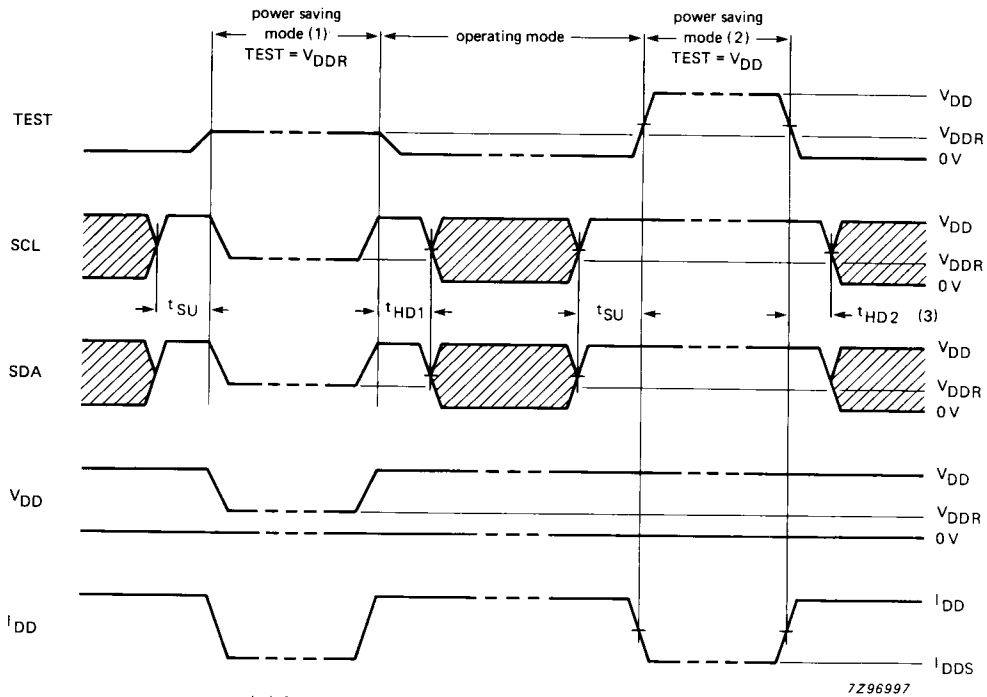
Fig.11 Application diagram.

128 × 8-bit/256 × 8-bit static RAMs  
with I<sup>2</sup>C-bus interface

PCF8570/8570C/8571

**POWER SAVING MODE**

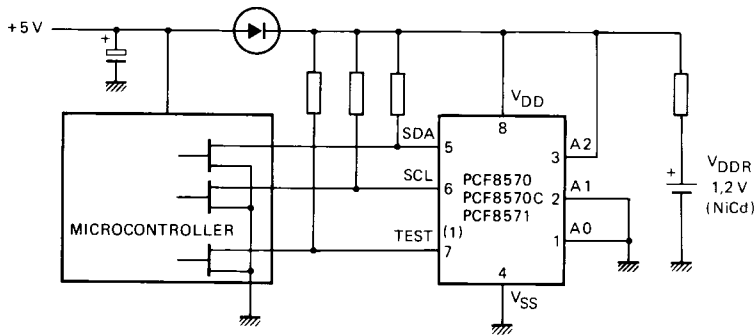
With the condition TEST = V<sub>DD</sub> or V<sub>DDR</sub> the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I<sup>2</sup>C-bus logic is reset.



7296997

- (1) Power saving mode without 5 V supply voltage.
- (2) Power saving mode with 5 V supply voltage.
- (3)  $t_{SU}$  and  $t_{HD1} \geq 4 \mu s$  and  $t_{HD2} \geq 50 \mu s$ .

Fig.12 Timing for power saving mode.



7290776.3

- (1) In the operating mode TEST = 0; In the power saving mode TEST = V<sub>DDR</sub>.

It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V<sub>DD</sub> and V<sub>SS</sub>.

Fig.13 Application example for power saving mode.

This datasheet has been downloaded from:

[www.DatasheetCatalog.com](http://www.DatasheetCatalog.com)

Datasheets for electronic components.