

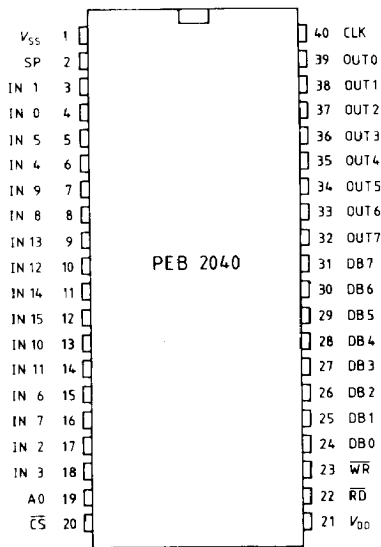
02 8262

PEB 2040 Memory Time Switch (MTS)

- Time/Space Switch for 2.048 MHz and 8.192 MHz PCM Systems
- Different Kinds of Operation Modes (2 Mbit/s, 8 Mbit/s or Mixed Mode)
- 16 Input PCM Lines and Speech Memory for all 512 Subscribers On-Chip
- Connection Memory for 256 Channels of 8 Output Lines On-Chip
- Non-Blocking Time Switch with 16/16 PCM Lines can be Built with Two Devices
- μ P-Interface for Writing and Reading the Connection Memory
- Delay Between Input and Output Lines Selectable
- Tristate for Further Expansion or Hot Standby
- Advanced NMOS Technology
- Single +5V Power Supply
- NMOS

Pin Configuration

(Top View)



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- All types of switching systems
- Complete switch in PCM PABX for up to 512 subscribers with only two devices
- Concentrator function
- Frequency-transforming interface between 2 MHz and 8 MHz PCM systems
- 16/16 space switch for 8 MHz PCM systems

The Siemens memory time switch PEB 2040 is a monolithic NMOS circuit with speech and connection memory on-chip. It connects any of 512 incoming PCM channels to any of 256 outgoing PCM channels. Two chips give a non-blocking 512 channel switch. Block diagrams of 2 PCM systems using the PEB 2040 are shown in Figure 1. Inputs and outputs are TTL-compatible.

Pin Definitions

Pin	Symbol	Function
1	V _{SS}	Ground (0V)
2	SP	Synchronous pulse (8 kHz); rising edge for input counter, falling edge for output counter; difference between rising and falling edge should be $\Delta = (2 + N \times 4) t_{CLK}$ ($N = 0 - 255$); rising edge synchronous with the incoming frames; output frame starts 2 clock pulses before the falling edge.
3	IN 1	PCM Input Port 1
4	IN 0	PCM Input Port 0
5	IN 5	PCM Input Port 5
6	IN 4	PCM Input Port 4
7	IN 9	PCM Input Port 9
8	IN 8	PCM Input Port 8
9	IN 13	PCM Input Port 13
10	IN 12	PCM Input Port 12
11	IN 14	PCM Input Port 14
12	IN 15	PCM Input Port 15
13	IN 10	PCM Input Port 10
14	IN 11	PCM Input Port 11
15	IN 6	PCM Input Port 6
16	IN 7	PCM Input Port 7
17	IN 2	PCM Input Port 2
18	IN 3	PCM Input Port 3
19	A 0*	Address 0, for separating different modes of the control words
20	\overline{CS}^*	Chip Select
21	V _{DD}	Supply Voltage +5V $\pm 5\%$
22	\overline{RD}^*	Read Pulse
23	\overline{WR}^*	Write Pulse
24	DB 0*	DATA Bus 0
25	DB 1*	DATA Bus 1
26	DB 2*	DATA Bus 2
27	DB 3*	DATA Bus 3
28	DB 4*	DATA Bus 4
29	DB 5*	DATA Bus 5
30	DB 6*	DATA Bus 6
31	DB 7*	DATA Bus 7
32	OUT 7	PCM Output Port 7
33	OUT 6	PCM Output Port 6
34	OUT 5	PCM Output Port 5
35	OUT 4	PCM Output Port 4
36	OUT 3	PCM Output Port 3
37	OUT 2	PCM Output Port 2
38	OUT 1	PCM Output Port 1
39	OUT 0	PCM Output Port 0
40	CLK	Clock pulse 8.192 MHz, duty cycle 50%

* μ P-controlled interface

Block Diagram of Two PCM Switch Configurations with PEB 2040

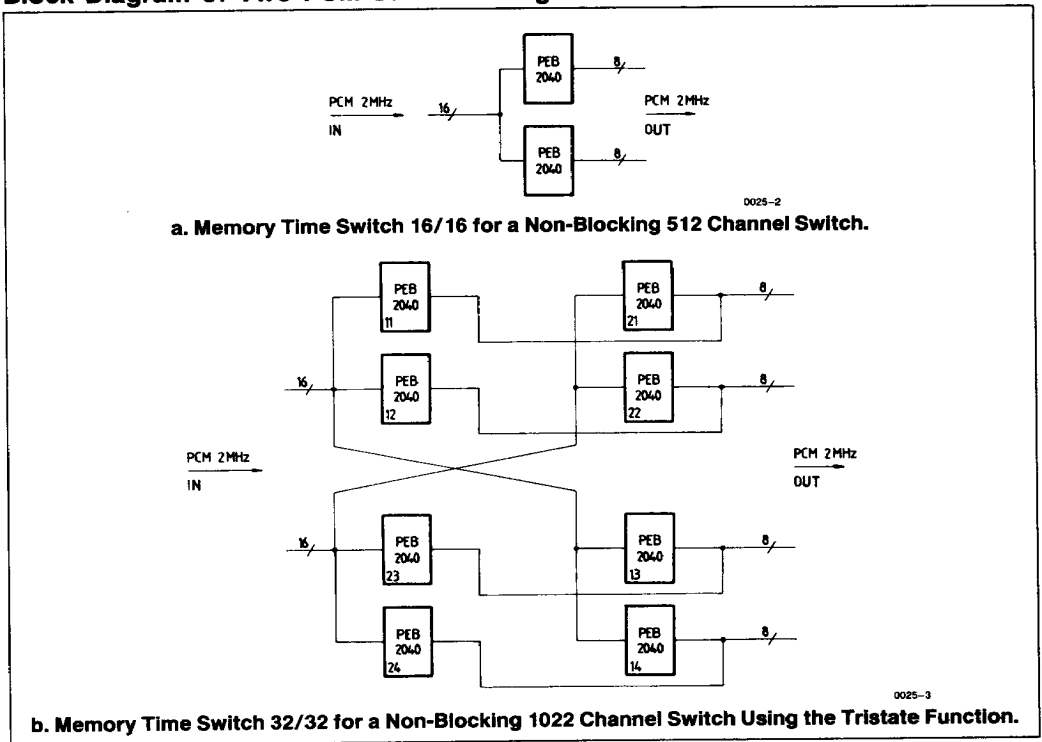


Figure 1 a. Non-Blocking 512 Channel Switch. b. Non-Blocking 1022 Channel Switch.

Functional Description of MTS 16/8

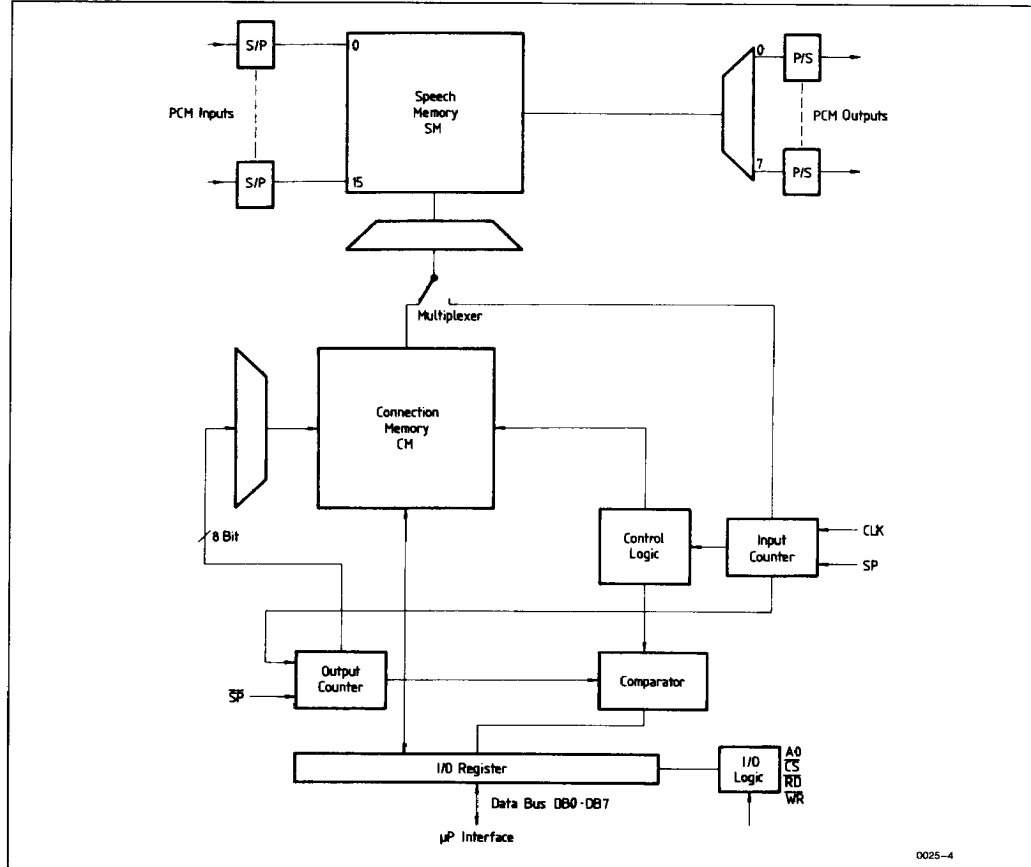
The PEB 2040 is a memory time switch module which has the ability to connect any of the 512 PCM channels of 16 incoming PCM lines to any of the 256 PCM channels of 8 output lines.

A block diagram of the main components is shown in Figure 2.

The PCM information of a complete frame is stored in the 4K speech memory SM. That means that all 512 8-bit words are written into a fixed position of

the SM. This is controlled by the input counter every 125 μ s. The words are read by a random access with an address that is stored in a connection memory CM for each of the 256 output channels. The access to the CM is controlled by the output counter.

To realize a connection the SM address and the CM address must be written into the PEB 2040 via a μ P interface. The SM address contains the time slots and line numbers of the incoming PCM words. The CM address consists of the time slots and line numbers of the output words.

Block Diagram**Figure 2**

Operation Modes

The PEB 2040 can be connected to 2.048 Mbit/s and 8.192 Mbit/s PCM lines. The operation mode is selected by the mode bits, where MI 0 and MI 1 define the bit rate of the input lines and, independently, MO 0 and MO 1 that of the output lines.

The corresponding input and output addresses are defined below. The mode MI 0 = MI 1 = 1 is only for space-switch application.

Input Configuration Table

Pin	MI 0 = 0, MI 1 = 0	MI 0 = 1, MI 1 = 0	MI 0 = 0, MI 1 = 1	MI 0 = 1, MI 1 = 1
	16 x 2 Mbit/s	4 x 8 Mbit/s	8 x 2 + 2 x 8 Mbit/s	16 x 8 Mbit/s
3	IN 1	IN 1 IN 0 IN 2 IN 3	IN 0	1
4	IN 0			0
5	IN 5			5
6	IN 4		IN 4	4
7	IN 9		IN 8	9
8	IN 8			8
9	IN 13		IN 12	13
10	IN 12		IN 14	12
11	IN 14		IN 3	14
12	IN 15			15
13	IN 10		IN 10	10
14	IN 11		IN 6	11
15	IN 6			6
16	IN 7		IN 2	7
17	IN 2			2
18	IN 3			3

Output Configuration

Pin	MO 0 = 0, MO 1 = 0	MO 0 = 1, MO 1 = 0	MO 0 = 0, MO 1 = 1
	8 x 2 Mbit/s	2 x 4 Mbit/s	8 x 2 + 4 x 2/1 x 8 Mbit/s
32	OUT 7	OUT 1 OUT 0	OUT 7
33	OUT 6		OUT 5
34	OUT 5		
35	OUT 4		OUT 3
36	OUT 3		
37	OUT 2		OUT 1
38	OUT 1		
39	OUT 0		
			OUT 0

PCM Interface

Control signals:

Clock: $\text{CLK } f_{\text{CLK}} = 8.192 \text{ MHz}$, $t_r, t_f \leq 10 \text{ ns}$

Synchronous pulse: $\text{SP } f_{\text{CLK}} = 8.000 \text{ kHz}$ defines the PCM frame with 1024 clock pulses $t_r, t_f \leq 10 \text{ ns}$

PCM input: $\text{IN } 0 - \text{IN } 15$

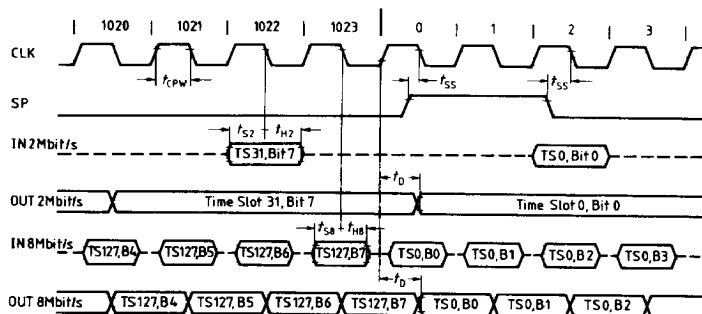
for 2 or 8 Mbit/s organized as 32 words of 8 bits or 128 words of 8 bits within a frame. The frame for all input lines starts with the rising edge of the SP signal.

PCM output: $\text{OUT } 0 - \text{OUT } 7$

for 2 or 8 Mbit/s. The frame for all output lines is controlled by the falling edge of the SP signal. The difference between the rising and the falling edge of the SP signal should be $\Delta = (2 + N \times 4) t_{\text{CLK}}$, $0 \leq 255$ (fixed at space switch application: $\Delta = (2 + 70 \times 4) t_{\text{CLK}} = 282 t_{\text{CLK}}$, $N = 70$). N defines the delay of the output frame counted in 2 MHz bit steps relative to the input frame, as shown in the timing diagram.

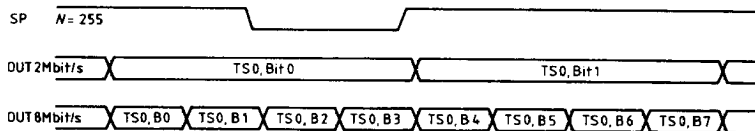
The outputs have tristate capability.

MTS 16/8 Timing Diagram



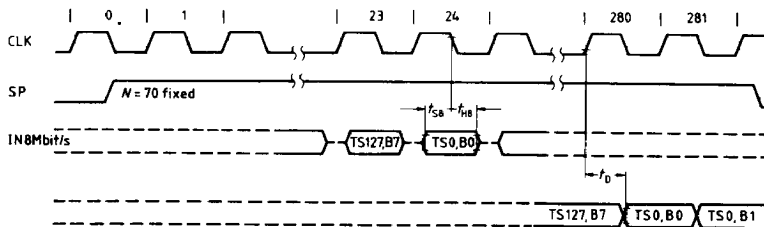
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Example with Delayed Output Frame



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Space Switch Application



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Timing with $f_{CLK} = 8.192 \text{ MHz}$

Symbol	Min	Max	Units
t _{SS}	15	105	ns
t _{S2}	5		ns
t _{H2}	30		ns
t _{S8}	5		ns
t _{H8}	39		ns
t _D		40	ns

at $C_L = 200 \text{ pF}$

μP interface DB0 – DB 7, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$, A0

Commands for access to the connection memory, selected by A 0 = 1.

All commands have a three-byte structure and must be executed completely.

Clock Timing

Symbol	Min	Max	Units
t _{CLK}	120		ns
t _r , t _f		10	ns
t _{CPW}	57	t _{CLK} – 57	ns
t _{CDC}	48	55	%

DB 7

DB 0

X	X	K1	K0	X	X	X	S8	Key word
S7	S6	S5	S4	S3	S2	S1	S0	Speech Memory Address
C7	C6	C5	C4	C3	C2	C1	C0	Connection Memory Address

Keyword	
K1	K0
1	0
0	1
0	0

Write connection memory
Write connection memory, with check bytes
Read connection memory

S8	S7	S6	S5	S4	S3	S2	S1	S0
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Speech memory address, stored in the connection memory

C7	C6	C5	C4	C3	C2	C1	C0
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Connection memory address

The speech memory address contains the time slots and line numbers of the incoming PCM words. The connection memory address consists of the time slots and line numbers of the output words with the following coordination.

2 Mbit/s input lines bit 0 to 3 line number
 bit 4 to 8 time slot number

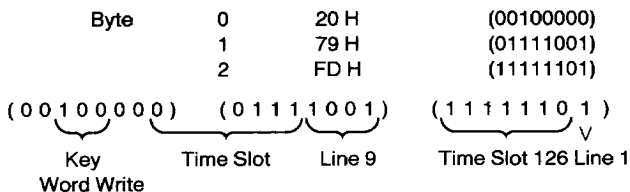
8 Mbit/s input lines bit 0 to 1 line number
 bit 2 to 8 time slot number

2 Mbit/s output lines bit 0 to 2 line number
 bit 3 to 7 time slot number

8 Mbit/s output lines bit 0 line number
 bit 1 to 7 time slot number

Example

Time slot 7 of the coming 2 Mbit/s line no. 9 shall be switched to time slot 126 of the output line no. 1 of an 8 Mbit/s system without check byte:



For Space-Switch Application with MI 0 = 1, MI 1 = 1; MO 0 = 1, MO 1 = 0

8 Mbit/s input lines bit 0 to 3 line number
 bit 4 to 8 the lower 5 bits of the time slot number
 8 Mbit/s output lines bit 0 line number
 bit 1 to 7 time slot number

The difference between the rising and the falling edge of the SP is fixed:

$$N = 70, \Delta = (2 + 70 \times 4) t_{CLK} = 282 t_{CLK}$$

The selection of 128 input time slots is possible by writing the connection memory (CM) as shown below.

In CM address 00–3F → S8–S4 (SM addr.) means TS 0–TS 31
 In CM address 40–7F → S8–S4 (SM addr.) means TS 32–TS 63
 In CM address 80–BF → S8–S4 (SM addr.) means TS 64–TS 95
 In CM address C0–FF → S8–S4 (SM addr.) means TS 96–TS 127

3 Examples:

	C7	C0	
CM address = 3F	00111111		output line 1, TS 31
SM address = 1 FA	111111010		input line 10, TS 31
	S8	S0	
	C7	C0	
CM address = 7F	01111111		output line 1, TS 31
SM address = 1 FA	111111010		input line 10, TS 63
	S8	S0	
	C7	C0	
CM address = C0	11000000		output line 0, TS 96
SM address = 008	000001000		input line 8, TS 96
	S8	S0	

Write Connection Memory

X	X	1	0	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

$A0 = 1, \overline{WR} = 0, \overline{CS} = 0$

Stores S8–S0 into the connection memory addressed with C7–C0.

Write Connection Memory with check bytes desired

X	X	0	1	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

$A0 = 1, \overline{WR} = 0, \overline{CS} = 0$

Stores S8–S0 into the connection memory addressed with C7–C0.

X	X	0	1	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

$A0 = 1, \overline{RD} = 0, \overline{CS} = 0$

S8–S0 have been overwritten by the connection memory in the next frame after writing the connection memory.

Read Connection Memory

X	X	0	0	X	X	X	X
X	X	X	X	X	X	X	X
C7	C6	C5	C4	C3	C2	C1	C0

$A0 = 1, \overline{WR} = 0, \overline{CS} = 0$

Overwrites S8–S0 with the connection memory address C7–C0, and can be read with the following sequence.

X	X	0	0	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	S0
C7	C6	C5	C4	C3	C2	C1	C0

$A0 = 1, \overline{RD} = 0, \overline{CS} = 0$

Mode/Status selected A0 = 0**Status** A0 = 0, \overline{RD} = 0, (\overline{WR} = 1), \overline{CS} = 0

DB7				DB0			
B	Z	X	RY	0	0	0	0

B = 1 Chip busy during command execution

Z = 1 Incomplete command instruction

RY = 1 Mode register blocked (after power-on)

Power-on Tristate

SB is set by power-on or by write mode register.

SB is reset by write mode register.

Write mode register is blocked at most seven frames after power-on

During that time RY in the status register is set to 1 SP and CLK should be applied immediately after power-on.

Mode A0 = 0, \overline{WR} = 0, (\overline{RD} = 1), \overline{CS} = 0

DB7				DB0			
R	TE	0	SB	MI 1	MI 0	MO 1	MO 0

R = Reset

R = 0 Reset

TE = Tristate enable

TE = 0 Mode without Tristate function

TE = 1 Tristate dependent on code

SB = Standby

SB = 1 Tristate independent from code

MI 1	MI 0	Input Operation Mode
0	0	16 x 2 Mbit/s
0	1	4 x 8 Mbit/s
1	0	2 x 8 + 8 x 2 Mbit/s

1	1	16 x 8 Mbit/s
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MO 1	MO 0	Output Operation Mode
0	0	8 x 2 Mbit/s
0	1	2 x 8 Mbit/s
1	0	1 x 8 / 4 x 2 Mbit/s

0	1	2 x 8 Mbit/s
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for space-switch application only

Reset

DB 7 = R

The PEB 2040 can be initialized by a mode byte with R = 0. This causes the complete connection memory to be overwritten with zeros. During this time the busy bit is set.

Tristate

DB 6 = TE, DB 4 = SB

The PCM outputs of the PEB 2040 have tristate capability.

1. SB = 1, is a standby mode. All outputs are tristated. The connection memory works in the normal mode.

The chip can be activated immediately by setting SB = 0.

2. TE = 1, (SB = 0): The output channels are tristated, if the speech memory address stored in the connection memory is S8 - S0 = 0. This means that time slot 0 of line 0 is not available for any output.

3. TE = 0, (SB = 0): Time slot 0 of line 0 is available, but tristate is not possible.

Operation Mode (input/output bit rate)

DB 0 = MO 0, DB 1 = MO 1, DB 2 = MI 0,
DB 3 = MI 1

The operation mode is selected by the mode bits, where MI 0 and MI 1 defines the bit rate of the input lines and, independently, MO 0 and MO 1 that of the output lines.

The corresponding input and output addresses are given in Table 1.

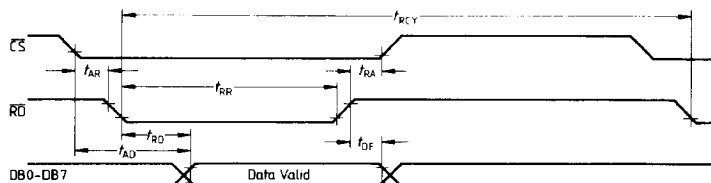
Example:

DB7				DB0			
1	1	0	0	0	0	0	0

PCM mode: 16 x 2 Mbit/s input
PCM mode: 8 x 2 Mbit/s output
with tristate

Timing of μ P Interface

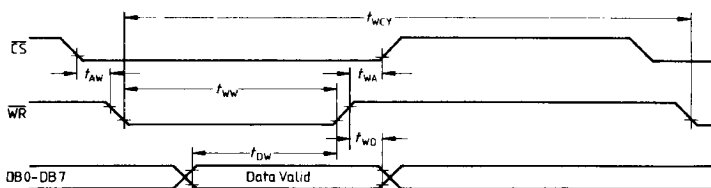
Read Operation



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Parameter	Symbol	Min	Max	Units
Address Stable before \overline{RD}	t_{AR}	0		ns
Address Hold after \overline{RD}	t_{RA}	0		ns
\overline{RD} Width	t_{RR}	180		ns
\overline{RD} to Data Valid	t_{RD}		90	ns
Address Stable to Data Valid	t_{AD}		100	ns
Data Float after \overline{RD}	t_{DF}	10	100	ns
\overline{RD} Cycle Time	t_{RCY}	500		ns

Write Operation



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Parameter	Symbol	Min	Max	Units
Address Stable before \overline{WR}	t_{AW}	0		ns
Address Hold Time	t_{WA}	0		ns
\overline{WR} Width	t_{WW}	190		ns
Data Setup Time	t_{DW}	130		ns
Data Hold Time	t_{WD}	0		ns
\overline{WR} Cycle Time	t_{WCY}	500		ns

The "busy time" during which a command or reset instruction is executed has to be programmed with its maximum length or must be controlled via the busy bit of the status register.

Busy Time

Parameter	Average	Max	Units
Reset	188	250	μ s
Read Connection Memory	63	125	μ s
Write Connection Memory	63	125	μ s
Write Connection Memory with Check Bytes Desired	188	250	μ s

Absolute Maximum Ratings*

Supply Voltage (V_{DD}) -0.3V to +7V
 Input Voltage (V_I) -0.3V to +7V
 Total Power Dissipation (P_{tot}) 1W
 Output Power Dissipation (P_O) +10 mW
 Operating Temperature (T_A) -0°C to +70°C
 Storage Temperature (T_{stg}) -55°C to +125°C

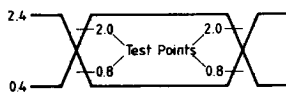
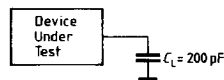
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and Operating Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$)

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Supply Current	I_{DD}		60	150	mA
Input Leakage Current, $V_I = 0$ to V_{DD}	I_{IL}	-10		10	μA
H Input Voltage	V_{IH}	2.0		V_{DD}	V
L Input Voltage	V_{IL}	0		0.8	V
H Output Voltage ($I_O = -0.2$ mA)	V_{OH}	2.4			V
L Output Voltage ($I_O = 2.0$ mA)	V_{OL}			0.4	V
Tristate Output Leakage $V_O = 0$ to V_{DD}	I_{OL}	-10		10	μA

Capacitance ($T_A = +25^\circ\text{C}$; $V_{CC} = \text{GND} = 0V$)

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Input Capacitance	C_{IN}	$f_c = 1$ MHz		5	10	pF
Input/Output Capacitance	$C_{I/O}$			10	20	pF
Output Capacitance	C_{OUT}	Unmeasured Pins Returned to GND		8	15	pF

AC Testing Input, Output Waveform**AC Testing Load Circuit****AC Testing**

Inputs are driven at 2.4V for a logic "1" and at 0.4V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and at 0.8V for a logic "0".

Ordering Information

Type	Package
PEB 2040	DIC 40