LSI/CSI
Manufacturers of Custom and Standard LSI Circuits
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RDD104

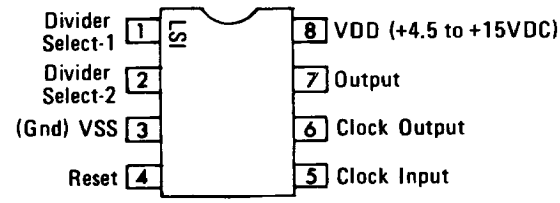
Revised July 1989

SELECTABLE 4 DECADE CMOS DIVIDER

FEATURES:

- Selectable Divide by 10, 100, 1000 or 10,000
- Clock Input Shaping Network Accepts Fast or Slow Edge Inputs
- Active Oscillator Network for External Crystal
- Square Wave Output
- Output-TTL Compatible at +4.5 Volt Operation
- High Noise Immunity
- Reset
- All Inputs Protected
- +4.5 to +15 Volt Operation
- Low Power Dissipation

Pin Connections RDD104:



TOP VIEW
Standard 8 Pin Plastic Mini-DIP
Figure 1

DESCRIPTION OF OPERATION:

The RDD104 is a monolithic CMOS (Complementary MOS) four decade divider circuit that advances on each negative transition of the input clock pulse. When the reset input is high the circuit is cleared to zero. The clock input is applied to a three stage amplifier network whose output is brought out so that an external crystal network can be used to form an oscillator circuit. If the clock output is not used, the amplifier acts as an input buffer. Two select inputs are provided which enables the circuit to divide by 10, 100, 1000, or 10,000.

The divider range is selected according to the following truth table:

DIVIDER SELECT INPUTS		OUTPUT DIVISION
SELECT 2 (Pin 2)	SELECT 1 (Pin 1)	
0	0	10,000
0	1	1,000
1	0	100
1	1	10

MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Temperature	T_A	−40 to +85	°C
DC Supply Voltage	V_{DD}	+18 to −0.5	VDC
Input Voltage	V_{IN}	V_{DD} to V_{SS}	VDC

D.C. ELECTRICAL CHARACTERISTICS:

(V_{SS} = 0 Volts, C Load = 50pF) Input rise and fall times = 20ns except for clock

	V_{DD}	TEMPERATURE (°C)			UNITS
		−40	+25	+85	
Quiescent Device Current	4.5V	10	10	300	μA Max
	10V	20	20	600	μA Max
Output Voltage, Low Level	4.5V	.01	.01	.05	V Min
	10V	.01	.01	.05	V Min
High Level	4.5V	4.49	4.49	4.45	V Max
	10V	9.99	9.99	9.95	V Max
Input Noise Immunity (Low and High)	4.5V	1.3	1.3	1.3	V Min
	10V	3.0	3.0	3.0	V Min
Output Drive Current N Channel Sink Current (V_{OUT}=V_{SS}+.4V)	4.5V	2.3	1.9	1.6	mA Min
	10V	5.0	4.0	3.5	mA Min
P Channel Source Current (V_{OUT} = V_{DD} − 1V)	4.5V	1.1	.95	.8	mA Min
	10V	2.5	2.1	1.8	mA Min
Input Capacitance (any input)			5.0		pF Max

DYNAMIC ELECTRICAL CHARACTERISTICS:

(C Load = 50pF, Input Rise and Fall Times = 20ns Except for Clock)

	V_{DD}	MIN	TYP	MAX	Units
Clock Input Frequency	4.5V	DC		1.5	MHz
	10V	DC		4.0	MHz
	15V	DC		6.0	MHz
Clock Input Rise and Fall Times	4.5 to 15V		No Limit		
Clock Output Rise and Fall Time CL=15pF	4.5V			140	ns
	10V			70	ns
Clock Output Propagation Delay CL=15pF	4.5V			300	ns
	10V			150	ns
Output Rise & Fall Times	4.5V			400	ns
	10V			200	ns
Propagation Delay to Output	4.5V			1500	ns
	10V			750	ns
Reset Pulse Width	4.5V	800			ns
	10V	400			ns
Reset Removal Time	4.5V			500	ns
	10V			250	ns
Reset Propagation Delay to Output	4.5V			1400	ns
	10V			700	ns
Select Input Setup Time	4.5V			800	ns
	10V			400	ns

Minimum Part Oscillator Circuit

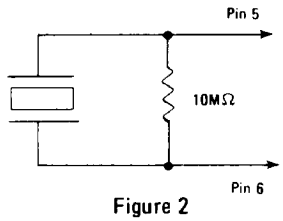


Figure 2

Typical Oscillator Circuit 1 MHz and Below with Trim

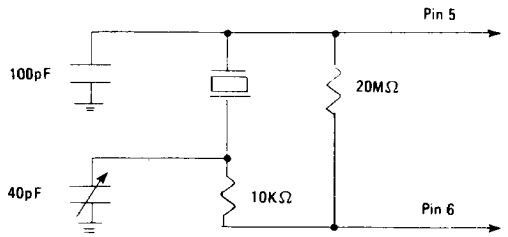


Figure 3

Typical Oscillator Circuit Above 1 MHz with Trim

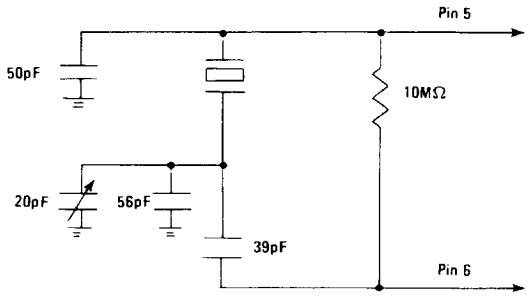


Figure 4

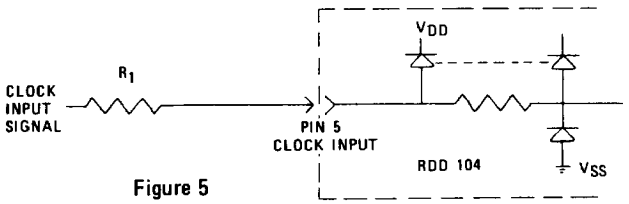


Figure 5

TYPICAL INPUT

If input signals are less than V_{SS} or greater than V_{DD}, a series input resistor, R1, should be used to limit the maximum input current to 2 milliamperes.

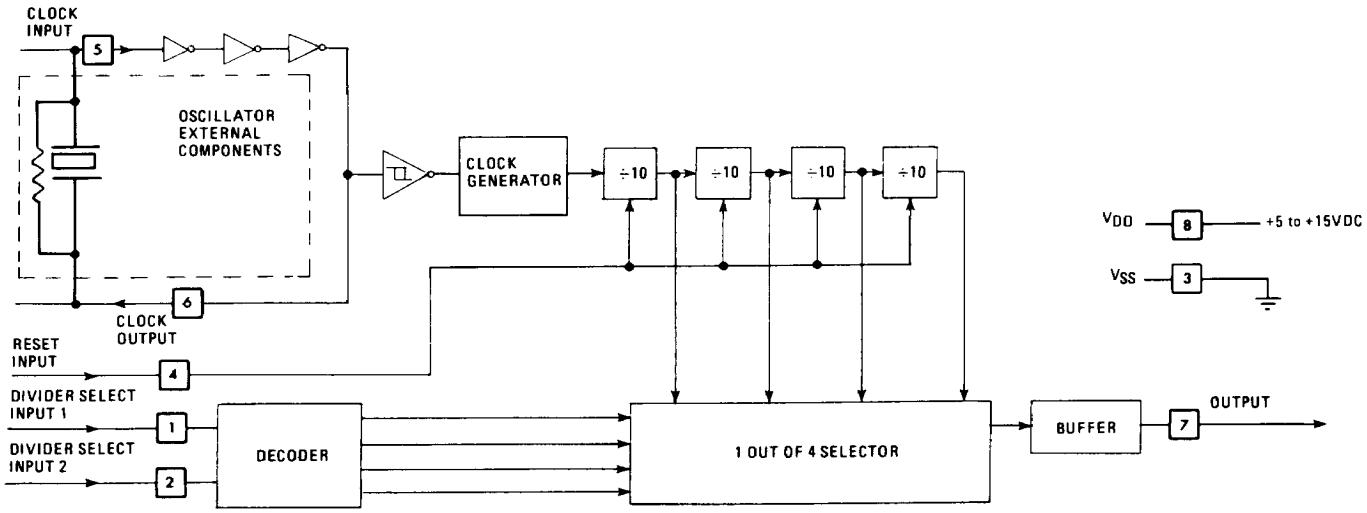


Figure 6 RDD104 BLOCK DIAGRAM