S-VHS digital Secam decoder (SDSD) SAA9056

GENERAL DESCRIPTION

The SAA9056 is designed to provide colour difference signals for a digital TV signal processing system.

Features

- Phase-linear chrominance bandpass filter for cross-colour improvement
- Programmable filter characteristics for optimum adaption for different IF stages
- Recursive "Cloche" (Bell) filter
- Zero-crossing detection, FM demodulator with high AM rejection
- One demodulator for both carrier frequencies
- Base-band signal adjustment in gain and offset
- De-emphasis with recursive filter structure
- Line delay and cross-over switch for colour difference signals
- Output multiplexer for the UV format of the Digital Multistandard Secam Decoder
- Standard identification circuit with programmable sensitivity
- Programmable I^2C-bus address

PACKAGE OUTLINE

28-lead DIL; plastic (SOT117).

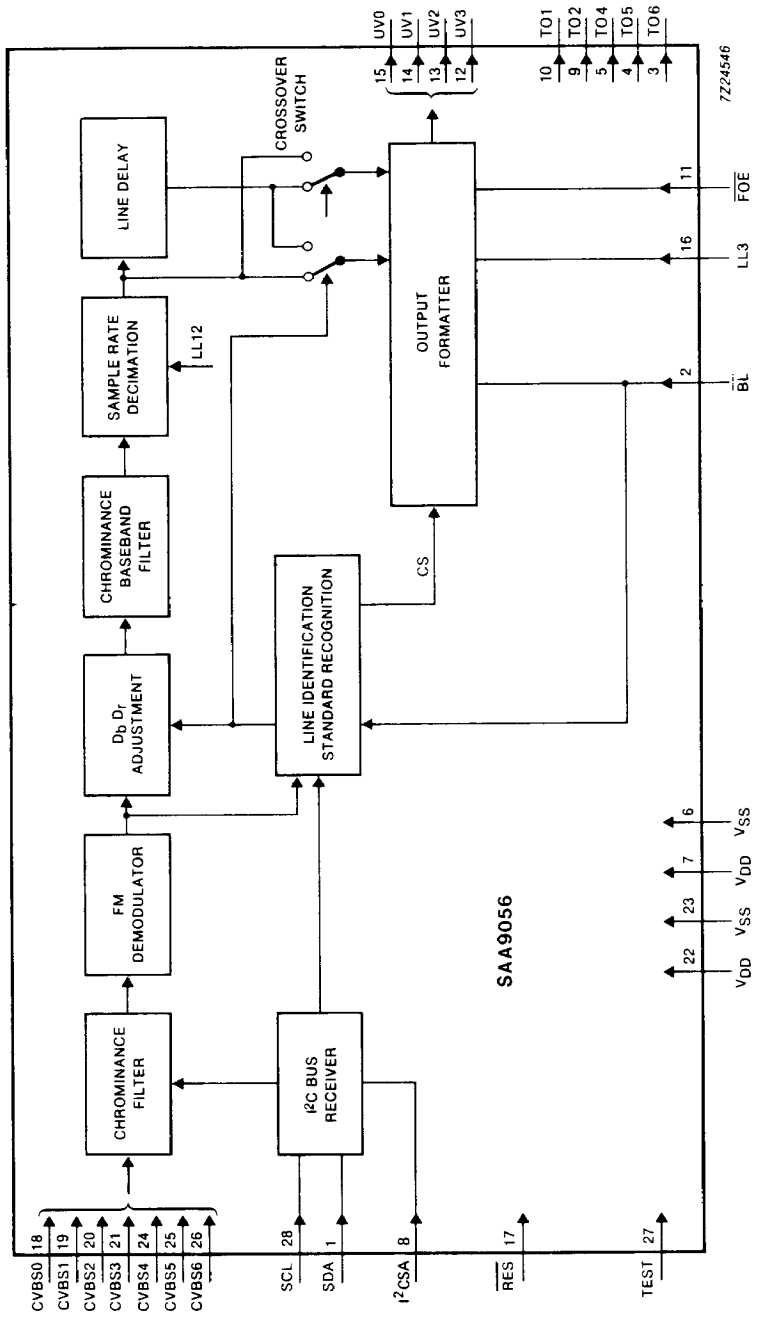


Fig. 1 Block diagram.

PINNING

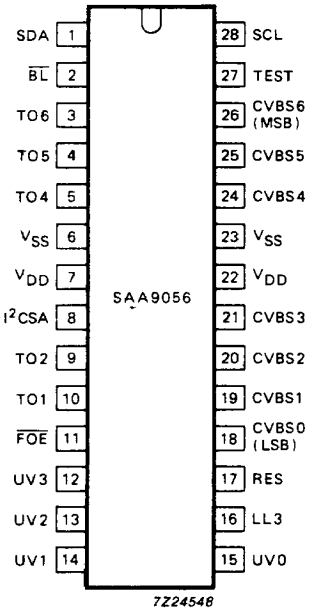


Fig.2 Pinning diagram.

1	SDA	I^2C-bus serial data input, receive only, no data is transmitted from the SDSD
2	$\overline{BL}$	This signal from the digital multistandard decoder indicates the active video and line blanking period
3	TO6	Test output pin, used during test mode only. Do not connect this pin
4	TO5	As pin 3
5	TO4	As pin 3
6	V_{SS}	Ground
7	V_{DD}	+ 5 V supply
8	I^2CSA	I^2C-bus select address. Input to select two different I^2C-bus slave addresses
9	TO2	As pin 3
10	TO1	As pin 3
11	$\overline{FOE}$	Fast output enable signal, forces the UV-outputs to High-Z state
12	UV3	UV colour difference signals, via this port the decoded colour difference signals are transmitted to the DMSD in a mixed parallel/serial format. Additionally the status flag CS (colour in SECAM detected) is encoded in the UV data stream. The output drivers can be set to high impedance (3-state) via the I^2C-bus.
13	UV2	As pin 12
14	UV1	As pin 12
15	UV0	As pin 12
16	LL3	LL3 is the line-locked system clock at 13.5 MHz
17	$\overline{RES}$	The reset signal (active LOW) disables the UV buffers. Minimum LOW-time on this input = 10 LL3-cycles
18	CVBS0	Composite video, blanking and synchronization (LSB) input
19	CVBS1	As pin 18
20	CVBS2	As pin 18
21	CVBS3	As pin 18
22	V_{DD}	As pin 7
23	V_{SS}	As pin 6
24	CVBS4	Composite video, blanking and synchronization
25	CVBS5	As pin 24
26	CVBS6	As pin 24 (MSB)
27	TEST	This signal (active HIGH) enables the scan test mode
28	SCL	I^2C-bus serial clock input

FUNCTIONAL DESCRIPTION

The S-VHS Digital SECAM Decoder (SDSD) forms an integral part of a digital TV signal processing system. The system incorporates a Video Processor and Input Selector (TDA9045), an A/D Converter (SAA9079), a Sample Rate Converter (SAA9058), a Digital Multi-Standard Decoder with separate chrominance and luminance input (SAA9051), a Digital Deflection Controller (SAA9062/3/4)*, a Clock Generator Circuit (SAA9057), a Video Processor with DACs (SAA9060), a Colour Transient Improvement Circuit (TDA4565), a Video Control Combination Circuit (TDA4580), and an Octuple 6-bit DAC and a Feature Box. Figure 9 illustrates the timing of the input and output signals relative to the input clock (LL3).

The S-DMSD (SAA9051) decodes and demodulates the colour information from all TV standards which employ a quadrature modulated colour carrier. The S-DMSD also processes the luminance and synchronization signals and generates auxiliary signals.

The SDSD separates the colour information which it demodulates and decodes to provide the colour difference signals. These signals are subsequently encoded to produce a serial/parallel data stream at the UV outputs. Figure 4 illustrates the formatting and timing of the UV output port.

To enable other sources (eg PIP-CO) to access the digital YUV-bus, a fast output enable signal ($\overline{FOE}$) is provided. Two LL3-cycles after the $\overline{FOE}$ becomes inactive (HIGH), the UV output port of the SDSD is forced to the High-Z state. When the $\overline{FOE}$ signal is active (LOW) again, it needs two LL3-cycles and the UV output port of the SDSD becomes active (see Fig.4).

The chrominance bandpass filter for separating the frequency modulated colour carrier consists of several phase-linear FIR filters which improve the cross-colour behaviour. The non-linear phase (Bell) filter has a recursive structure (IIR filter). Figure 3 illustrates the frequency response of the chrominance band-pass filter and Bell filter. One of the FIR filters can be programmed via the I^2C-bus to provide optimal adaption for the various IF stages. Different responses can be selected by means of a 7-bit control word. Figure 8 illustrates some examples of frequency responses of the programmable adaptive filer.

Only one FM demodulator is used to demodulate the chrominance signal; this accomodates both carrier frequencies regardless of the centre frequency. It is a zero-crossing demodulator with a real time divider which is a pipeline structure. After demodulation the baseband signal is adjusted, line sequentially, to the appropriate colour difference signal. During the clamping period, the demodulated reference carrier is compared with the previous reference signal by the line identification circuit. The identification circuit compares the phase of the two demodulated burst signals and, if the phase relationship is incorrect for several lines (not SECAM), the CS flag (colour in SECAM) will be reset.

The baseband filter consists of a linear phase low-pass filter together with a de-emphasis filter with a recursive structure. Figure 5 illustartes the frequency response of the de-emphasis and band-pass filters for the colour difference signals. After filtering, the sample rate is reduced to a quarter (LL12 = 3.375 MHz). The word length is truncated to seven bits. The resultant signal is delayed by one line period (64 μs = 216 clock periods of 3.375 MHz). The signals, delayed and non-delayed, can be switched either directly or cross-wise to two different outputs which correspond to the colour difference signals.

The cross-over switch is controlled by the line identification circuit. At the end of the chrominance path an output formatter transforms the 14 bits (2 x 7 bits clocked by 3.375 MHz) to a 4-bit wide channel which is clocked by 13.5 MHz (LL3). The bits are separated into odd and even and then serialized.

* The digital TV signal processing system has the option of using one of three Digital Deflection Controllers (SAA9062/3/4). The choice of DDC is dependent on the format of the CRT and the line/field frequency.

The format for the UV output is the same as that of the UV I/O port in the S-DMSD (SAA9051). The timing multiplexer is controlled by the external signal $\overline{BL}$ from the S-DMSD. Signal $\overline{BL}$ is also used as a line-locked synchronization signal to generate several internal burst gate pulses.

The CS flag is transmitted via the chrominance data-stream because the SDSD has no I^2C-bus transmitter. The CS bit is read once per line by the S-DMSD at LL3 clock cycle number 748 (see Fig.6). If no SECAM colour is detected the UV port will be set to zero. After reset the UV lines will be set to high impedance (3-state) and the SDSD must be re-initialized via the I^2C-bus to enable further operation.

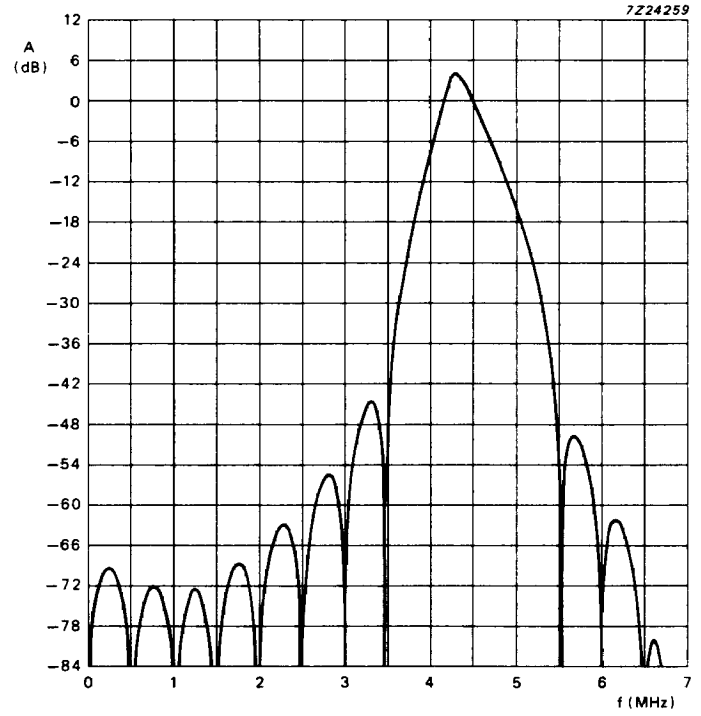


Fig. 3 Frequency response of chrominance bandpass and Bell filter.

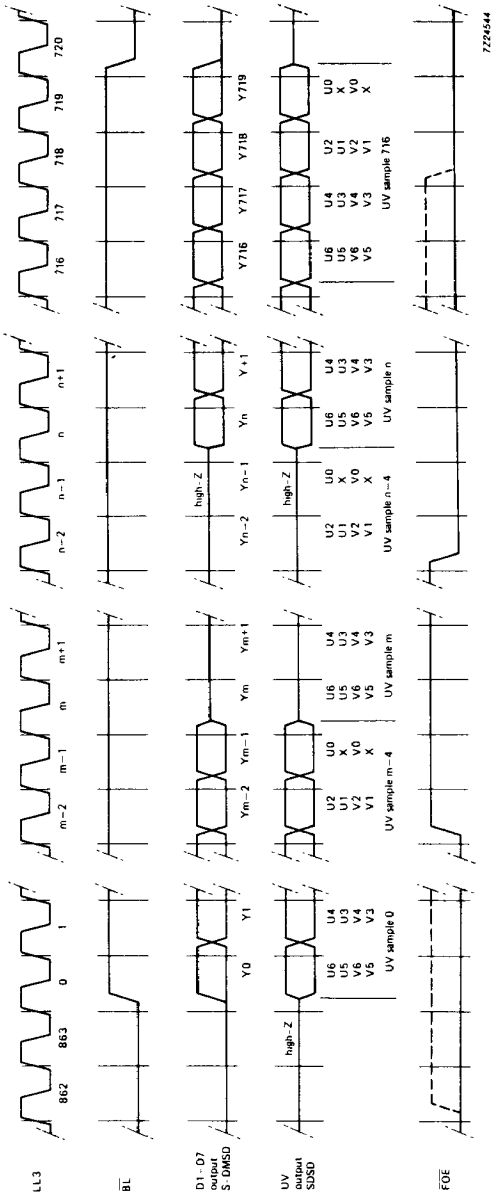


Fig.4 Timing of $\overline{FOE}$ signal.

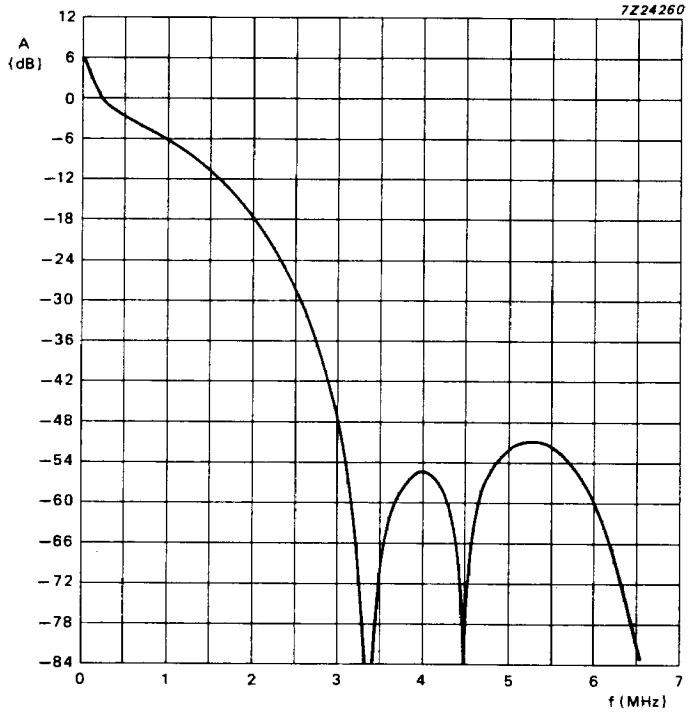
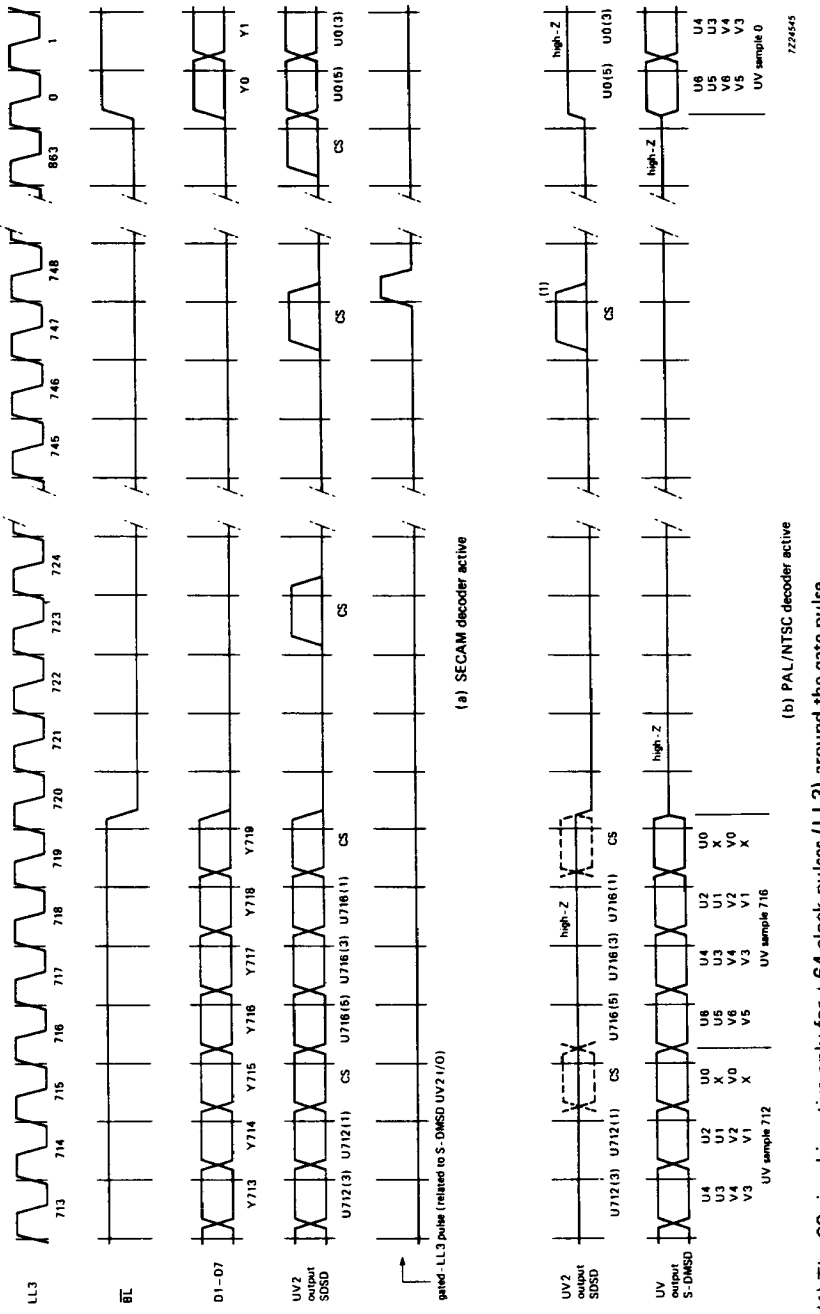


Fig. 5 Frequency response of the de-emphasis and base-band filter for the colour difference signals.



(1) The CS signal is active only for ± 64 clock pulses (LL3) around the gate pulse.

Fig.6 Position of CS signal read by S-DMSD.

I²C-BUS PROTOCOL

Slave receiver organization

Two different slave addresses are programmable with the I²CSA input at pin 8

I²CSA	slave receiver addresses							
	A6	A5	A4	A3	A2	A1	A0	*)
0 or unconnected	1	0	0	0	1	0	1	0 (bin) = 8A (hex)
1	1	0	0	0	1	1	1	0 (bin) = 8E (hex)

*) 0 = receiver mode

Fig. 7 Slave receiver format.

Table 1 Subaddress definition

register function	subaddress (HEX)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Main counter start address	10	MA1	MA0	X	DT4	DT3	DT2	DT1	DT0
(MA9.....MA0)	11	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2
Burst gate begin	12	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Burst gate end	13	BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0
Standard recognition sensitivity	14	R7	R6	R5	R4	R3	R2	R1	R0
Programmable adaptive filter	15	X	P6	P5	P4	P3	P2	P1	P0
Control register	16	X	X	X	X	X	C2	C1	C0
Reserved	17–1F	X	X	X	X	X	X	X	X

Notes to Table 1

1. The subaddress is automatically incremented to enable quick initialization by the I²C-bus controller within one transmission.
2. All eight bits of the subaddress are decoded by the device.
3. The subaddresses shown are acknowledged by the device. Subaddresses 00 to 0F (reserved for the Digital Multi-Standard Decoder) are not acknowledged. The subaddress counter wraps-around from 1F to 00. Subaddresses 20 to FF are not allowed.
4. X = don't care.
5. After power-on-reset the control register (subaddress 16) is set to logic 0, all other registers are undefined.

Subaddress 10 and 11 (HEX)

Main counter start address.

Application dependent.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
0	1	1	1	1	1	1	1	1	1	+511	outside central counter range
—										—	
—										—	
—										—	
—										—	
0	1	1	0	1	0	0	0	1	0	+418	
0	1	1	0	1	0	0	0	0	1	+417	417 x 74 ns ≈ +31 μs (maximum positive value)
—										—	
—										—	
—										—	
0	0	0	0	0	0	0	0	0	1	+1	+74 ns
0	0	0	0	0	0	0	0	0	0	0	reference point*

* Reference point position to be fixed.

MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	delay time	
1	1	1	1	1	1	1	1	1	1	−1	−74 ns
—										—	
—										—	
—										—	
1	0	0	1	0	0	0	0	1	0	−446	−446 x 74 ns ≈ −33 μs (maximum negative value)
1	0	0	1	0	0	0	0	0	1	−447	outside central counter range
—										—	
—										—	
—										—	
—										—	
1	0	0	0	0	0	0	0	0	0	−512	

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Internal counter range: −446 to + 417

Subaddress 12 (HEX)

Burst gate begin (start time)

Application dependent.

BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	1	1	74 ns
–	–	–	–	–	–	–	–	–	
–	–	–	–	–	–	–	–	–	
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

Subaddress 13 (HEX)

Burst gate end (stop time)

Application dependent.

BE7	BE6	BE5	BE4	BE3	BE2	BE1	BE0	dec	delay time
0	0	0	0	0	0	0	0	0	zero reference point
0	0	0	0	0	0	0	0	1	74 ns
–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–
1	1	1	1	1	1	1	1	255	18.89 μs

$$\text{Stepsize} = \frac{1}{13.5\ \text{MHz}} = 74\ \text{ns}$$

The stop time must be greater than the start time.

The reference point position of the burst gate start/stop time is identical with the main counter zero position.

Subaddress 14 (HEX)

Standard recognition sensitivity

Application dependent

R7	R6	R5	R4	R3	R2	R1	R0	function
								relationship between the number of line identification errors related to a window of 312 lines
0	0	0	0	0	0	0	0	0 : 312 theoretical highest sensitivity
0	0	0	0	0	0	0	1	1 : 312
0	0	0	1	1	0	0	1	25 : 312
1	1	1	1	1	1	1	1	255 : 312 theoretical lowest sensitivity

For programmed numbers from 0 to approximately 25 (dec) the colour signal is switched off. With the value 25 (dec) the colour signal will be enabled only when extremely good signal quality is present. If the colour signal quality is reduced, i.e. VCR signal source, bad S/N ratio, bad quantization, diminished colour carrier and insufficient IF adaption, the sensitivity should be set lower (higher programmed number up to 255 (dec) in order to prevent excessive switching and thus ensure constant colour.

Subaddress 15 (HEX)

Programmable adaptive filter PAF (P6–P0)

Application (IF stage) dependent

The programmable adaptive filter, together with the cloche and linear bandpass filter, forms a filter-curve that treats the chrominance frequency spectra with different gain but linear phase. The frequency characteristic is a system of sinusoidal waveforms which are described by:

- Reference "knots" of constant gain (0 dB)
- Frequency points ("tops") with maximum gain
- The amount of maximum gain
  (There is also a switchable pre-amplifier in another stage of the bandpass filter).

The components of the PAF can be programmed via the I²C-bus by using device address 8A (or 8E) and subaddress 15 thereby producing 57 different transfer functions. An example of some transfer functions is given in Figure 8 (a) to (d).

MSB	P6	P5	P4	P3	P2	P1	P0	function			
								maximum gain at tops			
–	X	X	X	X	1	1	1	19 dB			
–	X	X	X	X	1	1	0	14 dB			
–	X	X	X	X	1	0	1	9.5 dB			
–	X	X	X	X	1	0	0	6 dB			
–	X	X	X	X	0	1	1	3.5 dB			
–	X	X	X	X	0	1	0	2 dB			
–	X	X	X	X	0	0	1	1 dB			
–	X	X	X	X	0	0	0	0 dB			
								position of tops and knots (MHz)			
								top	knot	top	Figs 8a–d
–	X	1	1	1	X	X	X	3.375	4.5	5.625	+ A/dB (d)
–	X	1	1	0	X	X	X	4.5	5.625	6.75	–A/dB (d)
–	X	1	0	1	X	X	X	4.219	5.063	5.906	–A/dB (c)
–	X	1	0	0	X	X	X	3.375	4.219	5.063	+ A/dB (c)
–	X	0	1	1	X	X	X	4.05	5.4	6.75	–A/dB (b)
–	X	0	1	0	X	X	X	2.7	4.05	5.4	+ A/dB (b)
–	X	0	0	1	X	X	X	2.89	3.86	4.82	+ A/dB (a)
–	X	0	0	0	X	X	X	3.86	4.82	5.79	–A/dB (a)
								additional pre-amplification			
–	1	X	X	X	X	X	X	times two			
–	0	X	X	X	X	X	X	times one			
*	X	X	X	X	X	X	X	* MSB not used			

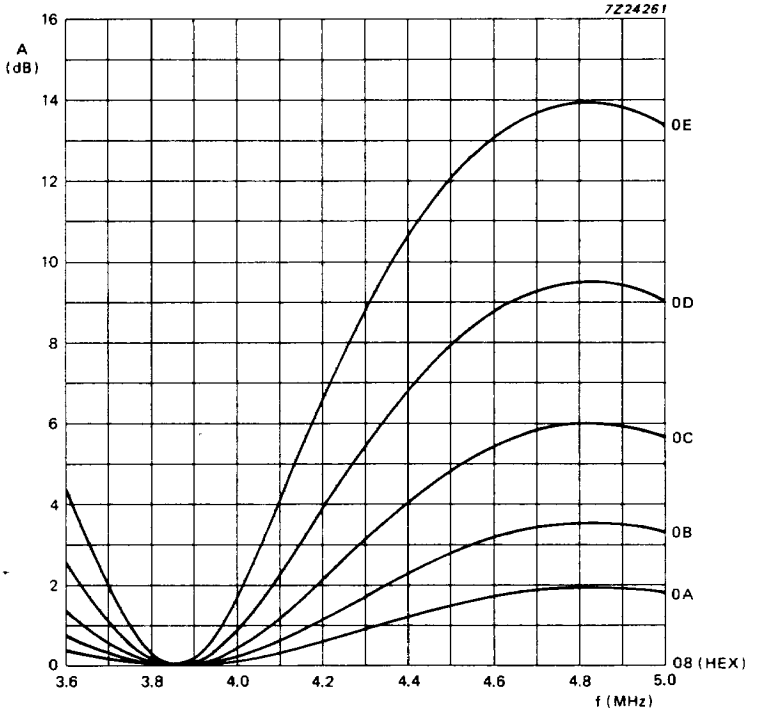


Fig. 8(a) Examples of frequency response for the programmable adaptive filter; from 08 to 0E (HEX).

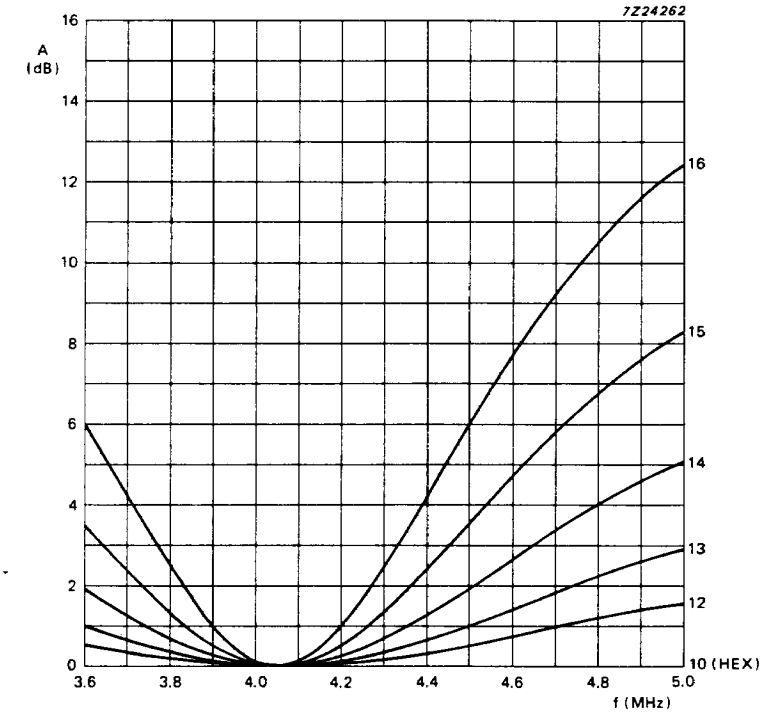


Fig. 8(b) Example of frequency response for the programmable adaptive filter; from 10 to 16 (HEX).

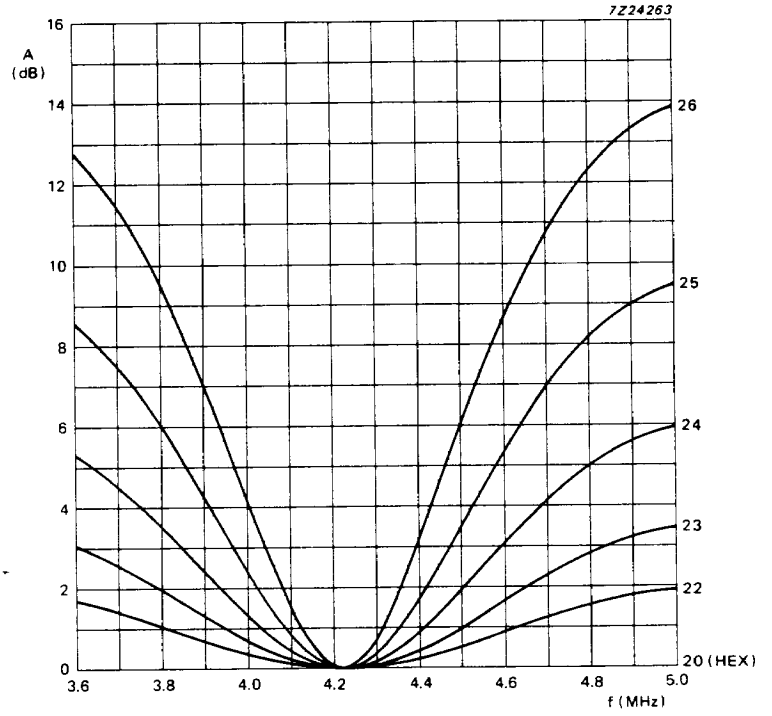


Fig. 8(c) Example of frequency response for the programmable adaptive filter; from 20 to 26 (HEX).

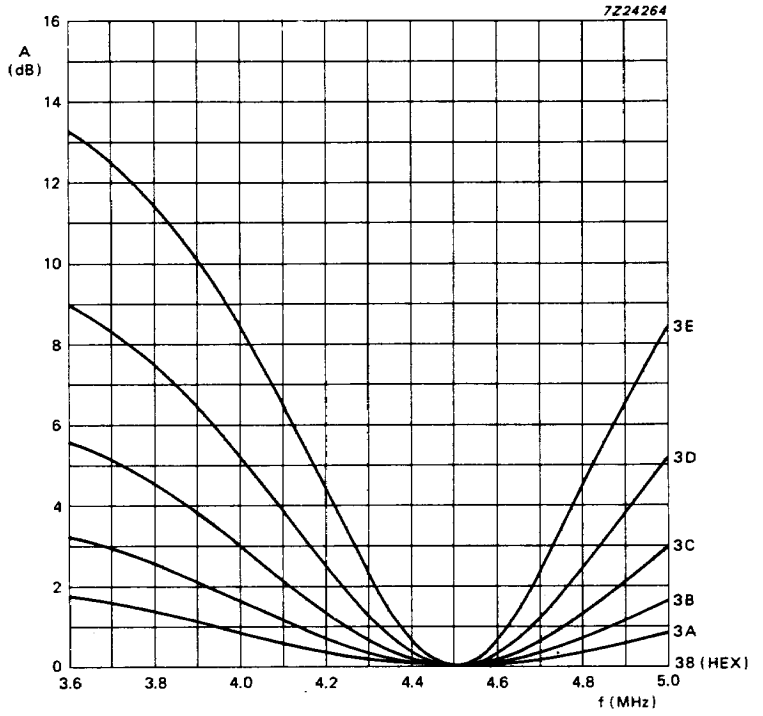


Fig. 8(d) Example of frequency response for the programmable adaptive filter; from 38 to 3E (HEX).

Subaddress 16 (HEX)

DSD control 3 register

C2	C1	C0	UV-output
X	0	1	active zero whole line
X	1	0	colour enable (if CS flag then colour on)
X	1	1	colour forced on (independent of CS flag)
0	X	X	positive UV
1	X	X	negative UV
0	0	0	3-state
1	0	0	UV2-output active during horizontal blanking period (CS-bit* transmission); high impedance in active line negative UV

After power-on reset the control register is set to logic 0.

* The position of the CS transmission is dependent on the start value of the main counter (Reg 10 and 11).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	I_{max} = 20 mA	V_{DD}	−0.5	7.0	V
Voltage input		V_I	−0.5	7.0	V
Voltage output		V_O	−0.5	7.0	V
Total power dissipation		P_{tot}	–	1.2	W
Operating ambient temperature range		T_{amb}	0	70	°C
Storage temperature range		T_{stg}	−65	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current (f_{nom}) Inputs LOW; outputs with maximum load	V_{DD} = 5.5 V	I_{DD}	–	–	180	mA
Inputs						
Input voltage LOW (clock data) pins 2, 16, 17 to 21; and 24 to 27		V_{IL}	0	–	0.8	V
Input voltage LOW (I^2C) pins 1 and 28		V_{IL}	0	–	1.5	V
Input voltage HIGH (data) pins 2, 17 to 21; and 24 to 27		V_{IH}	2	–	V_{DD}	V
Input voltage HIGH (LL3) pin 16		V_{IH}	2.4	–	V_{DD}	V
Input voltage HIGH (I^2C) pins 1 and 28		V_{IH}	3	–	V_{DD}	V
Input leakage current pins 1, 2, 12 to 21; and 24 to 27		I_{LI}	−10	–	+ 10	μA
Input current pins 8 and 11		I_I	−10	–	+ 60	μA
Input capacitance (data) pins 2, 18 to 21; and 24 to 27		C_I	2	–	7.5	pF
Input capacitance (clock) pin 16		C_I	5	–	10	pF
Input capacitance (reset) pin 17		C_I	2	–	10	pF
Outputs						
Output voltage LOW pins 3 to 5; 8 to 15	I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW SDA pin 1	I_{OL} = 5 mA	V_{OL}	0	–	0.45	V
Output voltage HIGH pins 3 to 5; 8 to 15	I_{OL} = −0.5 mA	V_{OH}	2.4	–	V_{DD}	V
Capacitive load of outputs in high impedance pins 12 to 15		C_Z	2	–	15	pF

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 0 to 70 °C; unless otherwise specified. All voltages are referenced to ground (pins 6 and 23) unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Clock timing (LL3)						
Cycle time	note 1	t_{C3}	69	–	80	ns
Duty factor		δ	43	–	57	%
Rise time	note 2	t_r	–	–	6	ns
Fall time	note 2	t_f	–	–	6	ns
Input timing						
Data set up time		t_{SU}	12	–	–	ns
Data hold time	note 3	t_{IH}	5	–	–	ns
Output timing						
Data load capacitance		C_L	7.5	–	50	pF
Data hold time	V_{IH}(CLK) = 3 V	t_{OH}	5	–	–	ns
Data delay time	C_L = 25 pF	t_{OD}	–	–	45	ns

Notes to the characteristics

1. Static deviation = ±2%; dynamic deviation = ±7% for signal path CVBS-DCVBS (this is required for the running-in of the DMSD sync processor).
2. The rising and falling edges of the clock signal are assumed to be smooth due to roll-off low-pass filtering.
3. Matches to SAA9058 for V_{IH}(LL3) ⩾ 3 V.

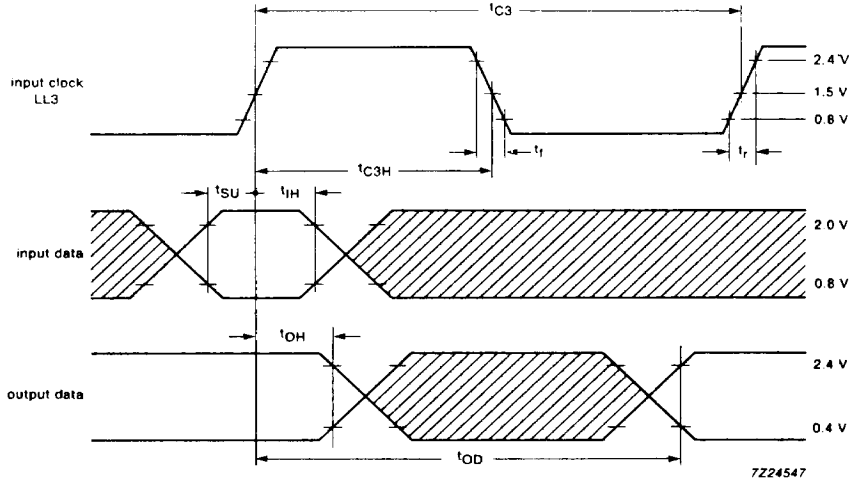


Fig. 9 Timing diagram.