SDA 2040
SDA 2060
SDA 2080

DIP 40

Features

- Upgraded 8-bit CPU as compared to SAB 8051
- +5V supply voltage
- On-chip 4K/6K/8Kbyte ROM
- 128 byte internal RAM
  64 Kbyte RAM can be connected externally
  (internal and external RAM can be used simultaneously)
- 1 µs internal cycle with 12 MHz clock frequency
- 34 bidirectional I/O ports:
  - two 8-bit ports
  - one 8-bit multifunction port
  - one 8-bit port with 15 mA current sink per output
    (suited for direct LED MUX control)
- One serial I^2C bus interface (2-bit port open drain) suited for multi-master operation
- Input for direct modulated digital infrared signal processing
  (optimum carrier frequency is approx. 30 kHz)
- Powerful interrupt structure with 5 sources and 2 hierarchy levels
- Instruction set downward-compatible with existing programs for SDA 2010/2030/2110
- Power-down mode with internal RAM data retention and reduced power consumption
- Two 16-bit timers/counters
- Instructions for direct multiplication or division, execution time only 4 µs
- Boolean processor implementable for pure controlling tasks

Circuit description

The three components SDA 2040/2060/2080 are identical with respect to pin configuration and functions, they differ, however, in the size of the program memory.

This enables an individual matching to system requirements.

Software development is supported in two ways:

1) Replacement of functions with SDA 2082 and external program memory.
   Note: Usability of ports P0 and P2 is limited.
2) Replacement of functions and emulation with bond out chip SDA 3080 and piggyback.

A Siemens microcomputer development system (e.g. SME 232) can be used for SDA 2040/60/80 program development and system testing. Powerful edit, assembler and debug programs are available.

The SDA 2040/60/80, a successor type to the SAB 8051, belongs to the family of single-chip microcomputers, for which the operational emphasis is no longer placed on pure numeric control functions.

The SDA 2040/60/80, specially developed for entertainment electronic applications, can be recommended especially for those applications, where lowest component costs and high quantities are an essential requirement.

Architecture and instruction set are based on the SAB 8051 microcomputer. In the same manner as the SAB 8051, the SDA 2040/60/80 possesses a number of features that facilitate programming:

- variable allocation of RAM
- unrestricted stack location in RAM
- 4 register banks
- special function register
- memory mapped I/O

Individually addressable bits and a Boolean processor enable the programmer to improve software performance. Numeric problems can be solved in binary or in BCD arithmetic. The large number of instructions for processing binary functions also plays a part in increasing the performance of the computer as a controller. All of these features, when used appropriately, lead to a reduction of peripheral hardware, to a simplification of the software, and thus, to a reduction of development and component cost.

The SDA 2040/60/80 contains a 4K/6K/8Kbyte program memory (ROM), an internal 128 byte RAM (an additional 64Kbyte can be added externally, ref. SDA 2082 application example), two 16-bit timers/counters, a nested interrupt structure with two priority levels, and an integrated oscillator. Additionally, the computer can address 64Kbyte of external data memory. The 34 digital I/O ports comprise four 8-bit ports and a serial interface with data and clock lines. The serial I/O interface fully complies with the I²C multimaster protocol. The IR input P3.0 can process modulated signals with a carrier frequency of approx. 30kHz. It contains a digital demodulator for deriving the envelope curve of modulated and inverted digital signals. As the digital demodulator is software enabled and disabled, it is also possible to use the IR port as a normal digital, quasi-bidirectional I/O port. The multifunction port P3 comprises two interrupt inputs and two counter inputs.

The instruction set, consisting of 49 one-byte, 46 two-byte, and 16 three-byte instructions, ensures efficient utilization of program memory. If a 12 MHz crystal is used, the execution time for the instructions is either 1 µs or 2 µs. The execution time for the very complex instructions for "multiply" and "divide" is only 4 µs. Information about the number of bytes and the execution time can be found in the instruction set summary for the SDA 2040/60/80.

Maximum ratings

Voltage between any pin and ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	2	W
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_{CC}	5 ± 10%	V
Ambient temperature	T_A	0 to 70	°C

DC characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ±10%; $V_{SS} = 0$ V

		Test conditions	min	max	
L input voltage (all inputs except XTAL 2, P 4)	V_{iL}		−0.5	0.8	V
L input voltage (XTAL 2)	V_{iL1}		−0.5	0.6	V
L input voltage (P 4)	V_{iL2}		−0.5	1.5	V
H input voltage (except XTAL 2, RST/V_{PD}, P 4)	V_{iH}		2.0	$V_{CC}+0.5$	V
H input voltage (XTAL 2)	V_{iH1}		2.5	$V_{CC}+0.5$	V
H input voltage (RST)	V_{iH2}		2.5	$V_{CC}+0.5$	V
H input voltage (V_{PD})	V_{iH3}	$V_{CC} = 0$	4.5	5.5	V
H input voltage (P 4)	V_{iH4}		3.0	$V_{CC}+0.5$	V
L output voltage (port 0)	V_{qL}	$I_{qL} = 3.2$ A		0.45	V
L output voltage (port 0)	V_{qL1}	$I_{qL1} = 15$ mA		1.0	V
L output voltage (ports 1, 2 and 3)	V_{qL2}	$I_{qL2} = 1.6$ mA		0.45	V
L output voltage (ALE)	V_{qL2}	$I_{qL2} = 3.2$ mA		0.45	V
L output voltage (port1)	V_{qL3}	$I_{qL3} = 7.5$ mA		1.0	V
L output voltage (port 4)	V_{qL4}	$I_{qL4} = 3.0$ mA		0.4	V
H output voltage (ports 1, 2 and 3)	V_{qH}	$I_{qH} = -80$ µA	2.4		V
H output voltage (port 0 and ALE)	V_{qH1}	$I_{qH1} = -400$ µA	2.4		V
Current of internal pull-up resistance (P 1, P 2, P 3)	I_{LQ}	0.45 V = V_{IN} = V_{CC}	−800		µA
Leakage current of outputs	I_{LQ1}	0.45 V = V_{IN} = V_{CC}		± 10	µA
Current consumption (all outputs disconnected)	I_{CC}			150	mA
Current consumption (power-down mode)	I_{PD}	$V_{CC} = 0$ V		20	mA
Capacitance of inputs/outputs	C_{IO}	$f_C = 1$ MHz		10	pF

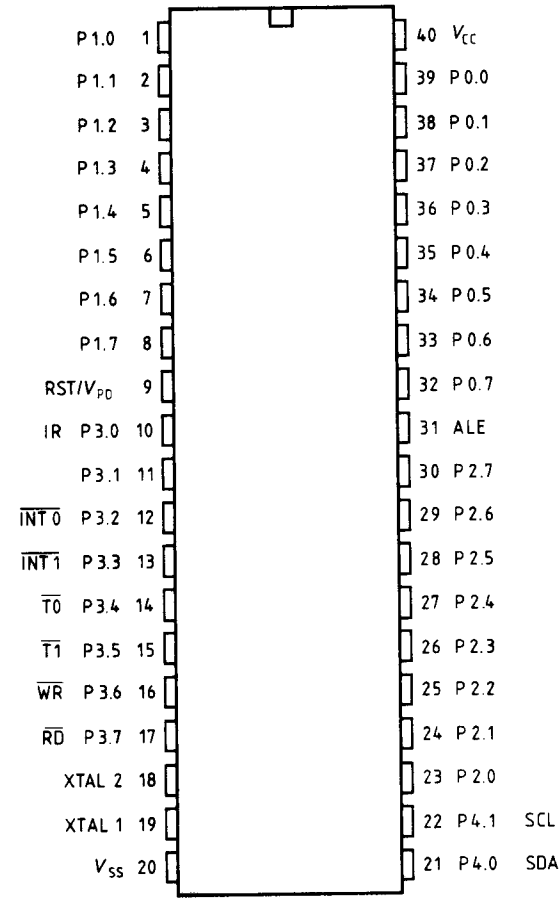
AC characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ± 10%; $V_{SS} = 0$ V

$C_L = 100$ pF (for port 0, and ALE output)
$C_L = 80$ pF (for all other outputs)

		Maximum ratings				
		Variable clock $1/t_{CL\,CL} = 1.2$–12 MHz		12 MHz clock		
		min	max	min	max	
Cycle time of oscillator	$t_{CL\,CL}$	83	833.3	83		ns
Min. cycle period	t_{CY}	12 $t_{CL\,CL}$	12 $t_{CL\,CL}$	1000		ns
ALE pulse width	$t_{LH\,LL}$	2 $t_{CL\,CL}$-40		127		ns
RD pulse width	$t_{RL\,RH}$	6 $t_{CL\,CL}$-100		400		ns
WR pulse width	$t_{WL\,WH}$	6 $t_{CL\,CL}$-100		400		ns

Pin configuration



Pin description

Symbol	Function
V_{SS}	GND 0 V
V_{CC}	+5 V
Port 0	Bidirectional 8-bit port with 3.2 mA current sink at 0.45 V and 15 mA current sink at 1.0 V for direct LED control (static or MUX operation).
Port 1	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V and 7.5 mA current sink at 1.0 V for direct LED display.
Port 2	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V.
Port 3	Bidirectional 8-bit port with 1.6 mA current sink at 0.45 V. Also includes the inputs of the interrupt and timer controls. For a program-controlled enabling of the function, the corresponding latch must be active high. The allocation of the special function registers is as follows: - $\overline{IR}$ (P 3.0) Input of the digital demodulator to generate an envelope curve of a standard modulated IR signal (inverted) - $\overline{INT\,0}$ (P 3.2) Input for interrupt 0 or for enabling/disabling the counter input T 0 - $\overline{INT\,1}$ (P 3.3) Input for interrupt 1 or for enabling/disabling the counter input T 1 - $\overline{T0}$ (P 3.4) Counter input T 0 - $\overline{T1}$ (P 3.5) Counter input T 1 - $\overline{WR}$ (P 3.6) Write strobe for external data memory (RAM) - $\overline{RD}$ (P 3.7) Read strobe for external data memory
Port 4	Bidirectional 2-bit port with open drain outputs, with 3 mA current sink at 0.4 V. Port 2 contains a bidirectional serial interface with DATA (SDA, pin 21) and CLOCK line (SCL, pin 22). The serial interface fully meets the requirements of the I^2C bus protocol.
RST/V_{PD}	At a connected supply voltage V_{CC} = 5 V, an edge transition from low to high (at approximately 3 V) resets the SDA 2040/60/80, i.e. the user program starts with address 0. When V_{PD} = high (approx. +5 V), a drop in V_{CC} triggers the processor's transition into the power-down mode. In this case, a current supply of max. 20 mA is provided to the RAM via pin RST/V_{PD}. In the case V_{PD} = 0 V and V_{CC} = 5 V, the RAM is supplied via V_{CC}.
ALE	Address Latch Enable output for controlling external memory access during normal operation.
XTAL1	Oscillator input for crystal operation. For external clock source connect to V_{SS}.
XTAL2	Oscillator output; required when crystal is used. Input during external clock supply.

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Arithmetic operations

Mnemonic	Description	Bytes	Cycles
ADD A, Rn	Add register to Accumulator	1	1
ADD A, direct	Add direct byte to Accumulator	2	1
ADD A, @ Ri	Add indirect RAM to Accumulator	1	1
ADD A, # data	Add immediate data to Accumulator	2	1
ADDC A, Rn	Add register to Accumulator with Carry flag	1	1
ADDC A, direct	Add direct byte to A with Carry flag	2	1
ADDC A, @ Ri	Add indirect RAM to A with Carry flag	1	1
ADDC C, # data	Add immediate data to A with Carry flag	2	1
SUBB A, rn	Subtract register from A with Borrow	1	1
SUBB A, direct	Subtract direct byte from A with Borrow	2	1
SUBB A, @ Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB A, # data	Subtract immediate data from A with Borrow	2	1
INC A	Increment Accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement Accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @ Ri	Decrement indirect RAM	1	1
INC DPTR	Increment Data Pointer	1	2
MUL AB	Multiply A&B	1	4
DIV AB	Divide A&B	1	4
DA A	Decimal Adjust Accumulator	1	1

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Logical operations

Mnemonic	Description	Bytes	Cycles
ANL A, Rn	AND register to Accumulator	1	1
ANL A, direct	AND direct byte to Accumulator	2	1
ANL A, @ Ri	AND indirect RAM to Accumulator	1	1
ANL A, # data	AND immediate data to Accumulator	2	1
ANL direct, A	AND Accumulator to direct byte	2	1
ANL direct, # data	AND immediate data to direct byte	3	2
ORL A, Rn	OR register to Accumulator	1	1
ORL A, direct	OR direct byte to Accumulator	2	1
ORL A, @ Ri	OR indirect RAM to Accumulator	1	1
ORL A, # data	OR immediate data to Accumulator	2	1
ORL direct, A	OR Accumulator to direct byte	2	1
ORL direct, # data	OR immediate data to direct byte	3	2
XRL A, Rn	Exclusive-OR register to Accumulator	1	1
XRL A, direct	Exclusive-OR direct byte to Accumulator	2	1
XRL A, @ Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL A, # data	Exclusive-OR immediate data to Accumulator	2	1
XRL direct, A	Exclusive-OR Accumulatur to direct byte	2	1
XRL direct, # data	Exclusive-OR immediate data to direct byte	3	2
CRL A	Clear Accumulator	1	1
CPL A	Complement Accumulator	1	1
RL A	Rotate Accumulator left	1	1
RLC A	Rotate A left thorugh the Carry flag	1	1
RR A	Rotate Accumulator right	1	1
RRC A	Rotate A right through the Carry flag	1	1
SWAP A	Swap nibbles within the Accumulator	1	1

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Data transfer operations

Mnemonic	Description	Bytes	Cycles
MOV A, Rn	Move register to Accumulator	1	1
MOV A, direct	Move direct byte to Accumulator	2	1
MOV A, @ Ri	Move indirect RAM to Accumulator	1	1
MOV A, # data	Move immediate data to Accumulator	2	1
MOV Rn, A	Move Accumulator to register	1	1
MOV Rn, direct	Move direct byte to register	2	2
MOV Rn, # data	Move immediate data to register	2	1
MOV direct, A	Move Accumulator to direct byte	2	1
MOV direct, Rn	Move register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	2
MOV direct, @ Ri	Move indirect RAM to direct byte	2	2
MOV direct, # data	Move immediate data to direct byte	3	2
MOV @ Ri, A	Move Accumulator to indirect RAM	1	1
MOV @ Ri, direct	Move direct byte to indirect RAM	2	2
MOV @ Ri, # data	Move immediate data to indirect RAM	2	1
MOV DPTR, # data 16	Load Data Pointer with a 16-bit constant	3	2
MOVC A@A + DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC A@A + PC	Move Code byte relative to PC to Accumulator	1	2
MOVX A, @ Ri	Move External RAM (8-bit addr) to Accumulator	1	2
MOVX A, @ DPTR	Move External RAM (16-bit addr) to Accumulator	1	2
MOVX @ Ri, A	Move A to External RAM (8-bit addr)	1	2
MOVX @ DPTR, A	Move A to External RAM (16-bit addr)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with Accumulator	1	1
XCH A, direct	Exchange direct byte with Accumulator	2	1
XCH A, @ Ri	Exchange indirect RAM with Accumulator	1	1
XCHD A, @ Ri	Exchange low-order digital indirect RAM with A	1	1

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Boolean variable manipulation

Mnemonic	Description	Bytes	Cycles
CLR C	Clear Carry flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry flag	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement Carry flag	1	1
CPL bit	Complement direct bit	2	1
ANL C, bit	AND direct bit to Carry flag	2	2
ANL C,/bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to Carry flag	2	2
ORL C,/bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry flag	2	1
MOV bit, C	Move Carry flag to direct bit	2	2

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Program control operations

Mnemonic	Description	Bytes	Cycles
ACALL addr 11	Absolute subroutine call	2	2
LCALL addr 16	Long subroutine call	3	2
RET	Return from subroutine	1	2
RETI	Return from interrupt	1	2
AJMP addr 11	Absolute jump	2	2
LJMP addr 16	Long jump	3	2
SJMP rel	Short jump (relative addr)	2	2
JMP @ A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is zero	2	2
JNZ rel	Jump if Accumulator is not zero	2	2
JC rel	Jump if Carry flag is set	2	2
JNC rel	Jump if Carry flag is not set	2	2
JB bit, rel	Jump if direct bit set	3	2
JNB bit, rel	Jump if direct bit not set	3	2
JBC bit, rel	Jump if direct bit is set and clear bit	3	2
CJNE A, direct, rel	Compare direct to A and jump if not equal	3	2
CJNE A, # data, rel	Compare immediate to A and jump if not equal	3	2
CJNE Rn, # data, rel	Compare immediate to register and jump if not equal	3	2
CJNE @ Ri, # data, rel	Compare immediate to indirect and jump if not equal	3	2
DJNZ Rn, rel	Decrement direct and jump if not zero	2	2
DJNZ direct, rel	Decrement direct and jump if not zero	3	2
NOP	No operation	1	1

Symbols and abbreviations

A	Accumulator	Rr	Register label (r=0-7)
adr	11-bit program memory address	Sn	S interface label (n = 0; 1)
CNT	Event counter	T	Timer
DA	D/A converter indication	T0, T1	Test 0, test 1
data	8-bit binary number	#	Refers to immediate data
P	Mnemonic for "in page" operation	@	Refers to indirect addressing
Pp	Port label (p = 0-3)		