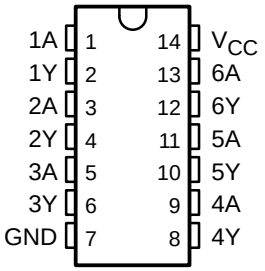
- **Convert TTL Voltage Levels to MOS Levels**
- **High Sink-Current Capability**
- **Input Clamping Diodes Simplify System Design**
- **Open-Collector Driver for Indicator Lamps and Relays**
- **Inputs Fully Compatible With Most TTL Circuits**

SN5407, SN5417 . . . J OR W PACKAGE
SN7407, SN7417 . . . D, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

These TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS) or for driving high-current loads (such as lamps or relays), and also are characterized for use as buffers for driving TTL inputs. The SN5407 and SN7407 have minimum breakdown voltages of 30 V, and the SN5417 and SN7417 have minimum breakdown voltages of 15 V. The maximum sink current is 30 mA for the SN5407 and SN5417 and 40 mA for the SN7407 and SN7417.

These devices perform the Boolean function Y = A in positive logic.

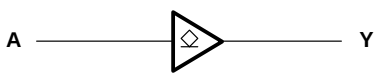
These circuits are completely compatible with most TTL families. Inputs are diode clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 145 mW, and average propagation delay time is 14 ns.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube	SN7407D	7407
		Tape and reel	SN7407DR	
		Tube	SN7417D	7417
		Tape and reel	SN7417DR	
	PDIP – N	Tube	SN7407N	SN7407N
			SN7417N	SN7417N
	SOP – NS	Tape and reel	SN7407NSR	SN7407
			SN7417NSR	SN7417
–55°C to 125°C	CDIP – J	Tube	SNJ5407J	SNJ5407J
			SNJ5417J	SNJ5417J
	CFP – W	Tube	SNJ5407W	SNJ5407W
			SNJ5417W	SNJ5417W

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram, each buffer/driver (positive logic)



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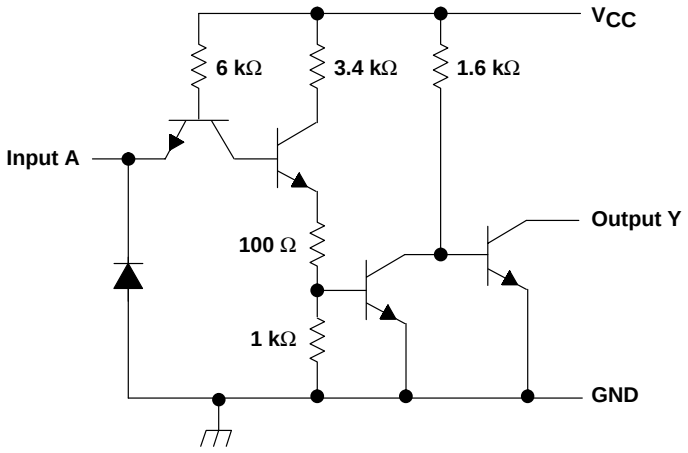
schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . 0.5 V to 5.5 V
Output voltage, V_O (see Notes 1 and 2): SN5407, SN7407 . . . . . 30 V
SN5417, SN7417 . . . . . 15 V
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. This is the maximum voltage that should be applied to any output when it is in the off state.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN5407, SN5417	4.5	5	5.5	V
		SN7407, SN7417	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	SN5407, SN7407			30	V
		SN5417, SN7417			15	
I_{OL}	Low-level output current	SN5407, SN5417			30	mA
		SN7407, SN7417			40	
T_A	Operating free-air temperature	SN5407, SN5417	–55		125	°C
		SN7407, SN7417	0		70	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

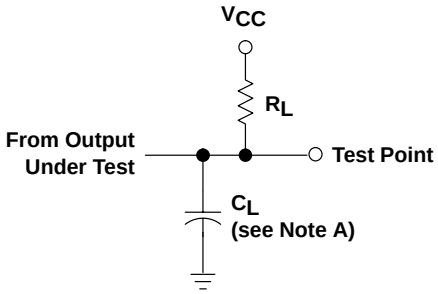
PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = –12 mA				–1.5	V
I_{OH}	V_{CC} = MIN, V_{IH} = 2 V	V_{OH} = 30 V (SN5407, SN7407)			0.25	mA
		V_{OH} = 15 V (SN5417, SN7417)			0.25	
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V	I_{OL} = 16 mA			0.4	V
		I_{OL} = 30 mA (SN5407, SN5417)			0.7	
		I_{OL} = 40 mA (SN7407, SN7417)			0.7	
I_I	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = MAX, V_{IH} = 2.4 V				40	µA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V				–1.6	mA
I_{CCH}	V_{CC} = MAX			29	41	mA
I_{CCL}	V_{CC} = MAX			21	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

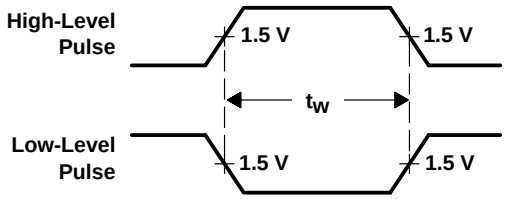
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 110 Ω, C_L = 15 pF		6	10	ns
t_{PHL}					20	30	
t_{PLH}	A	Y	R_L = 150 Ω, C_L = 50 pF			15	ns
t_{PHL}						26	

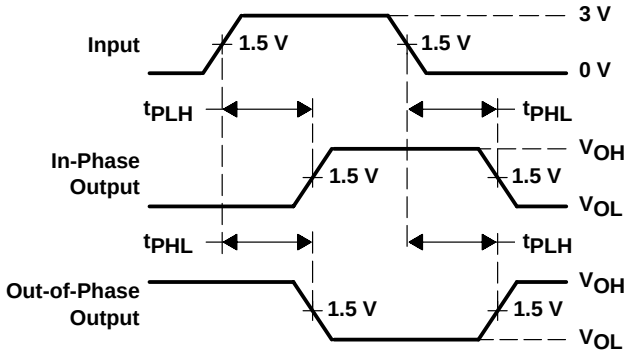
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE WIDTHS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

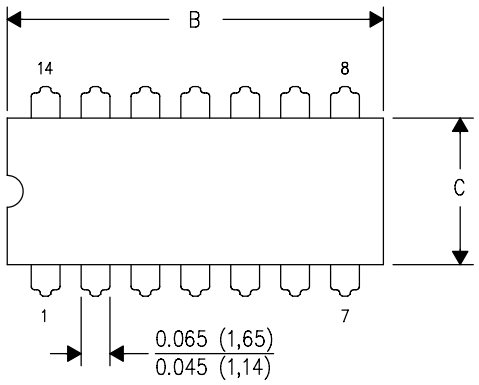
NOTES: A. C_L includes probe and jig capacitance.
B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 7 ns, t_f ≤ 7 ns.
D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

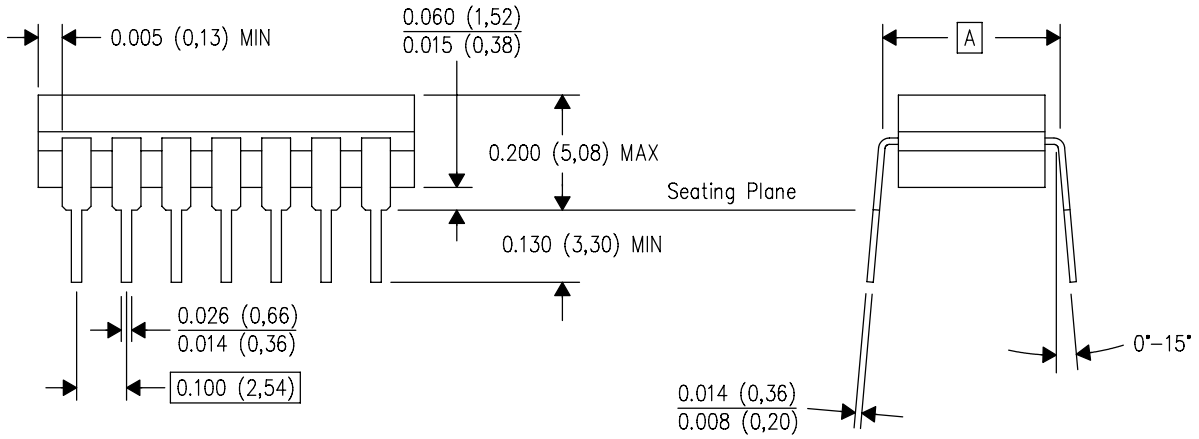
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

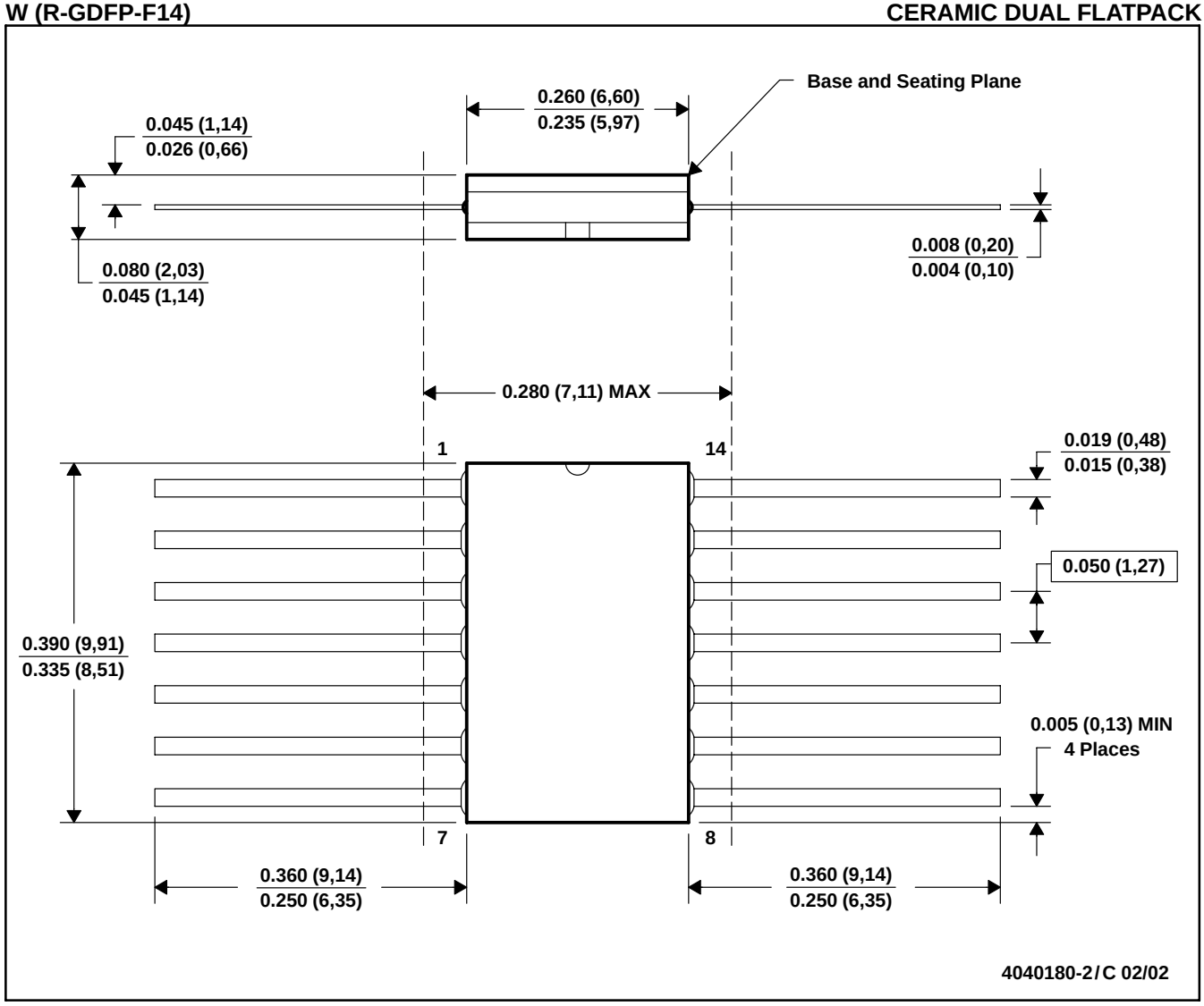


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MCFP002A – JANUARY 1995 – REVISED FEBRUARY 2002

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**

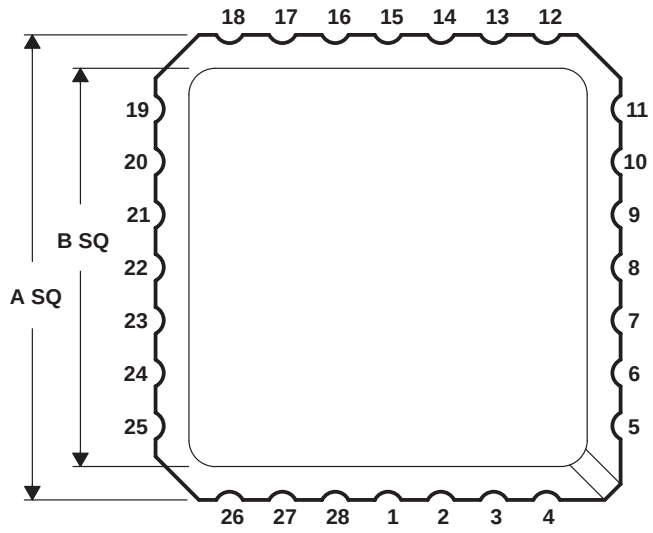


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

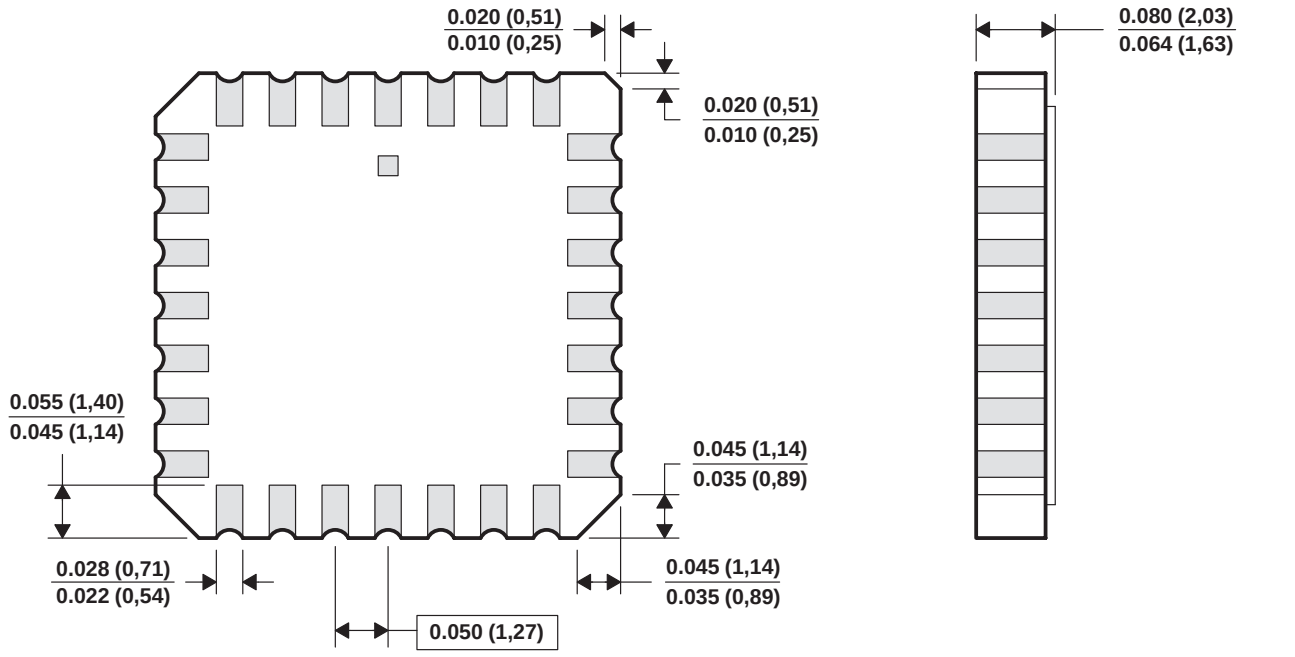
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



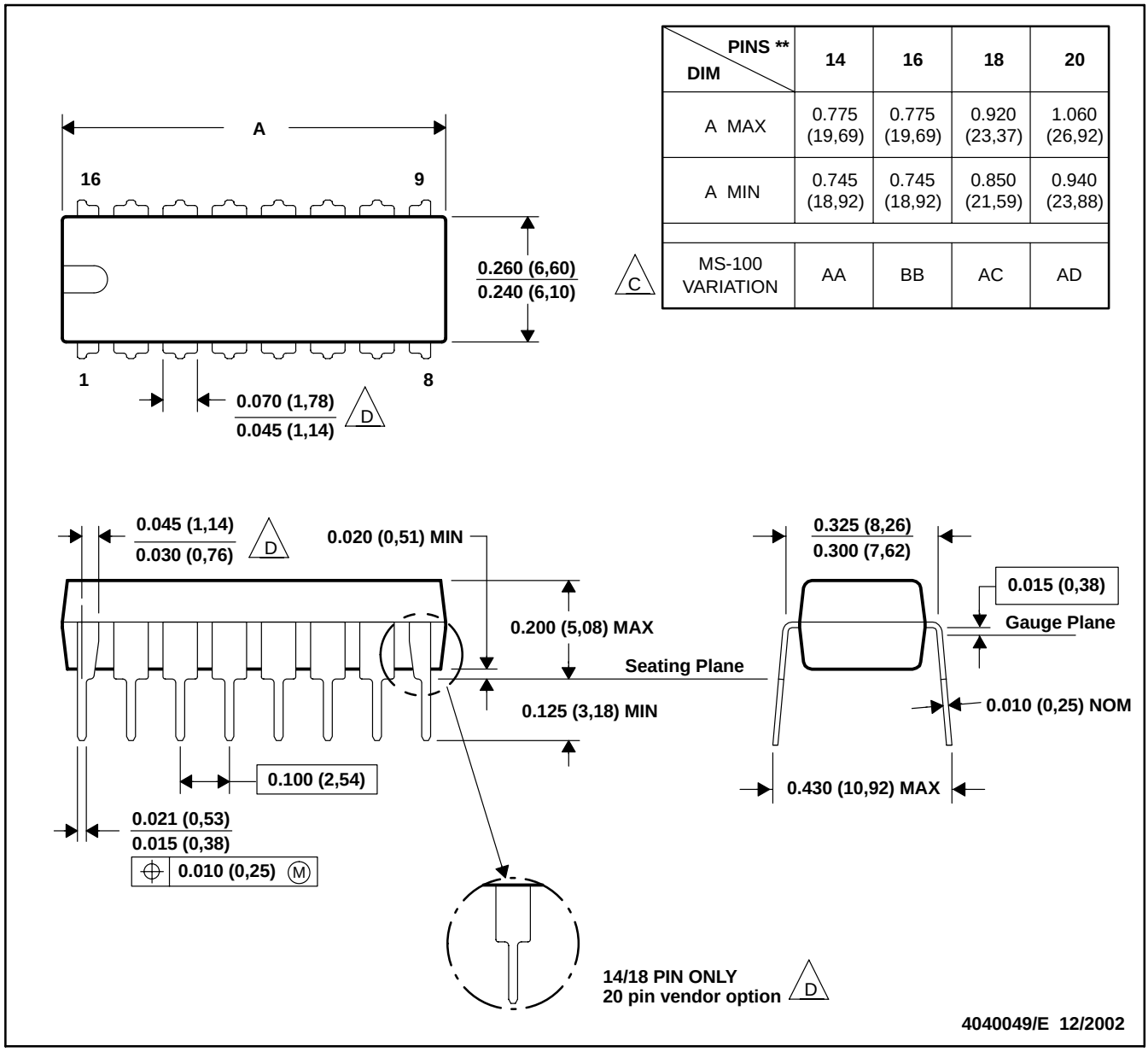
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

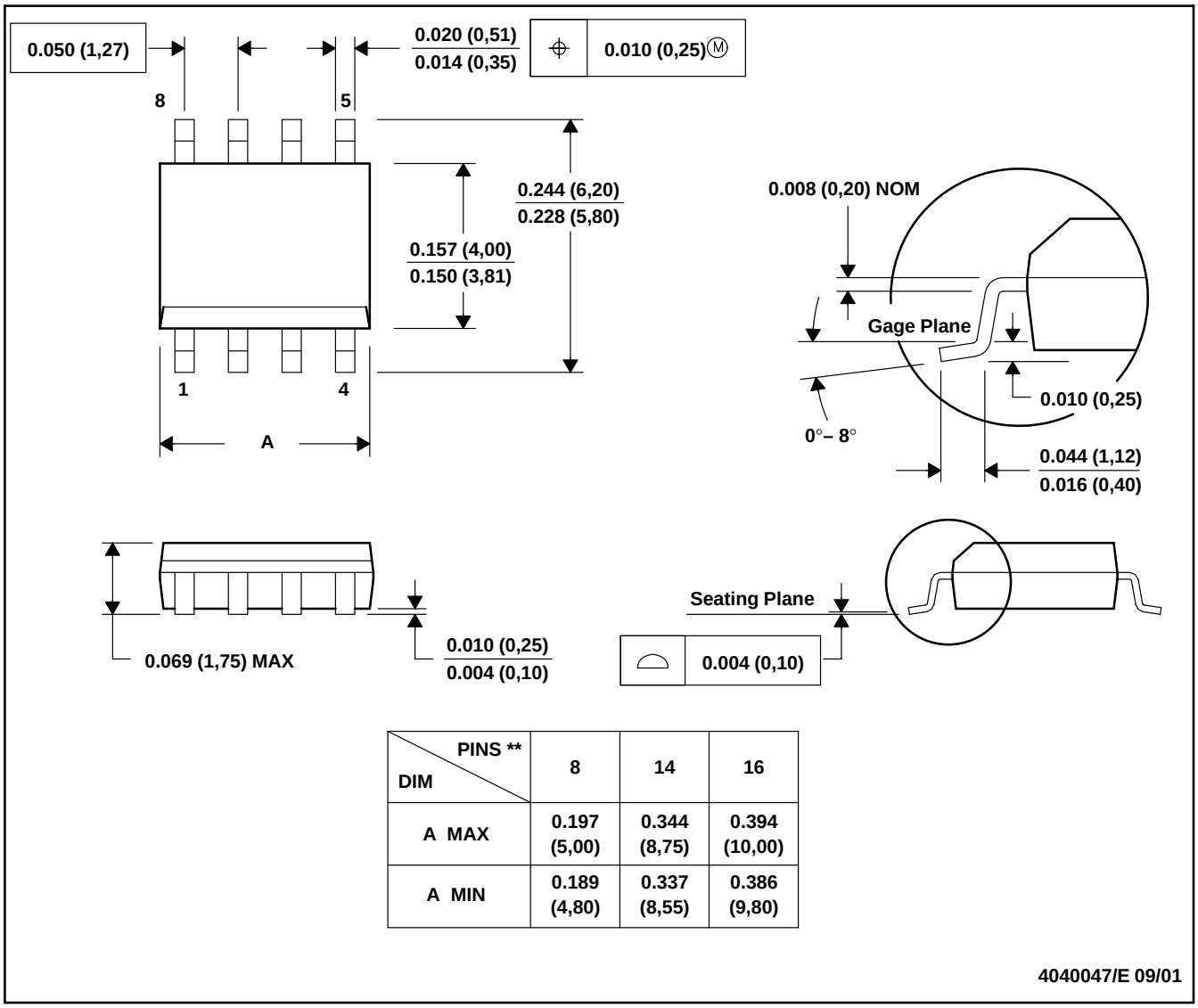
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

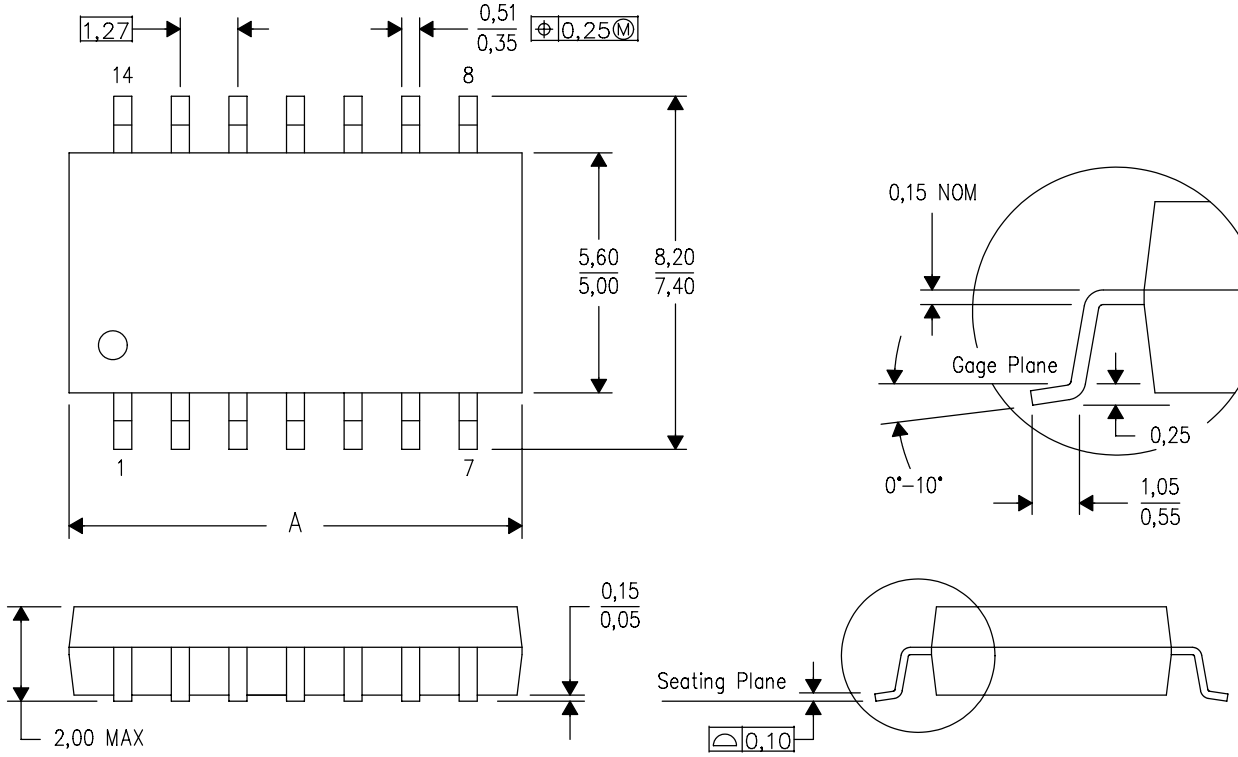
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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