- **Operating Range 2-V to 5.5-V V_{CC}**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

SN54AHC125 . . . J OR W PACKAGE
SN74AHC125 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)

```
          _____
1OE  []  1      14  [] V_CC
1A   []  2      13  [] 4OE
1Y   []  3      12  [] 4A
2OE  []  4      11  [] 4Y
2A   []  5      10  [] 3OE
2Y   []  6       9  [] 3A
GND  []  7       8  [] 3Y
```
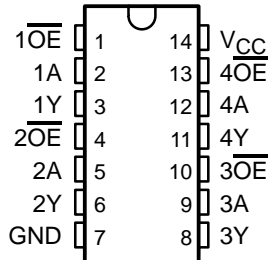
SN74AHC125 . . . RGY PACKAGE
(TOP VIEW)

```
        1OE   V_CC
         |     |
        1    14
1A   2          13  4OE
1Y   3          12  4A
2OE  4          11  4Y
2A   5          10  3OE
2Y   6           9  3A
        7     8
         |     |
        GND   3Y
```
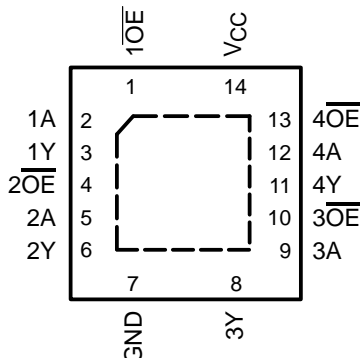
SN54AHC125 . . . FK PACKAGE
(TOP VIEW)

```
         1A  1OE  NC  V_CC  4OE
          3   2   1   20   19
1Y   []  4              18  [] 4A
NC   []  5              17  [] NC
2OE  []  6              16  [] 4Y
NC   []  7              15  [] NC
2A   []  8              14  [] 3OE
          9  10  11  12  13
         2Y  GND  NC  3Y  3A
```
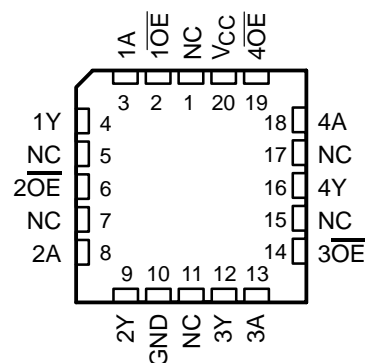
NC – No internal connection

description/ordering information

The 'AHC125 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high. When $\overline{OE}$ is low, the respective gate passes the data from the A input to its Y output.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Tape and reel	SN74AHC125RGYR	HA125
	PDIP – N	Tube	SN74AHC125N	SN74AHC125N
	SOIC – D	Tube	SN74AHC125D	AHC125
		Tape and reel	SN74AHC125DR	
	SOP – NS	Tape and reel	SN74AHC125NSR	AHC125
	SSOP – DB	Tape and reel	SN74AHC125DBR	HA125
	TSSOP – PW	Tape and reel	SN74AHC125PWR	HA125
	TVSOP – DGV	Tape and reel	SN74AHC125DGVR	HA125
−55°C to 125°C	CDIP – J	Tube	SNJ54AHC125J	SNJ54AHC125J
	CFP – W	Tube	SNJ54AHC125W	SNJ54AHC125W
	LCCC – FK	Tube	SNJ54AHC125FK	SNJ54AHC125FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)
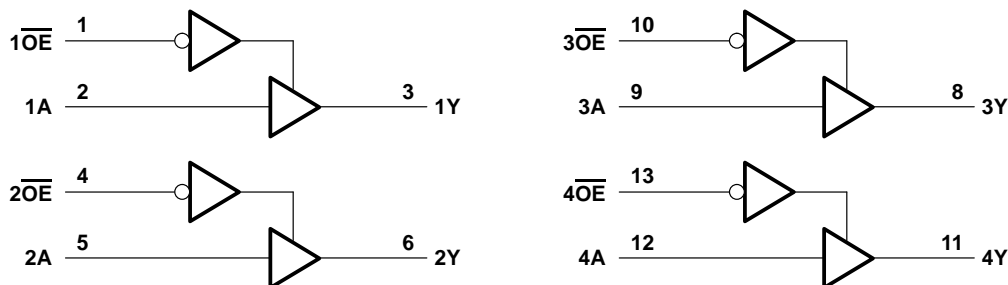
Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... −20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Continuous current through V_{CC} or GND .... ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
(see Note 2): DB package .... 96°C/W
(see Note 2): DGV package .... 127°C/W
(see Note 2): N package .... 80°C/W
(see Note 2): NS package .... 76°C/W
(see Note 2): PW package .... 113°C/W
(see Note 3): RGY package .... 47°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			SN54AHC125 MIN	SN54AHC125 MAX	SN74AHC125 MIN	SN74AHC125 MAX	UNIT
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 3$ V	2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 3$ V		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50		−50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		−4		−4	mA
		$V_{CC} = 5$ V ± 0.5 V		−8		−8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		4		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$ MIN	$T_A = 25°C$ TYP	$T_A = 25°C$ MAX	SN54AHC125 MIN	SN54AHC125 MAX	SN74AHC125 MIN	SN74AHC125 MAX	UNIT
V_{OH}	$I_{OH} = -50$ µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	$I_{OH} = -4$ mA	3 V	2.58			2.48		2.48		
	$I_{OH} = -8$ mA	4.5 V	3.94			3.8		3.8		
V_{OL}	$I_{OL} = 50$ µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	$I_{OL} = 4$ mA	3 V			0.36		0.5		0.44	
	$I_{OL} = 8$ mA	4.5 V			0.36		0.5		0.44	
I_I	$V_I = 5.5$ V or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5		±2.5	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	µA
C_i	$V_I = V_{CC}$ or GND	5 V		4	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0$ V.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54AHC125 MIN	SN54AHC125 MAX	SN74AHC125 MIN	SN74AHC125 MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF		5.6*	8*	1*	9.5*	1	9.5	ns
t_{PHL}	A	Y	C_L = 15 pF		5.6*	8*	1*	9.5*	1	9.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		5.4*	8*	1*	9.5*	1	9.5	ns
t_{PZL}	$\overline{OE}$	Y	C_L = 15 pF		5.4*	8*	1*	9.5*	1	9.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		7*	9.7*	1*	11.5*	1	11.5	ns
t_{PLZ}	$\overline{OE}$	Y	C_L = 15 pF		7*	9.7*	1*	11.5*	1	11.5	ns
t_{PLH}	A	Y	C_L = 50 pF		8.1	11.5	1	13	1	13	ns
t_{PHL}	A	Y	C_L = 50 pF		8.1	11.5	1	13	1	13	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		7.9	11.5	1	13	1	13	ns
t_{PZL}	$\overline{OE}$	Y	C_L = 50 pF		7.9	11.5	1	13	1	13	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		9.5	13.2	1	15	1	15	ns
t_{PLZ}	$\overline{OE}$	Y	C_L = 50 pF		9.5	13.2	1	15	1	15	ns
$t_{sk(o)}$	$\overline{OE}$	Y	C_L = 50 pF			1.5**				1.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
** On products compliant to MIL-PRF-38535, this parameter does not apply.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	SN54AHC125 MIN	SN54AHC125 MAX	SN74AHC125 MIN	SN74AHC125 MAX	UNIT
t_{PLH}	A	Y	C_L = 15 pF		3.8*	5.5*	1*	6.5*	1	6.5	ns
t_{PHL}	A	Y	C_L = 15 pF		3.8*	5.5*	1*	6.5*	1	6.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15 pF		3.6*	5.1*	1*	6*	1	6	ns
t_{PZL}	$\overline{OE}$	Y	C_L = 15 pF		3.6*	5.1*	1*	6*	1	6	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15 pF		4.6*	6.8*	1*	8*	1	8	ns
t_{PLZ}	$\overline{OE}$	Y	C_L = 15 pF		4.6*	6.8*	1*	8*	1	8	ns
t_{PLH}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	1	8.5	ns
t_{PHL}	A	Y	C_L = 50 pF		5.3	7.5	1	8.5	1	8.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	1	8	ns
t_{PZL}	$\overline{OE}$	Y	C_L = 50 pF		5.1	7.1	1	8	1	8	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	1	10	ns
t_{PLZ}	$\overline{OE}$	Y	C_L = 50 pF		6.1	8.8	1	10	1	10	ns
$t_{sk(o)}$			C_L = 50 pF			1**				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74AHC125		UNIT
		MIN	**MAX**	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 5: Characteristics are for surface-mount packages only.
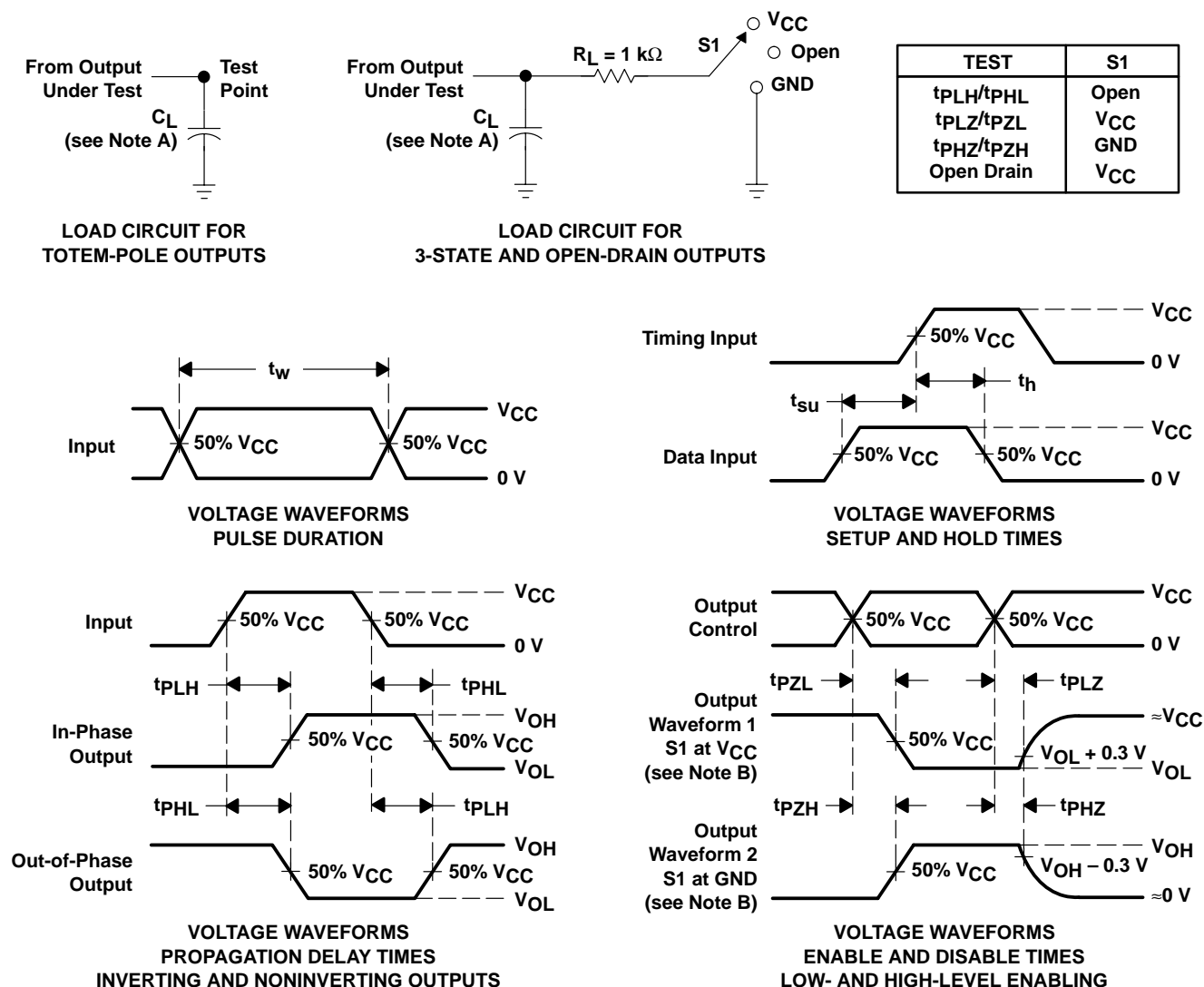
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265