

SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

- D-Type Flip-Flops in a Single Package With 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

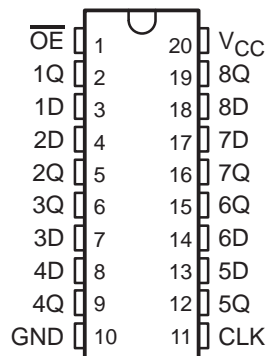
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

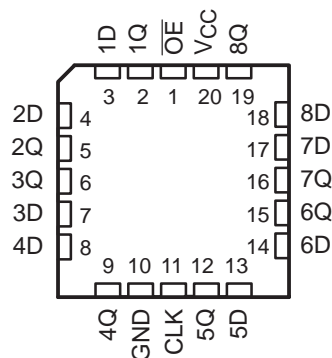
\overline{OE} does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374A and SN54AS374 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS374A and SN74AS374 are characterized for operation from 0°C to 70°C .

SN54ALS374A, SN54AS374 . . . J PACKAGE
SN74ALS374A, SN74AS374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS374A, SN54AS374 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z



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 **TEXAS
INSTRUMENTS**

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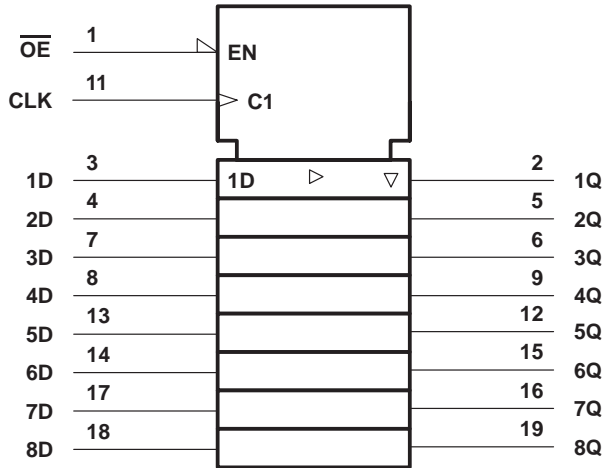
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SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374

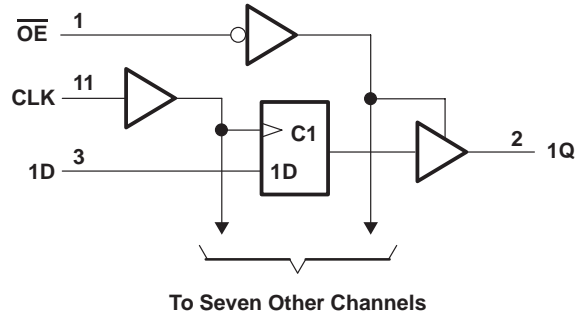
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I	-0.5 V to 7 V
Voltage applied to a disabled 3-state output	-0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	SN54ALS374A			SN74ALS374A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			-1			-2.6	mA
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	-55	125		0	70		°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS374A			SN74ALS374A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$		-1.5			-1.5			V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -1\text{ mA}$	2.4	3.3					
		$I_{OH} = -2.6\text{ mA}$				2.4	3.2		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25 0.4		0.25 0.4				V
		$I_{OL} = 24\text{ mA}$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.7\text{ V}$	20			20			μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$,	$V_O = 0.4\text{ V}$	-20			-20			μA
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$	0.1			0.1			mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$	20			20			μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$	-0.2			-0.2			mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-20	-112		-30	-112		mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	11	20	11 19				mA
		Outputs low	19	28	19 28				
		Outputs disabled	20	31	20 31				

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		SN54ALS374A		SN74ALS374A		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	30		35		MHz
t_w	Pulse duration	16.5		14		ns
t_{su}	Setup time	10		10		ns
t_h	Hold time	4		0		ns

switching characteristics over recommended operating conditions (unless otherwise noted (see Figure 3))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS374A		SN74ALS374A		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			30		35		MHz
t_{PLH}	CLK	Q	3	14	3	12	ns
t_{PHL}			5	17	5	16	
t_{PZH}	\overline{OE}	Q	3	18	3	17	ns
t_{PZL}			5	21	5	18	
t_{PHZ}	\overline{OE}	Q	1	11	1	10	ns
t_{PLZ}			2	19	2	18	



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recommended operating conditions

		SN54AS374			SN74AS374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.7			0.8			V
I_{OH}	High-level output current	-12			-15			mA
I_{OL}	Low-level output current	32			48			mA
T_A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS374			SN74AS374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$	-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$	2.4	3.2					
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$				2.4	3.3		
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 32\text{ mA}$	0.29			0.5			V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$				0.34	0.5		
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$	50			50			μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$	-50			-50			μA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$	0.1			0.1			mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$	20			20			μA
I_{IL}	$\overline{\text{OE}}$, CLK	-0.5			-0.5			mA
	Data	-3			-2			
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	77			77			mA
	Outputs high	84	128	84			128	
	Outputs disabled	84	128	84			128	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		SN54AS374		SN74AS374		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	100*		125		MHz
t_w	Pulse duration	CLK high		5.5*	4	ns
		CLK low		3*	3	
t_{su}	Setup time	Data before CLK \uparrow		3*	2	ns
t_h	Hold time	Data after CLK \uparrow		3*	2	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.



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switching characteristics over recommended operating conditions (unless otherwise noted)
(see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS374		SN74AS374		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			100*		125		MHz
t_{PLH}	CLK	Q	3	11	3	8	ns
t_{PHL}			4	11.5	4	9	
t_{PZH}	\overline{OE}	Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	\overline{OE}	Q	2	10	2	6	ns
t_{PLZ}			2	7	2	6	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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APPLICATION INFORMATION

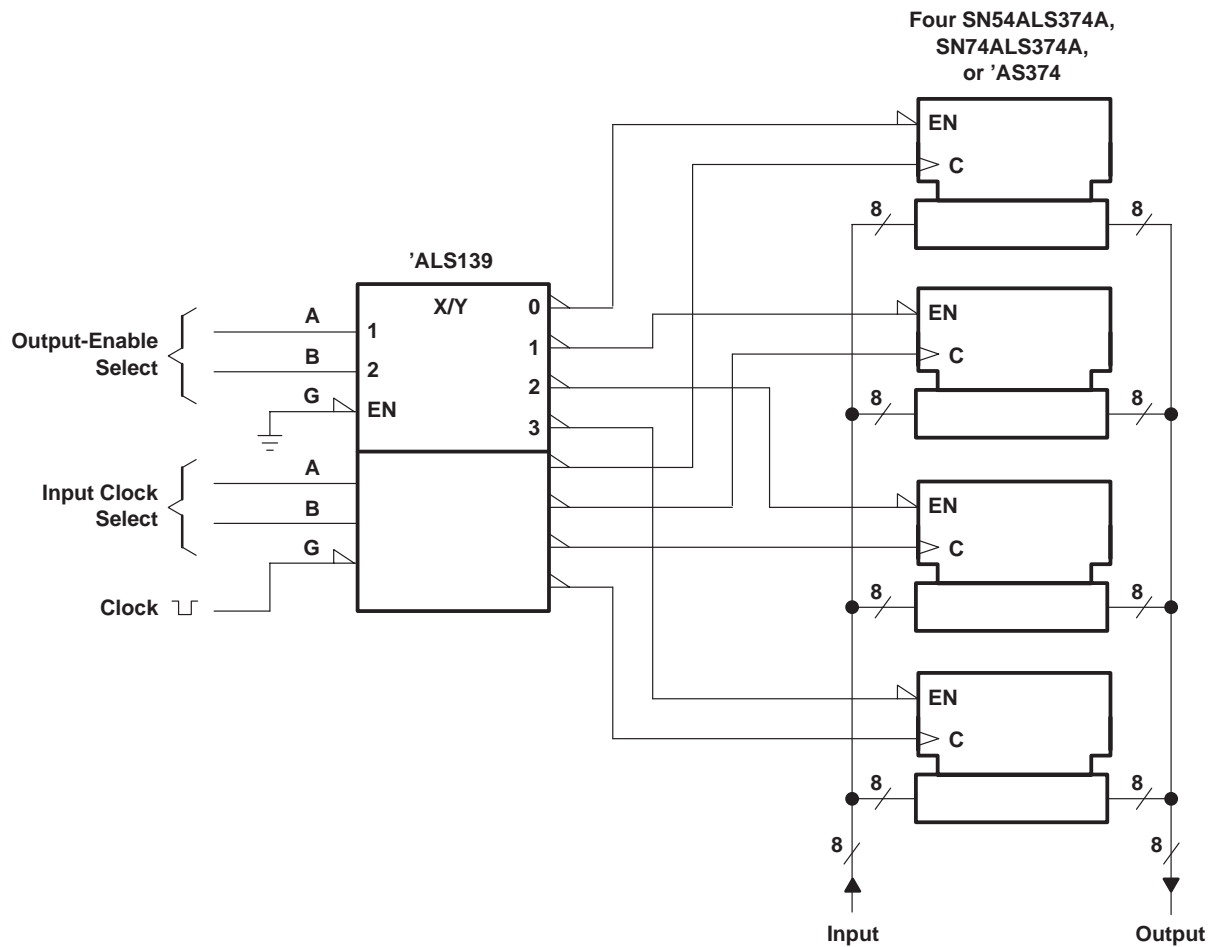


Figure 1. Expandable 4-Word by 8-Bit General File Register

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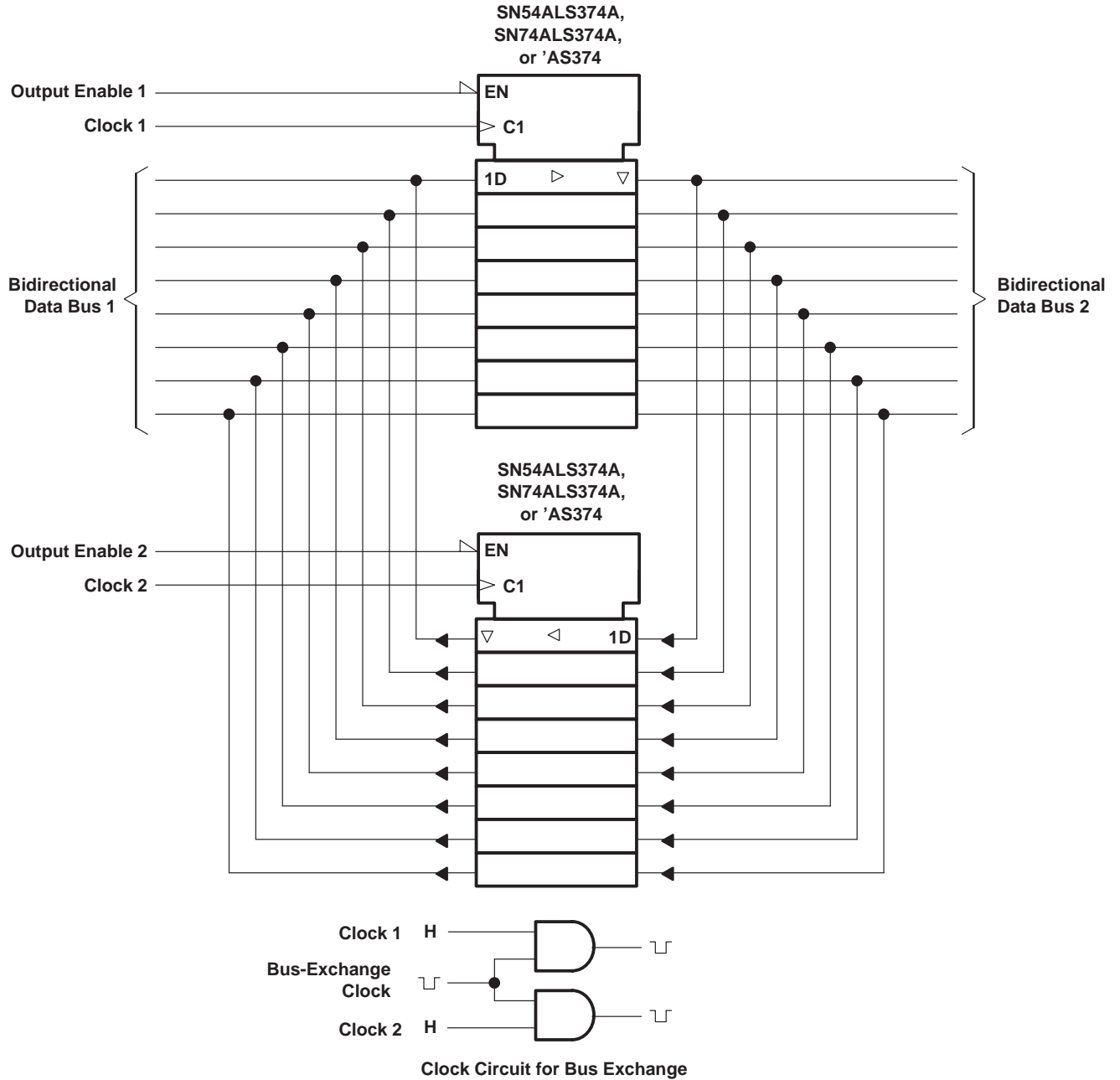
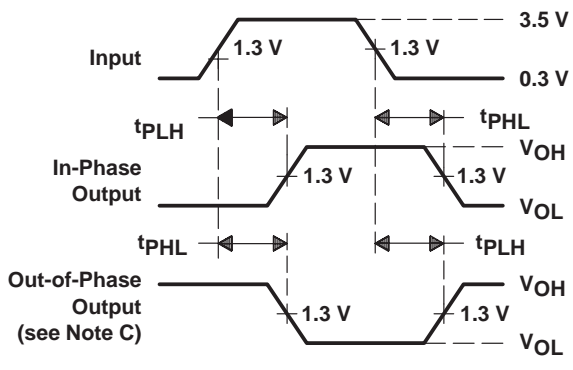
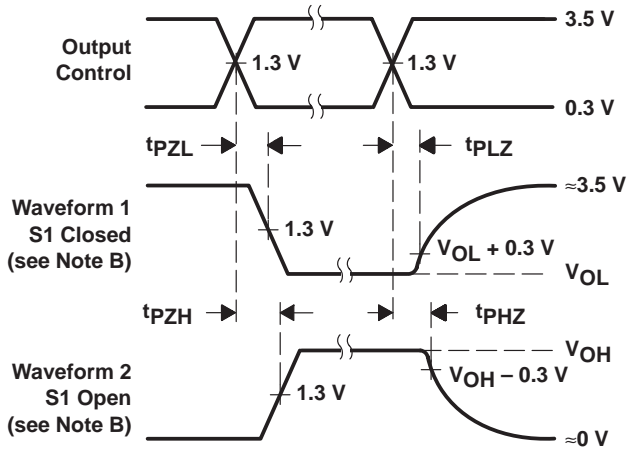
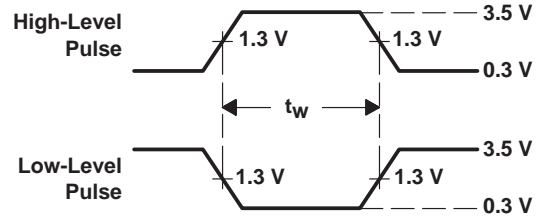
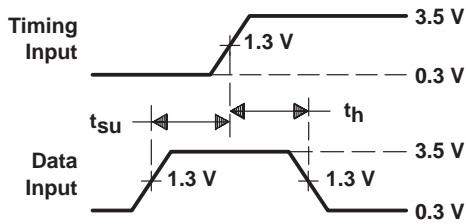
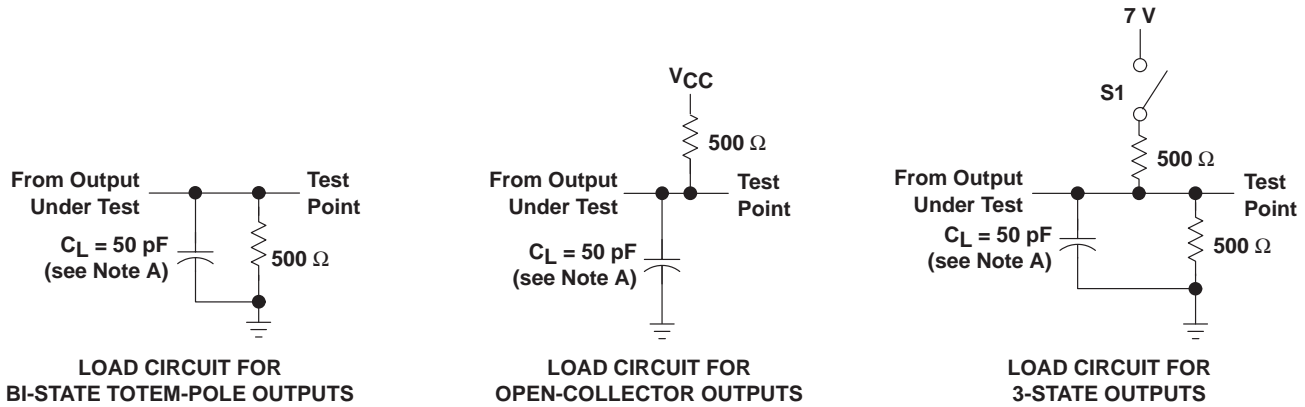


Figure 2. Bidirectional Bus Driver

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PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 - D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 - E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

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