

# SN54HC107, SN74HC107 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

D2684, DECEMBER 1982 — REVISED JUNE 1989

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

## description

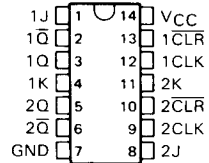
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the CLR input resets the outputs regardless of the levels of the other inputs. When  $\overline{\text{CLR}}$  is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54HC107 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC107 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

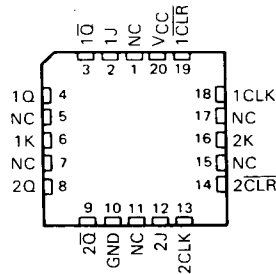
FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	X	X	X	L	H
H	I	L	L	$\text{Q}_0$	$\overline{\text{Q}}_0$
H	I	H	L	H	L
H	I	L	H	L	H
H	I	H	H	TOGGLE	TOGGLE
H	H	X	X	$\text{Q}_0$	$\overline{\text{Q}}_0$

SN54HC107 . . . J PACKAGE  
SN74HC107 . . . D OR N PACKAGE  
(TOP VIEW)

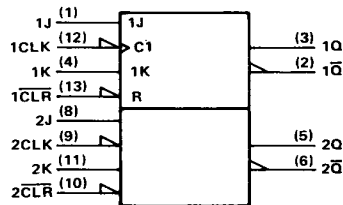


SN54HC107 . . . FK PACKAGE  
(TOP VIEW)



NC—No internal connection

## logic symbols†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, and N packages.

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



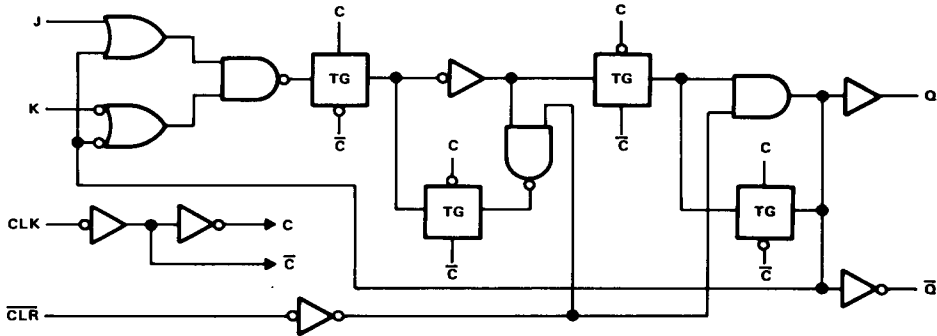
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**SN54HC107, SN74HC107**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH CLEAR**

logic diagram, each flip-flop (positive logic)



**absolute maximum ratings over operating free-air temperature †**

Supply voltage, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}(V_I < 0 \text{ or } V_I > V_{CC})$	$\pm 20 \text{ mA}$
Output clamp current, $I_{OK}(V_O < 0 \text{ or } V_O > V_{CC})$	$\pm 20 \text{ mA}$
Continuous output current, $I_O (V_O = 0 \text{ to } V_{CC})$	$\pm 25 \text{ mA}$
Continuous current through $V_{CC}$ or GND pins	$\pm 50 \text{ mA}$
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

		SN54HC107			SN74HC107			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2 \text{ V}$	1.5		1.5			V
		$V_{CC} = 4.5 \text{ V}$	3.15		3.15			
		$V_{CC} = 6 \text{ V}$	4.2		4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2 \text{ V}$	0	0.3	0	0.3		V
		$V_{CC} = 4.5 \text{ V}$	0	0.9	0	0.9		
		$V_{CC} = 6 \text{ V}$	0	1.2	0	1.2		
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) times	$V_{CC} = 2 \text{ V}$	0	1000	0	1000		ns
		$V_{CC} = 4.5 \text{ V}$	0	500	0	500		
		$V_{CC} = 6 \text{ V}$	0	400	0	400		
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

**SN54HC107, SN74HC107**  
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC107		SN74HC107		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.80		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	4.5 V		0.17	0.26		0.4		0.33		
	6 V		0.15	0.26		0.4		0.33		
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 5.2 mA	6 V								
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			4		80		40	μA
C <sub>i</sub>		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC107		SN74HC107		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t <sub>w</sub>	Pulse duration	CLR low	2 V	100		150		125	ns
			4.5 V	20		30		25	
			6 V	17		25		21	
	CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t <sub>su</sub>	Setup time before CLK↓	Data (J, K)	2 V	100		150		125	ns
			4.5 V	20		30		25	
			6 V	17		25		21	
	CLR inactive	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
t <sub>h</sub>	Hold time, data after CLK↓	2 V	0		0		0	ns	
		4.5 V	0		0		0		
		6 V	0		0		0		

**SN54HC107, SN74HC107**  
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50 \text{ pF}$  (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC107		SN74HC107		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	9		4.2		5	MHz	
			4.5 V	31	45		21		25		
			6 V	36	53		25		29		
t <sub>pd</sub>	$\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	2 V		126	155		235		195	ns
			4.5 V		25	31		47		39	
			6 V		21	26		40		32	
t <sub>pd</sub>	CLK	Q or $\overline{\text{Q}}$	2 V		100	125		185		160	ns
			4.5 V		20	25		37		32	
			6 V		17	21		32		27	
t <sub>t</sub>		Q or $\overline{\text{Q}}$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C <sub>pd</sub>	Power dissipation capacitance per flip-flop	No load, T <sub>A</sub> = 25°C	35 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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