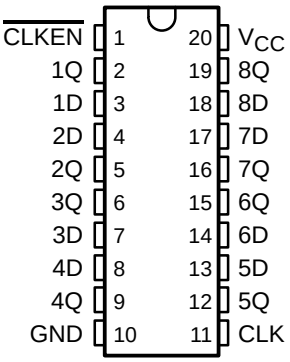
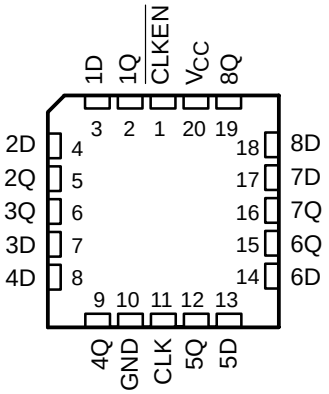
- **Operating Voltage Range of 4.5 V to 5.5 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 80-μA Max I_{CC}**
- **Typical t_{pd} = 12 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **Inputs Are TTL-Voltage Compatible**
- **Contain Eight Flip-Flops With Single-Rail Outputs**
- **Clock Enable Latched to Avoid False Clocking**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**

SN54HCT377 . . . J OR W PACKAGE
SN74HCT377 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HCT377 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These devices are positive-edge-triggered D-type flip-flops. The ’HCT377 devices are similar to the ’HCT273 devices, but feature a latched clock-enable ($\overline{\text{CLKEN}}$) input instead of a common clear.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse if $\overline{\text{CLKEN}}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at $\overline{\text{CLKEN}}$.

ORDERING INFORMATION

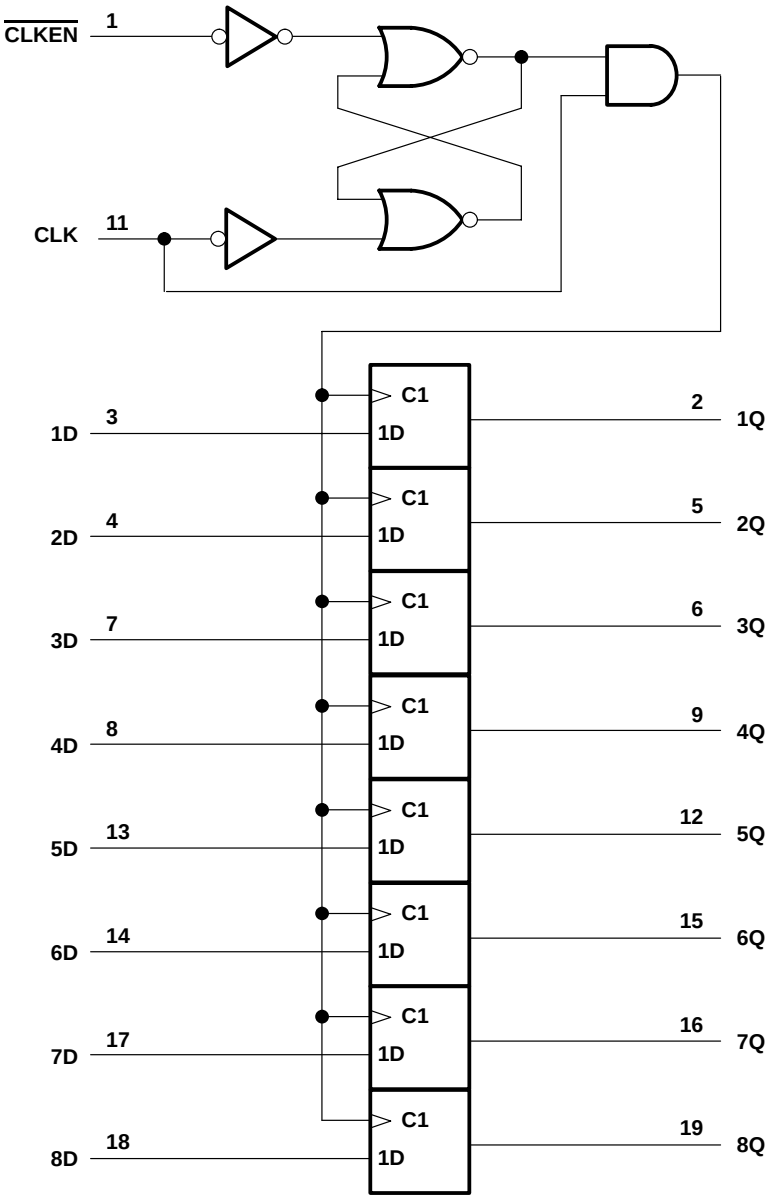
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HCT377N	SN74HCT377N
	SOIC – DW	Tube	SN74HCT377DW	HCT377
		Tape and reel	SN74HCT377DWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54HCT377J	SNJ54HCT377J
	CFP – W	Tube	SNJ54HCT377W	SNJ54HCT377W
	LCCC – FK	Tube	SNJ54HCT377FK	SNJ54HCT377FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLKEN}}$	CLK	D	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HCT377			SN74HCT377			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V			0.8			0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times				500			500	ns
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HCT377		SN74HCT377		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	4.5 V	4.4	4.499		4.4		4.4		V
		I_{OH} = –4 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	4.5 V		0.001	0.1		0.1		0.1	V
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		5.5 V			8		160		80	µA
ΔI_{CC}‡	One input at 0.5 V or 2.4 V, Other inputs at GND or V_{CC}		5.5 V		1.4	2.4		3		2.9	mA
C_i			4.5 V to 5.5 V		3	10		10*		10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HCT377		SN74HCT377		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		4.5 V		25		17		20	MHz
			5.5 V		30		19		22	
t_w	Pulse duration	CLK high or low	4.5 V	20		30		25		ns
			5.5 V	18		28		23		
t_{su}	Setup time before CLK↑	Data	4.5 V	12		18		15		ns
			5.5 V	10		17		14		
		$\overline{CLKEN}$ high or low	4.5 V	12		18		15		
			5.5 V	10		17		14		
t_h	Hold time data after CLK↑	Data	4.5 V	3		3		3		ns
			5.5 V	3		3		3		
		$\overline{CLKEN}$ inactive or active	4.5 V	5		5		5		
			5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN54HCT377					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			4.5 V	25	31		17		MHz
			5.5 V	30	37		19		
t_{pd}	CLK	Any	4.5 V		15	30		45	ns
			5.5 V		12	28		40	
t_t		Any	4.5 V		8	15		22	ns
			5.5 V		6	14		21	

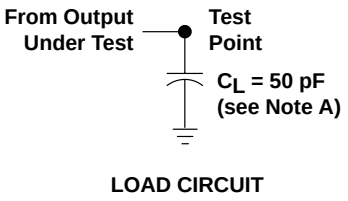
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	SN74HCT377					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
f_{max}			4.5 V	25	31		20		MHz
			5.5 V	30	37		22		
t_{pd}	CLK	Any	4.5 V		15	30		38	ns
			5.5 V		12	28		35	
t_t		Any	4.5 V		8	15		19	ns
			5.5 V		6	14		17	

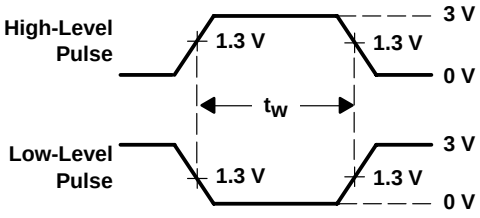
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	30	pF

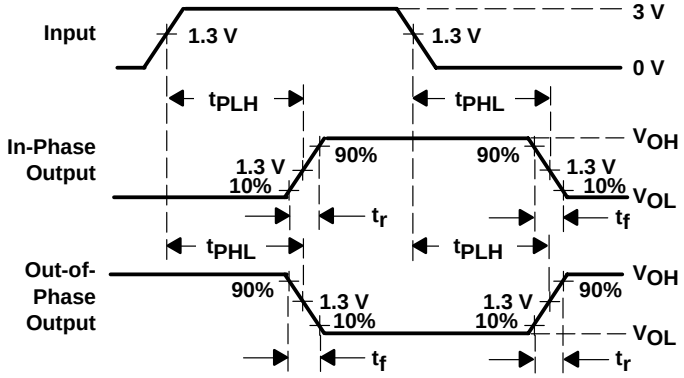
PARAMETER MEASUREMENT INFORMATION



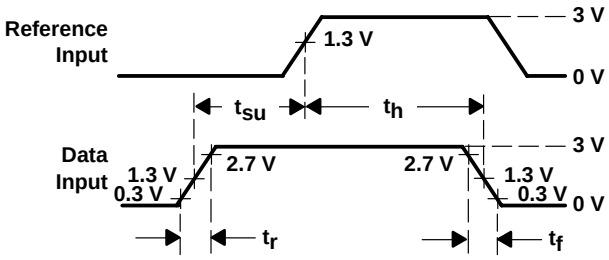
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES

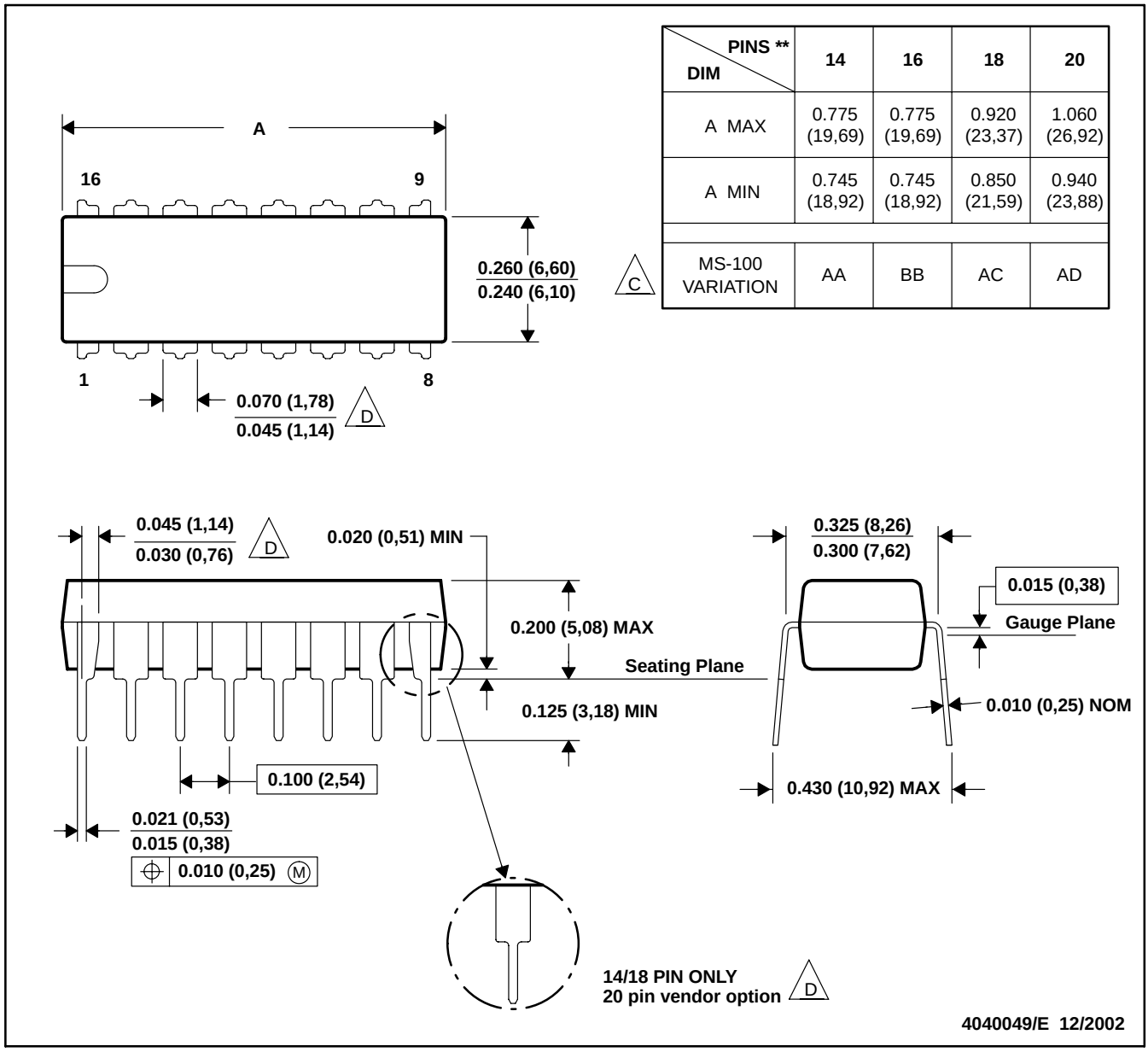
NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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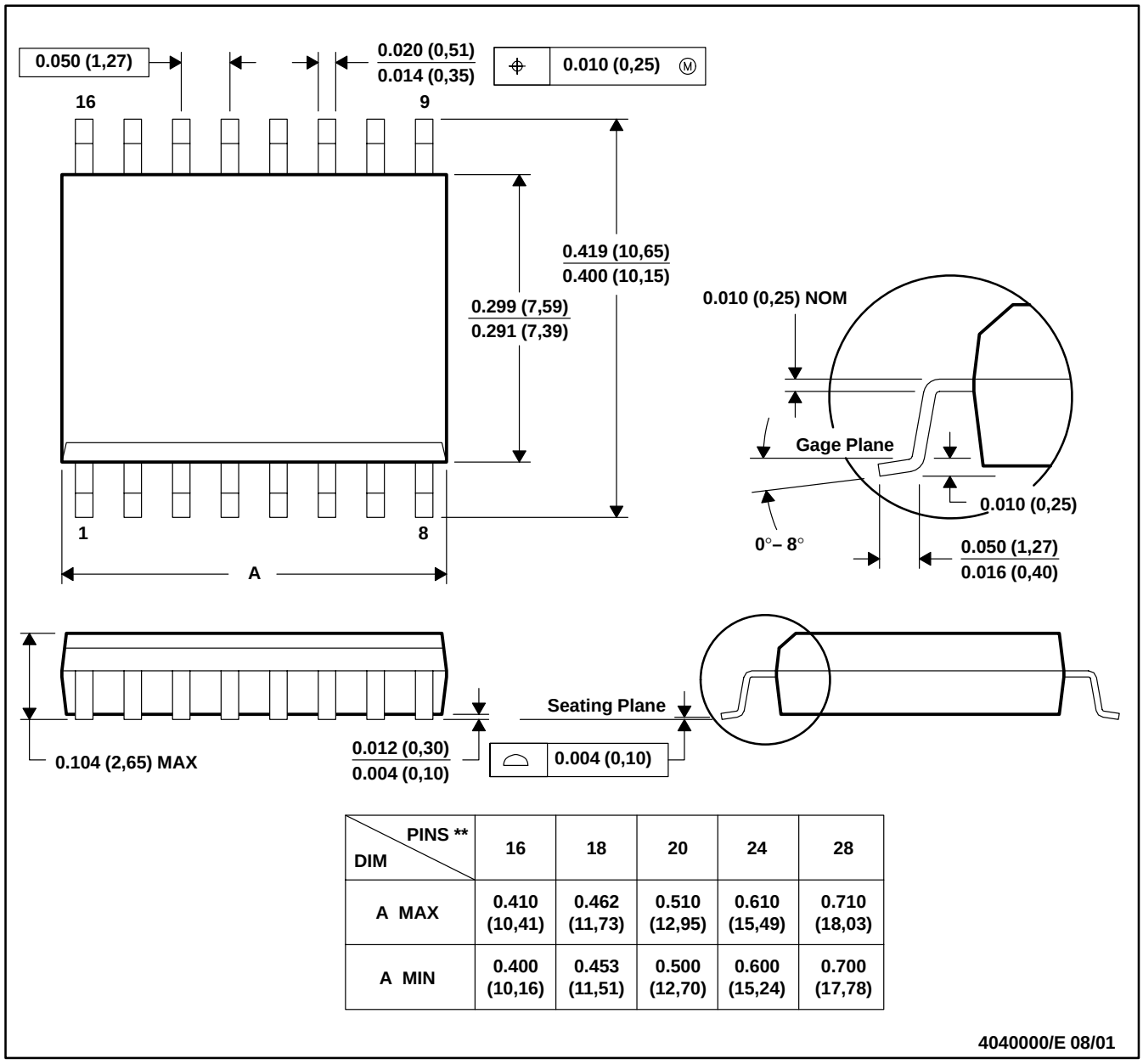
DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

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